

CHAPTER II

TIMER/COUNTER

2.1 GENERAL DESCRIPTION [3]

The Timer-Counter(T.C.) under development is a general-purpose 6-decade unit that includes a precision preset timing circuit. It can be used in either a simple or a complex counting system to control the duration of a counting interval for all the Counters in the system. When it is operated as a Counter, it accepts and counts NIM-standard slow positive pulse. Timing intervals can be set at 0.1 sec. and 0.1 min. steps and will not be displayed. Only counting data can be printed together with the counting data from any other ORTEC printing modules by an ORTEC 777 Line Printer or, through an ORTEC 432A Printout Control, or by an ORTEC 222, which is a modified Teletype.

The unit is designed for preset timing control of a counting system that includes only one Counter or up to as many as 50 Counters. The associated signals through the rear pannel of the Timer Counter permit a flexible overall system control to be designed for a wide variety of associated system accessories.

The T.C. is packaged in a MIM-standard double-width module. It includes all the connectors and controls that will be used for either manual or automatic operation and indicates the

accumulated count with 7-segment light-emitting diodes (LED) in a direct-reading display. A start indicator which is also an LED, lights to show when the T.C. is in a counting condition. The start is controlled by the manual Count/Stop switch, by the gate signal input circuit with BNC connector on the front panel. For Counter only and by a common line signal through the standard ORTEC printing loop IN/OUT connector on the rear panel.

In T.C. mode the preset time function is enabled by setting the Preset M-thumb wheel at any digit between 1 and 9 and by selecting a decade multiplier 10^0 through 10^5 by setting the Preset N-thumb wheel at any digit between 0 and 5, the T.C. stops all other Counters that are included in the printing loop whenever its time level reaches the combination that is selected. The preset time can be disabled by setting both Preset M and N at digit 0, the unit then functions as a counter only. If the Counter is allowed to overflow, this overflow is shown by an LED on the front panel; the indicator remains lit from the first overflow until the unit is reset. At each overflow an output pulse is also furnished through a rear panel connector and may be used for connection to another Counter for an increased counting capacity.

When power is first applied to the unit, reset is generated automatically by a signal through a rear panel BNC connector or through a common line in the standard ORTEC printing loop through the In/Out connector on the rear panel.

The seven segments in each of the six characters of the

digital display can be tested at any time by pressing the Display Test switch on the front panel. When this switch is pressed, all seven segments in each digit should light to provide a reading of 888 888.

The two-position toggle switch on the front panel marked Master/Slave selects the function control of this module when it is connected in a standard ORTEC printing loop. The T.C. responds to a common preset signal or furnishes it for any switch position and also responds to local gate control and reset for any switch position. But with the switch set at Master, this module can also furnish gate control and reset to all slave modules in the system. When the switch is set at Slave, this module accepts gate control and reset from the system common lines.

2.2 DATA TRANSFER SYSTEM [3]

In normal operation all Counters and Timers in the system can count until a system set signal occurs; then all modules stop accumulating and the accumulated data are transferred out to a printer, one module at a time. The signal sequence for transferring Data for 705849 from a printing scaler is shown in Fig 2.1. The Print Command signal originates in the Printout Control Module such as the ORTEC 432 A or ORTEC 777. It can be initiated manually, be triggered externally or be initiated automatically in the system reaching a preset time condition. The Start Data Transfer is supplied from The Printout Control to Counter 1, from Counter 1 to Counter 2 etc. In the system the Start Data Transfer

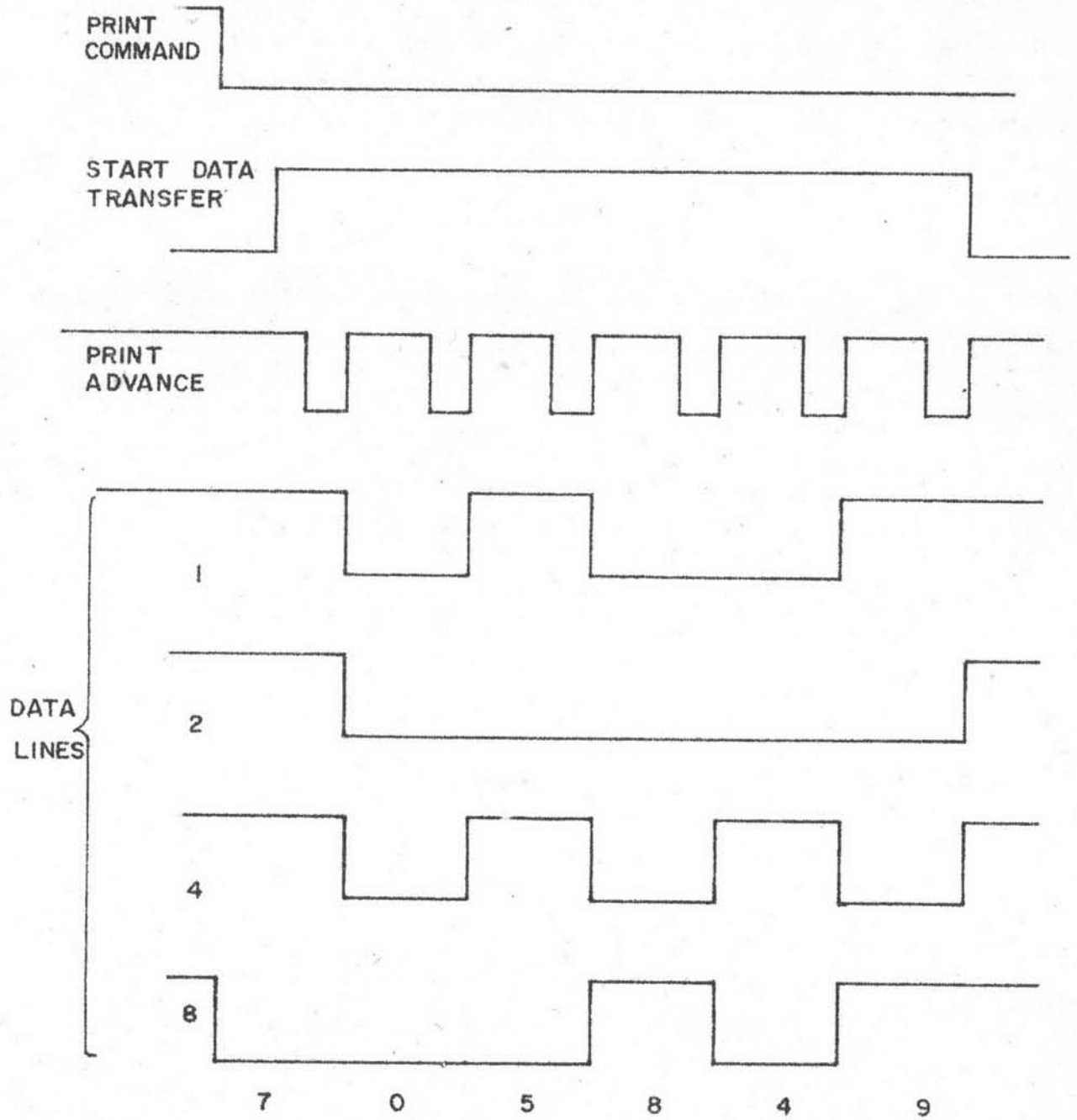


FIG. 2.1 Signal Sequence for Transferring Data for 705849.

signal from the Printout Control is called Previous Module Finish (PMF) at the input of the Timer/Counter and is called "This Module Finish" (TMF) at the output of the T.C.

The following sequence of events illustrates how a multiple-counter printing system operates:

1. A Print Command is generated manually, by a trigger or by a preset condition.
2. All modules in the system stop accumulating and remain static for 1 or 2 sec.
3. All displays are blank except the MSD in the display of Counter 1, this digit is lighted until the digit has been accepted by the output device.
4. Each of the remaining five digits in Counter 1 is printed in succession and as each digit is being printed, it is also illuminated in the display of the counter.
5. A space or a line feed is generated (depending upon the type of the Control unit under using) in the printed format after the six digits that represent the data in Counter 1.
6. The six digits for Counter 2 are printed in succession, a space or line feed is generated as in step 5.
7. This sequence repeats until the last counter has finished printing.
8. After the last set of data has been printed the system will remain in a static or noncounting mode until a new cycle is initiated and the display will be turned on.

2.3 CIRCUIT DESCRIPTION

2.3.1 General

The T.C. is a precision timer with built in counter. The counter is a 6-decade ripple scaler preceded by a precise linear discriminator and includes logic for gating. The block diagram are shown in Fig. 2.2 and 2.3. For more details the complete schematic is shown in Fig. 2.4, 2.5 and 2.6. As shown in Fig. 2.2 the timing pulses that are counted by the timer portion are derived from the line frequency. These pulses are passed through a synchronizer before enabling the gate and through a count down circuit to provide on output at either 0.1 sec. or 0.1 min. intervals. The purpose for synchronization is to prevent ambiguity of pulse recognition at the start of the gate. The preset unit then counts down pulses from the divider (counting register) and after the preset is reached then inhibits the gate. The timer portion is reset to zero, together with the main counting register, by any reset that originates locally or from the system.

In the counter portion shown in Fig. 2.3 in-put pulses that pass through the discriminator and gate are sent to the counting register to be collected. The 24 data lines, for the six 4-bit word groups from the counting register, are gated one word at a time to the four common data lines. These data lines lead to a decode for the display and to the output for the printing loop. An internal scanner gates the four bits for a digit onto the four

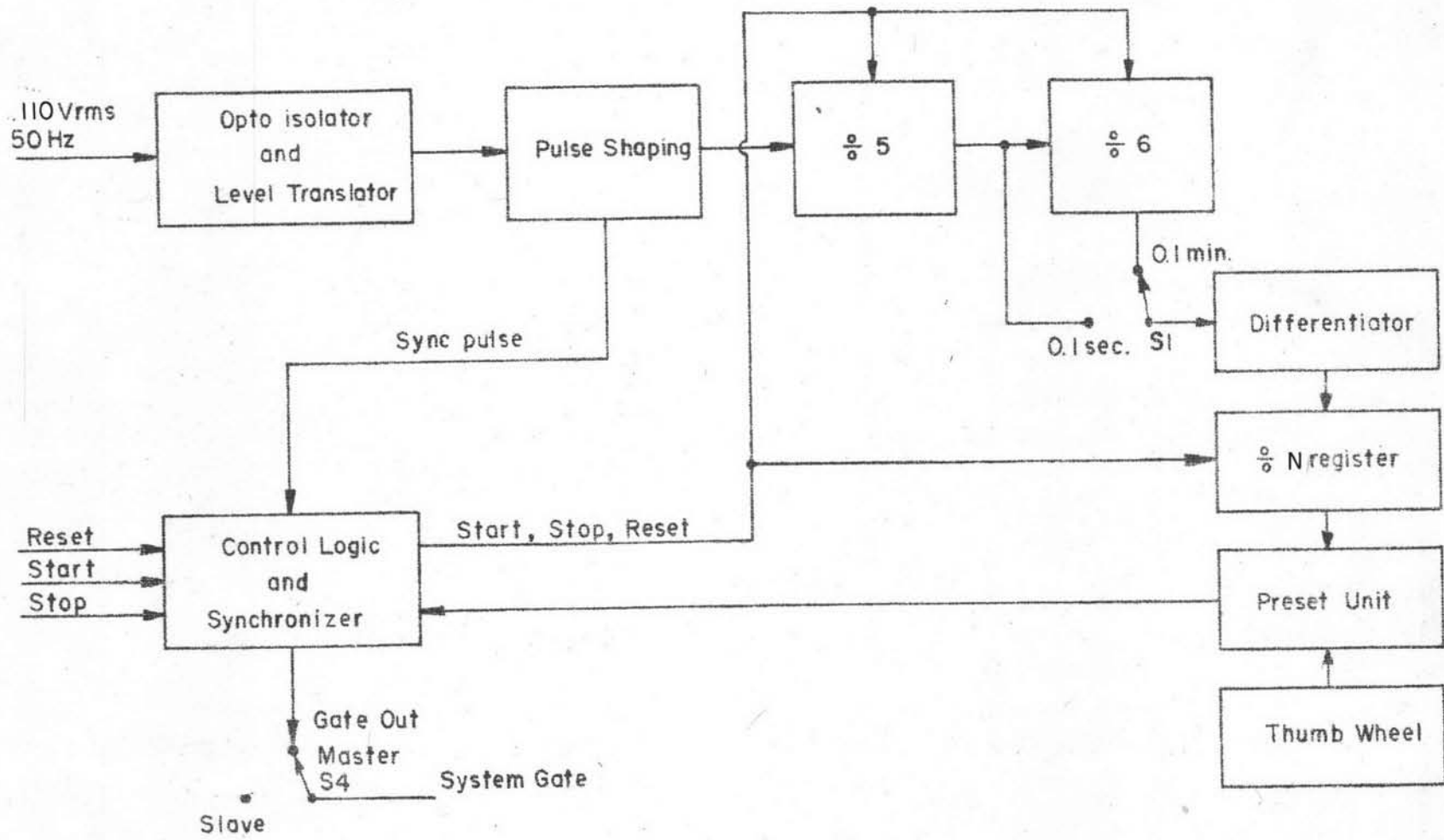


FIG.2.2 Block Diagram of The Timer Board.

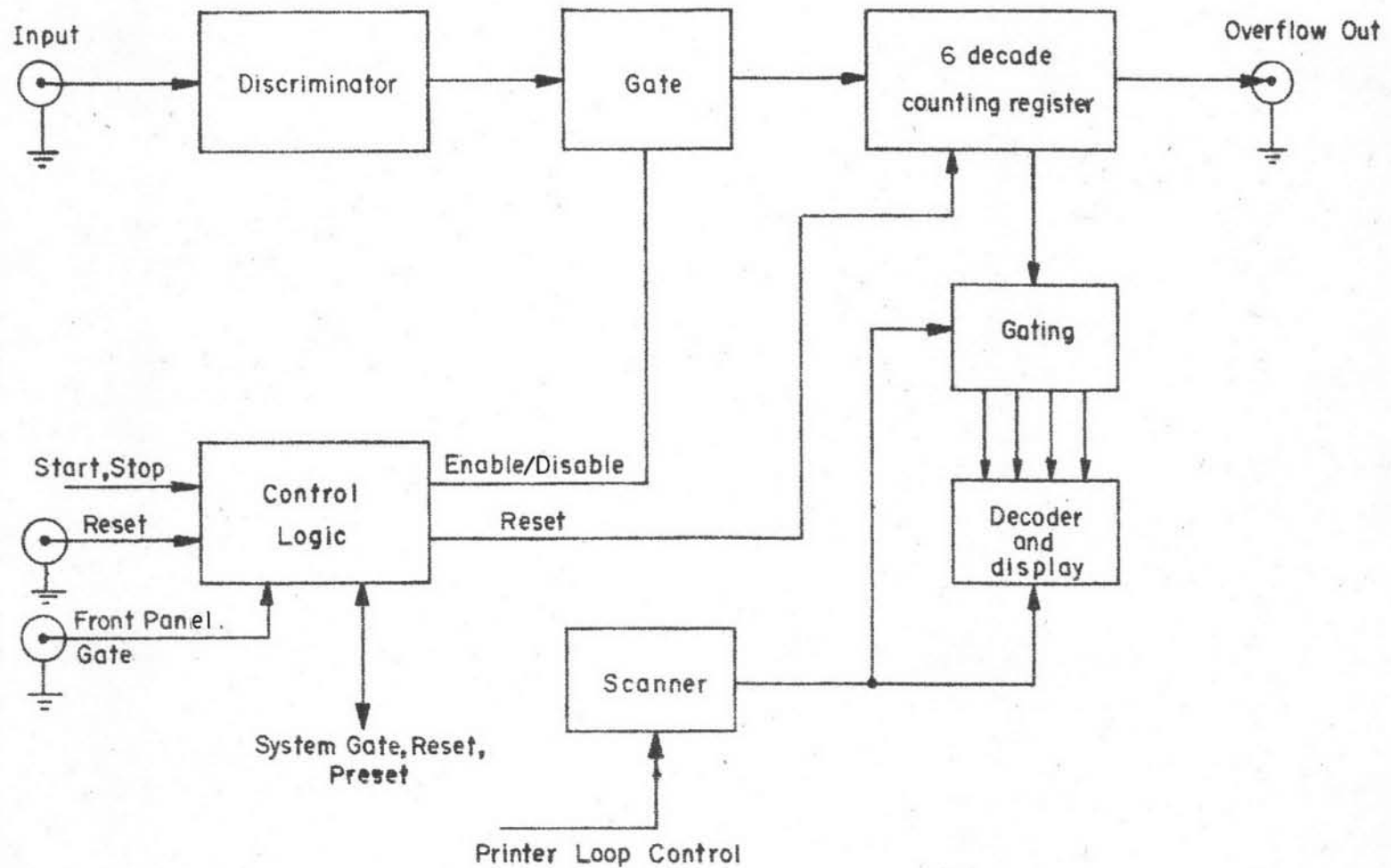


FIG.2.3 Block Diagram of The Counter Board.

common lines and also selects the proper location in the display for that digit. During non printing intervals the scanner is driven by an internal oscillator that operates at about 1 KHz and continually recycles the scan through the six digits. During printing intervals the internal oscillator is turned off and the scan is advanced at the rate of the printing accessory.

The control logic block is the same for both unit. It also includes routing to and from the system lines according to selection that is made with the Master/Slave switch.

2.3.2 Timer

2.3.2.1 Optical Isolator and Level Translator

The optical isolator consists of diode D_1 , neon tube NE_1 , compound photo transistor Q_1 and R_1 . Line voltage of $110V_{rms}$ 50 Hz is rectified by D_1 , and NE_1 is turned ON and OFF during each successive cycle. The photo transistor Q_1 then translates the ON-OFF light into a train of pulses whose period corresponds to that of line frequency and the magnitude compatible to TTL level.

2.3.2.2 Pulse Shaping Circuit:

The circuit uses IC_1 a, an inverter, to speed up the rise and fall time of the pulses from the optoisolator circuit. To prevent an ambiguity that may arise due to some jitters that may impose on the signals during the switching of Q_1 , the falling edge of IC_1 a output then triggers IC_2 , a monostable multivibrator, giving a clear rectangular pulse the width of which

is about 10 m sec.

2.3.2.3 0.1 Sec, 0.1 min.Selector, Differentiator and Divider Circuit (Fig. 2.4)

IC₃ and IC₄ scale down the input frequency by a factor of 5 and 6 corresponding to the setting of switch S₁ at 0.1 sec. and 0.1 min respectively. S₁ when in 0.1 sec. enables IC₅ c and disables IC₅ d, pulses whose period is 0.1 sec. are then passed to the differentiator circuit. For 0.1 min. IC₅ c is disabled, thus pulses of 0.1 sec. period are further divided by 6 in IC₆ before entering the differentiator circuit. The differentiator composes IC₆ b,c, P₆ and C₂ and changes the pulse of long duration into a narrow clock pulse whose width is determined by R₆ and C₂. The clock pulses are then applied to the divider circuit (IC₇ to 11) to be counted down in a multiple of ten from 10 to 10⁵.

2.3.2.4 Preset Circuit (Fig. 2.4)

Thumb wheel switches TH₁ and TH₂ preset the time in $M \times 10^N$ style, where TH₁ selects the number of N and TH₂ the number of M. Data selector IC₁₂ selects pulse from the divider network whose location corresponds to the setting of N. For each pulse transmitted through IC₁₂, a narrow negative pulse is obtained from IC₁₅ b output and being counted down by IC₁₇. IC₁₇ then compares M with the number of pulses from IC₁₂, and at the instant when M equal to the pulses counted a borrow signal is generated from IC₁₇. The borrow signal then triggers the control circuit

to inhibit the gating circuit. TH_2 when in zero setting causes the outputs of IC_{18} a and b to be High and $IC_{16}b$ to be Low thus preventing pulses from the selector IC_{12} to be counted down in IC_{17} , hence the timer portion has no influence upon the gating circuit and the module operates as a counter.

2.3.2.5 Control Logic (Fig.2.4)

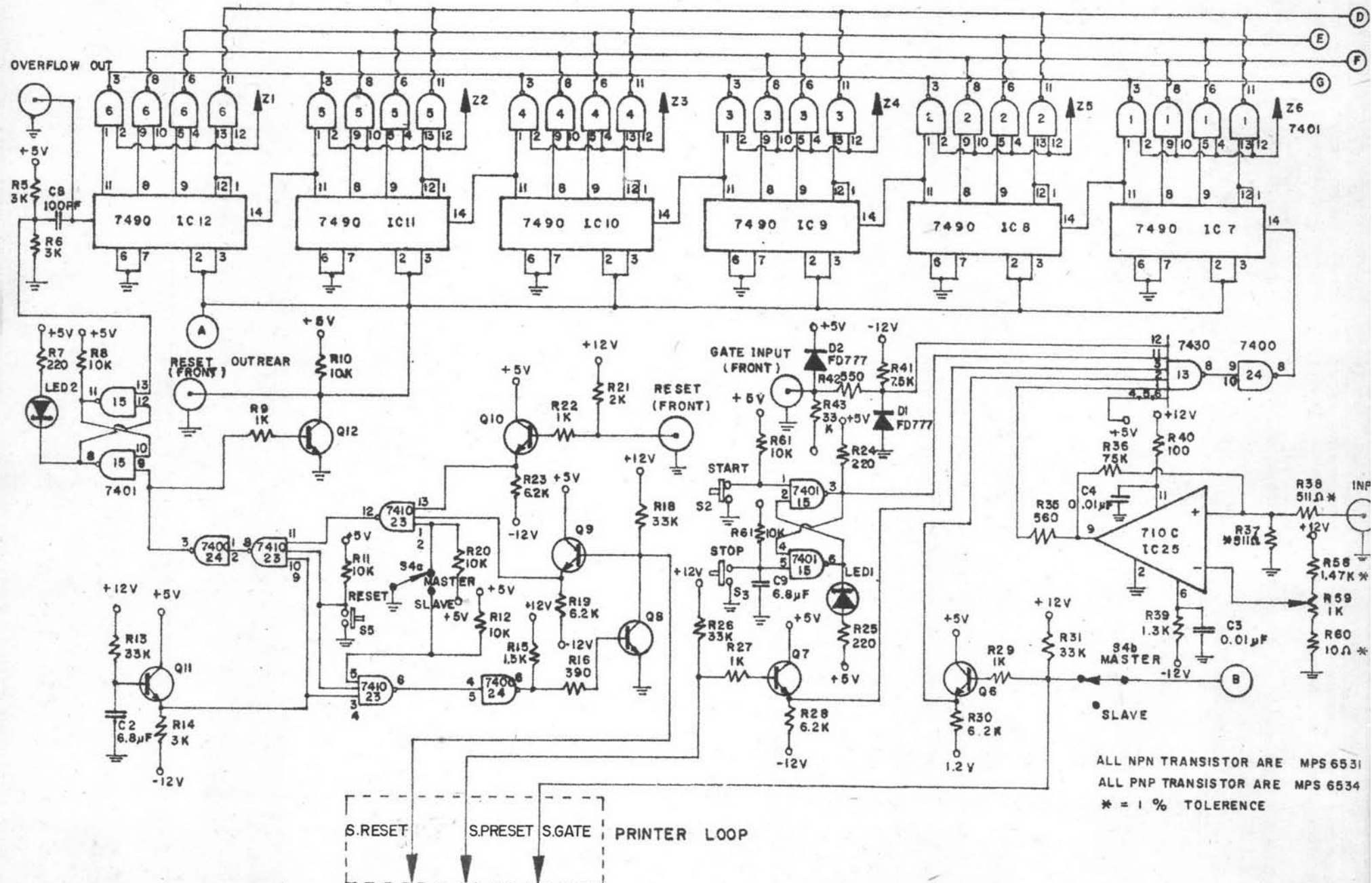
To initiate the cycle S_2 is pressed, the latching action of $IC_{13}a$ and b causes a negative pulse at the clear input of IC_{14} a. The Q output of IC_{14} a then goes Low. IC_{14} b forms a synchronizer to synchronize the initiating command and the edge of the first timing pulse. When synchronization begins Q output of IC_{14} b is high. Also the output of the synchronizer is used to drive the gate buffer Q_2 .

The stop circuit consists of IC_{18} c and d forming a switch debouncing circuit. When S_3 is released negative edge is coupled through IC_{13} c and d to IC_{14} , changes state of IC_{14} a and b thus closing the gate.

2.3.3 Counter

2.3.3.1 Pulse input circuit (Fig. 2.5)

Positive input signals in the range of 0.1 through 10 V can be applied through the front panel BNC Input Connector. They are d-c coupled through divider network R_{37} and R_{38} to the positive input of the comparator IC_{25} . The negative input to IC_{25} is the d-c level selected with Discriminator Control R_{59} on the front panel. Each input pulse whose amplitude exceeds the dis-



criminating level will generate a logic output from IC₂₅ pin 9 to drive IC₁₃. If the counter is not being reset and is in the counting condition the input pulse becomes a clock pulse into the last significant decade IC₇ and is counted.

2.3.3.2 Gating (Fig. 2.5)

With no Gate input signal and the unit operates in counter mode only ie, TH₂ is set at 0 or S₄ set at Slave and the starting circuit is initiated (S₂ is pressed), IC₁₅ pin 3 goes High enabling gate IC₁₃ to pass the signals from the discriminator to be accumulated in the data register (IC₇ to IC₁₂). When S₃ is pressed IC₁₅ pin 3 goes Low thus inhibiting the accumulation. Likewise, if there is a Gate input connection and the signal is dropped to $\leq 1.5V$ IC₁₃ pin 12 is Low and the gate is inhibited. If switch S₄ is set at Master, system gate is then applied to the timer gate output and the Stop depends on the time interval of the timer board.

2.3.3.3 Counting Register (Fig. 2.5)

The counting register includes decade counter IC₇ through IC₁₂. They are connected to form a ripple counter for all six digits of the 999,999 count capacity. IC₇ is the least significant digit and IC₁₂ is the most significant digit. The BCD identification of each digit is carried through four lines to a set of gates that will pass the identity through the four common BCD lines when gated by the scanner. The overflow from IC₁₂ pin 11 is coupled through C₁ to the latching network IC₁₅ c and d.

The first overflow after a reset will trigger the latch to drive LED₂. The overflow output is obtained from the front panel BNC connector.

2.3.3.4 Scanner (Fig. 2.6)

The scanner generates the Z₁ through Z₆ signals in sequence. It gates the most significant digit onto the common lines first with Z₁, then it gates each less significant digit in order through Z₆. When no print signal is furnished from the printer loop (nonprinting condition) an interval oscillator advances the scanner. When a print signal is present (printing interval), the scanner counts Print Advance input signals between the PMF and TMF signals, it scans through the available digits only one time during the printing cycle. The interval oscillator uses IC₂₂ a and b to generate an output signal at about 1 KHz. The output feeds through IC₂₁ pin 3 and 6 unless a print signal is present and to the clock input of IC₁₉ pin 1. The binary output IC₁₉ is fed to the 4 to 16 line decoders IC₁₇ used as a 3 to 6 line decoders. When all the three bits at the input of IC₁₇ are zero, it identifies zero at pin 1, this generates Z₁ at IC₁₇ pin 1 and \bar{Z}_1 at IC₁₆ pin 8. The next oscillator pulse changes the count for a \bar{Z}_2 at IC₁₇ pin 2 and Z₂ at IC₁₆ pin 2. This sequence signal operation continues until each signal has been generated in turn and an oscillator pulse advances the counter out of its Z₆ condition and back to Z₁ and the scanning is recycled immediately.

2.3.3.5 Decode and Display (Fig. 2.6)

The four bits that are present on the common lines

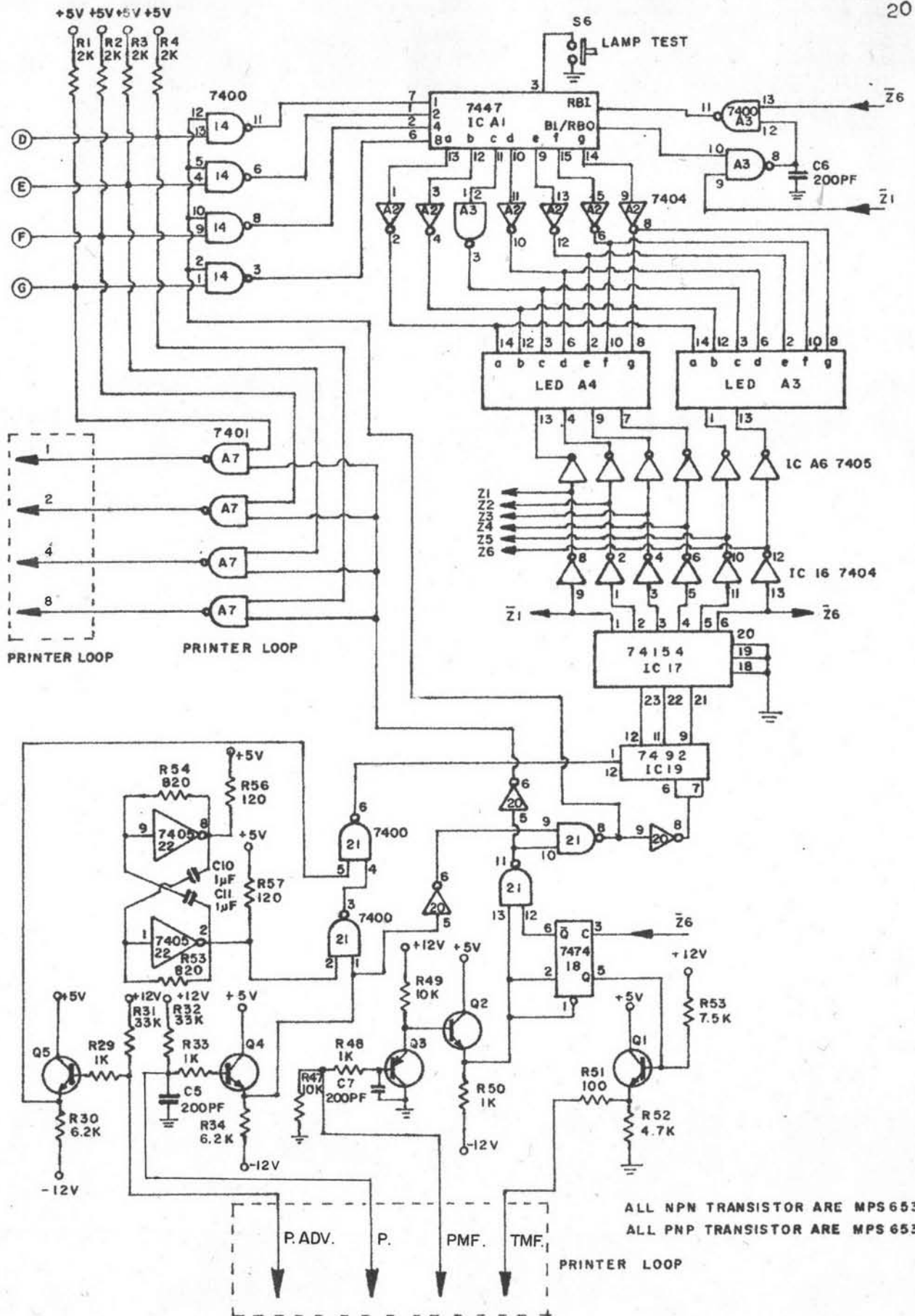


FIG.26 Schematic Diagram for Strobing Display and Printout Control.

at any time represent one of the digits. This combination is decoded in IC_{A1} and furnishes the correct configuration of blanking and illumination to the seven LED segments at the anodes of all six digits in the display LED_{A3} and LED_{A4} . The scanner signal will have selected which of the six digits in the counting register is gated onto the four common lines, and the same signal completes the cathode path of the proper digit in the display. For example when Z_6 is present, the cathode of the least significant digit in the display is selected, and the digit is identified through IC_{14} the four common lines, and IC_{A1} to the segments of LED_{A3} for that digit.

For reference, the seven segments are identified a through g. Viewed from the front of the display as shown in Fig.2.7 Any digit between 0 and 9 can be obtained by selective blanking of these segments. When switch S_6 is pressed IC_{A1} provides no blanking for any segment and the display should illuminate all segments for a reading of 888 888. IC_{A3} pin 11 provides for automatic blanking of insignificant zeros in the display. At Z_1 time, for the most significant digit, IC_1 , receives a signal from IC_{A3} pin 6 to blank all segments if all inputs to IC_1 are Low. Internal logic in IC_{A1} (RBO) resets the blanking control through IC_{A3} pin 8 when it identifies any digit other than zero from the four common lines. So until there is a digit that is non zero, nothing can be shown in the display. When the scan reaches Z_6 the signal at IC_{A3} pin 11 will remove the automatic blanking leaving the least significant digit to be always displayed.

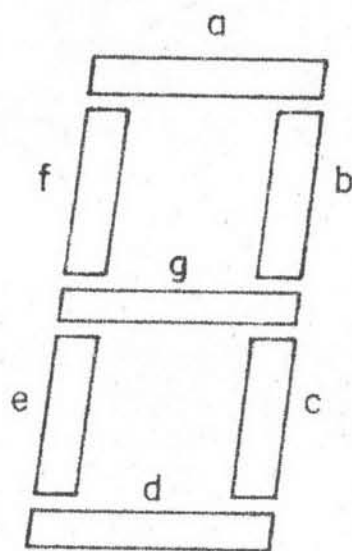


FIG. 2.7 Segments Identification for a 7-Segment Display.

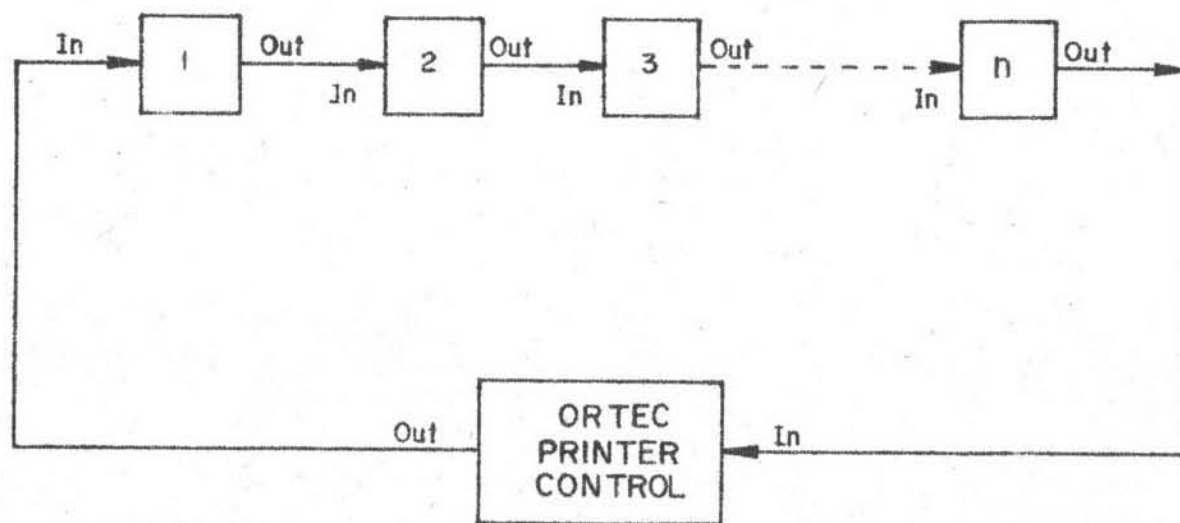


FIG. 2.8 Timer-Counter Interconnection for System Operation.

2.3.3.5 Printing Circuit (Fig.2.6)

A printing loop is formed by cabling the printing modules and either an ORTEC 777 Line Printer or 432A Printout Control in a circuit as shown in Fig. 2.8.

In the T.C. the system preset is accepted through Q_7 of the counter board to turn off the input gate IC_{13} pin 8. This prevents any advance of the counting register. The print signal is accepted through pin 5 of the In (Out) connector and Q_4 to inhibit oscillator gate IC_{21} pin 3' to reset the scanner to Z_1 through IC_{20} pin 6, IC_{21} pin 8 and IC_{20} pin 8 and to clamp all four gates of IC_{14} to provide a "code 15" input to IC_{A1} that blanks the display. The module then waits until its turn to be printed out. A Previous Module Finish (PMF) input from the printer loop signals the printing cycle for the module. The PMF originates in the control module if the T.C. is Counter 1 and the system of Fig.2.6 or is the TMF output from the previous Counter for any of the other positions in the loop. The PMF input releases the reset latch at IC_{21} pin 8, releases the blanking clamp to IC_{14} and enables gate IC_{A7} to transfer the data from the four common lines in the T.C. to the system common lines. The most significant digit is gated from IC_{12} through IC_6 by Z_1 for transfer to the Printer and to the display. At print advance, when the digit has been accepted by the Printer, the signal through Q_5 and IC_{21} pin 6 advances IC_{19} for the Z_2 digit that is in IC_{11} . Each subsequent print advance selects the next digit until Z_6 , after which IC_{18}

generates a TMF output and restores the off-line condition of the T.C. When the last module in the loop furnishes TMF to the next control module, the control module determines the next sequence. It can remove preset, generate reset, or whatever is appropriate to the program that has been selected.

2.3.3.6 Master/Slave Circuits (Fig. 2.5)

Switch S_4 selects the mode of operation for this function. When the switch is set at Master, internal reset and gate signals are furnished to the system reset and gate lines for control of any other modules that are for Slave.

With S_4 set at Master, IC₂₃ pin 12 is held High, thus prevents system reset to enter IC₂₃ pin 8. If Reset push button S_5 is pressed a reset signal is generated via IC₂₃ pin 8, IC₂₄ pin 3, Q₁₂ collector to reset the module and to drive the system reset line via IC₂₃ pin 6, IC₂₄ pin 6 and Q₈.

If S_4 is set at Slave, timer gate out is disconnected from the system gate by S_4 and the module loses control upon other modules in the system. Since IC₂₃ pin 6 is held High, module reset cannot pass through IC₂₃ pin 6, IC₂₄ pin 6 and Q₈ to the system reset.

2.3.3.7 Local Reset (Fig. 2.5)

Local reset is generated at IC₂₃ pin 8 if any of its inputs goes Low. The inputs originate with switch S_4 , from Reset BNC through Q₁₀, IC₂₃ pin 12, from Q₁₁ at the time power is first applied to the unit, or from the system reset line through IC₂₃ pin 12.

2.3.3.8 Power Supply

The unit derives the power supply from the NIM Power Supply which provides a ± 12 V DC at 2A, ± 24 V DC at 1A and 115 V AC. The + 5 V DC required by the digital IC's is obtained from the regulator circuit.
