CHAPTER 2

CIRCUIT DESCRIPTION

The simplified block diagram of the high voltage power supply is shown in Fig. 1. Power transformer is used to provide low ac voltage to dc power supplies I, II, and III. Dc power supply I supplies power to the inverter through the pass device in the regulator where power supply II delivers essential power to the control circuits in the regulator and the protection circuit. Dc power supply III supplies power to the oscillator driver which comprises an astable multivibrator and inverter driver. The output transformer in the inverter steps up the low square-wave voltage to a higher one to the voltage multiplier which provides a dc voltage four time as high as the peak value of the square-wave voltage at the secondary winding of the output transformer. To reduce the ripple voltage at the output which occurs through output loading a filter is provided. High voltage is fed back directly to a voltage divider network the output of which is then compared with an internal reference voltage giving an error signal to control circuits in the regulator. The regulator is used to provide voltage level to the inverter determined by the internal reference voltage. The meter M is used as a coarse indicator for high voltage level at the output. Thus variation of the output high voltage is achieved by varying the reference voltage through dial control at the

front panel. The protection circuit composes of an amplifier, a comparator and a shut down device. They are used to protect the output from over loading or detrimental shorting. The sensing voltage which develops across a resistor in the output is amplified and the level is compared with the reference. When the output is loaded more than 2 mA, the shut down device will turn down the reference voltage of the control circuit in the regulator to zero level and no more power is supplied to the inverter.

2.1 INVERTER [1], [2], [3], [9]

The heart of the high voltage power supply is the dc-ac inverter and it deserves to be mentioned first.

In general, there are two types of basic practical circuit of voltage inverter used in high voltage power supply. They are

1. self-oscillating type,
2. driven type,

only the latter will be discussed in the following section because of its high efficiency and frequency stability from zero to full load.

2.1.1 Driven Type Inverter

Figure 2 represents a simplified schematic diagram of a driven type inverter. The inverter consists of a pair of push-pull power transistors Q_{11} and Q_{12} as power inverter and an output transformer T_1. The switching operation is accomplished by altering the base drive of both

transistors. As Q_{11} turns on and Q_{12} turns off, current is drawn from V_{cc} supply through winding Tp1 creating a magnetic field within the core in one direction. Before the magnetic flux reaches the saturation, Q_{11} will turn off and Q_{12} will turn on instead. This drives the current through winding Tp2 creating the magnetic field in the opposite direction. Again, before this reverse magnetic flux reaches the sturation, Q_{11} will turn on and Q_{12} will turn off to repeat the cycle of switching process. As Q_{11} and Q_{12} alternately conduct, an ac square wave voltage will be produced on the secondary winding Ts.

As having seen above, the supply voltage, the frequency of the oscillation, and the maximum flux linkage are all related. The exact form of this relation is

$$V_{cc} = 4f\ T_p A_c B_{max} \times 10^{-8} \qquad \text{.....(2.1)}$$

where $B_{max} = 0.8\ B_{sat}$ is recommended.

The output voltage may be changed by altering the number of turns of the secondary winding in accordance with the familiar ideal transformer equation :

$$\frac{T_p}{T_s} = \frac{V_{in}}{V_{out}} \qquad \text{.....(2.2)}$$

Since the highest efficiency in power conversion is desirable, the following design criteria must be considered.

2.1.2 Transistor Selection

The transistors must possess sufficient capabilities in three areas:

a) Adequate current rating : The transistor type selected must be capable of carrying maximum collector current.

b) Adequate breakdown voltage rating : The transistor must have collector-emitter breakdown voltage in excess of the sum of the supply voltage plus the induced winding voltage plus any voltage spikes encountered during turn-off. A minimum breakdown voltage rating of the transistor of 2.25 times the supply voltage is recommended.

c) Power rating : The transistor must be able to withstand the maximum power excursions occurring during switching.

2.1.3 Transformer Consideration

2.1.3.1 Core : The selected core should provide high efficiency in power conversion while its size is small. Ferrite cores are most suitable for inverter applications. The high resistivity of ferrite reduced eddy current losses to a minimum. In addition, ferrites can be obtained with high permeabilities and square shape of hysteresis loops. The reason for the desirability of a square hysteresis loop is the independence of the frequency of transistor parameters and loading. For the same saturation flux density, less magnetization force is required for a material of high

permeability. This means less magnetization current is required and more current can be applied to the load. Power loss in the core determines not only the efficiency but also the frequency range in which the core can be operated safely without overheating. Owing to simplicity of manipulation ferrite cores in EE, EI, EP and pot forms are widely used.

2.1.3.2 Flux Density : For driven type inverter, the usable maximum flux density is assumed to be lower than saturated flux density because if the inverter is driven into saturation useless collector power dissipation will occur and overheating of transistors may result. To ensure that this will not happen, the maximum flux density taken into calculation should be 10-20 percent lower than saturated flux density.

2.1.3.3 Frequency : A selection of frequency of operation is very important in specifying the output power rating, because the maximum power that can be handled by a core is given by

$$P_{max} = 2k_w B_{max} f J W A_c \times 10^{-8} \qquad \text{.....(2.3)}$$

where k_w is a factor used in determining maximum power handling of a core.

The losses in ferrite core are predominately due to hysteresis loss which is

$$P_h = f W_h V \times 10^{-7} \qquad \text{.....(2.4)}$$

where $$W_h = \frac{1}{4\pi} \oint HdB$$

$\oint HdB$ = loop area of B-H curve

V = volume of core

f = frequency of operation

Since both P_{max} and P_h vary linearly with frequency, the inverter efficiency is independent of frequency. Now we can conclude that the optimum frequency of operation for a given core is; from eq. (2.3)

$$f = \frac{P_{max} \times 10^8}{2k_w B_{max} J W A_c} \times k_i \qquad \text{.....(2.5)}$$

where k_i is a factor to compensate for the thickness of the interlayer insulation and $k_i = 2$ is found from experiment for mylar film 1.5 mils thick.

Additionally, although the efficiency of inverter using ferrite core is independent of frequency, over-all efficiency will decrease at higher frequency due to transistor switching loss. So the calculated frequency should lie between 1-15 kHz.

2.1.3.4 Winding : By putting equation (2.1) in a form more suitable for design, one obtains number of primary turn which is

$$T_p = \frac{V_{in} \times 10^8}{4f A_c B_{max}} \qquad \text{.....(2.6)}$$

To get the number of turns of secondary winding, multiply a factor K_1 into equation (4.2) to compensate for transformer voltage drop and losses, then equation (2.2) becomes

$$T_s = K_1 T_p \frac{V_{out}}{V_{in}} \qquad \text{.....(2.7)}$$

where $K_1 = 1.05$ is recommended.

In selecting the value of current density of conductor wire there are some factors to be considered. The optimum value of current density can be determined from eq. (2.8) as follows,

$$J = \left[\frac{2P_{max} n}{k_w l_w W} \right]^{1/2} \qquad \text{.....(2.8)}$$

where n is an allowable fraction of voltage drop in wire

There will be a current break down (overheating) occurring in the winding if the value of J used is too high. To ensure that this will not happen, the value of 1/J should never be less than 700 circular mils per ampere and up to 1000 circular mils per ampere is desirable in larger units. The wire size of the wiring can be calculated from eq. (2.9) and (2.10) as follows,

$$\text{wire size of } T_p = \frac{1}{J} \frac{I_c}{2} \qquad \text{.....(2.9)}$$

$$\text{wire size of } T_s = \frac{1}{J} I_{out} \qquad \text{.....(2.10)}$$

In addition, the secondary winding should be wound on the bobbin first, then the primaries are wound in bifilar form on top of the secondary winding. Bifilar winding is achieved by winding both primaries at the same time putting the wires on the bobbin parallel to each other. This is done to minimize voltage spikes due to leakage inductance. Electically, it seem to make little difference as to the order of the windings

on the core except that owing to its smaller diameter the secondary wire is more easily wound the bobbin than on top of the heavier primary wire.

2.1.4 Circuit Refinement

Resistive loading is the most desirable for inverters because the load current is constant during a half cycle of operation. For capacitive load, the load current will be larger during the early portions of the half cycle and additional base drive may be needed to keep the transistor saturated during the entire half cycle. Figure 3 shows collector waveforms for resistive, and capacitive loading.

In addition, storage time of the high voltage transistors can cause excessive currents in the transistor during switching. In the circuit of Figure 2, when transistor Q_{11} turns on and if transistor Q_{12} does not completely turn off, the current in both transistors will rise to a very high value. The modifications in the base circuit shown in Figure 4 can help to reduce this problem. The capacitors C_9 and C_{10} will remove out some storage charge in the base junction. The base circuit time constant should be much smaller than the period of operation to assure that both C_9 and C_{10} is completely discharged before the next half cycle starts. So the equation is :

$$R_{23}C_9 = R_{24}C_{10} \leq \frac{T}{20} \qquad \text{.....(2.11)}$$

where $R_{23} = R_{24}$, and $C_9 = C_{10}$.

As the transistor turns off, the spike voltage may exceed the breakdown voltage of the transistor and the transistor may be destroyed. To avoid this, the leakage inductance of the input windings should be minimized by using bifilar windings on the input as mentioned in 2.1.3.4. And to assure that the transistor will never be destroyed, a diode R-C clamp circuit shown in Figure 5 can be used without slowing down the switching speed or requiring excessive power dissipation in any active device.

The $R_{25}C_{11}$ time constant must be large enough to avoid voltage rise on the clamp during switching. The resistor R_{25} must be quite large to avoid excessive power dissipation. Diodes D_3 and D_4 must be able to handle the peak collector current and fast enough so that breakdown doesn't occur before the diodes turn on. The diodes must also be able to block twice the supply voltage. The values of R_{25} and C_{11} are given by

$$R_{25}\, C_{11} \geq 20\, T \qquad \text{.....(2.12)}$$

2.2 OSCILLATOR [5]

Since output power inverter switching is accomplished by square wave driving action, a basic astable multivibrator with driver circuit in Figure 6 is introduced.

Refer to Figure 6, transistors Q_7 and Q_8 form a regenerative switch in conjunction with resistance-capacitance components to produce a switching action. The discharge

action of both capacitor C_7 and C_8 are used to produce square wave across R_c and this square wave is directly coupled to the base of the driver transistor Q_9 and Q_{10}. Then the square wave output from the collector of transistor Q_9 and Q_{10} drive the base of power inverter Q_{11} and Q_{12}. Diode D_1 and D_2 are used to prevent Q_7 and Q_8 from emitter-base voltage breakdown which will occur during reverse biasing.

The period of oscillation, T can be calculated from equation (2.13) as follow:

$$T = 2\tau \ln(2) \qquad \text{.....(2.13)}$$

where $\tau = R_b C$

This equation approximates the value for T because R_c, V_{BE} (SAT), V_{CE} (SAT), and V_E of Q_7 and Q_8 are neglected since

$$V_{cc} \gg V_{BE} \text{ (SAT)}$$

$$V_{cc} \gg V_{CE} \text{ (SAT)}$$

$$V_{cc} \gg V_E$$

and $$R_b \gg R_c$$

2.3 VOLTAGE MULTIPLIER [4]

Voltage multipliers are essential for high voltage applications because the induced voltage on secondary winding of the inverter transformer is limited by the insulation breakdown of the secondary winding. The voltage multiplier is a convenient and efficient method of

obtaining high dc voltages but its voltage ripple and attenuation factor can affect the inverter design. Some helpful design equation are provided in the following paragraphs.

2.3.1 The Ideal Multiplier

An unloaded two-stage multiplier is shown in Figure 7. Capacitor C_{20} is charged through diode D_{13} on each negative half cycle of the square-wave generator to voltage V_p. On the positive half cycle, charge is transfered through C_{20} to C_{21} and also through C_{22} to C_{23}. Since no charge is lost and stray capacitance is neglected, the output voltage rapidly approaches the ideal voltage, $E_{o_{ideal}}$. For an M-stage multiplier.

$$E_{o_{ideal}} = M\, V_{pp} \qquad \text{.....(2.14)}$$

2.3.2 Effect of Load Current

The two stage multiplier with a finite resistive load is shown in Figure 8. If each multiplier capacitor has value "C_m", the output ripple voltage, E_{IR} is

$$E_{IR} = \frac{I_L}{fC_m} \cdot \frac{M(M+1)}{2} \qquad \text{.....(2.15)}$$

and the dc output, $E_{o_{DC}}$ is

$$E_{o_{DC}} = M\, V_{pp} - \frac{I_L}{fC_m} \sum_{i=i}^{M} (i)^2 - \frac{M\,(M+3)}{2} \cdot V_D \qquad \text{.....(2.16)}$$

where I_L = load current

f = frequency of the inverter

V_p = input peak - peak voltage

V_D = forward diode voltage

2.4 FILTER [6]

Since the dc output with low ripple voltage is desirable for nuclear radiation application, the RC input filter circuit is used to minimize output ripple. The 3-stage RC input filter is shown in figure 9. The design equations for the N-stage filter are as follows:-

For one-stage RC input filter, the output ripple voltage, E_{oR} is

$$E_{oR} = \frac{X_{C_1}}{R_1} \cdot E_{IR} \qquad \text{.....(2.17)}$$

where $X_{C_1} \ll R_1$, and $X_{C_1} = \frac{1}{2\pi f C_1}$

For N identical stage RC input filter with resistor R_F and capacitor C_F, E_{oR} is

$$E_{oR} = \left[\frac{X_{CF}}{R_F}\right]^N \cdot E_{IR} \qquad \text{.....(2.18)}$$

2.5 REGULATOR [7], [8], [10]

In general, there are two types of basic voltage regulator (a) series-dissipative regulator, (b) switching regulator. Only the former is suitable in the high voltage power supply application since no voltage spikes occur in this type of voltage regulator. A block diagram of series-

dissipative regulator is shown in Figure 10.

2.5.1 Comparator

A voltage comparator which is the heart of the regulator comprises an error amplifier and one unity-gain buffer as shown in Figure 11. The error amplifier compares a voltage which is sampled from the H.V. output through a feedback network with a reference voltage. Since this network forms a negative feedback loop, the pass device is controlled to supply current to the inverter in order to produce the voltage at the H.V. output in such a way as to minimize the difference between those two input voltages of the error amplifier. Unity-gain buffer is used to increase the input impedance of the error amplifier. The integrated circuit operational amplifiers which have a differential input and a single-ended output shown in Figure 12 are used as an error amplifier and unity-gain buffer. In addition, capacitor C_{13} in Fig. 11 is used to prevent the regulator to switch and act as a true series-dissipative regulator.

2.5.1.1 Error Amplifier : In general, the ideal operational amplifier is characterized by

1. Infinite voltage gain
2. Infinite input resistance
3. Zero output resistance
4. Infinite bandwidth
5. Zero offset

Two very powerful tools for circuit analysis and design are implied by the ideal properties listed above, namely;

(a) as a result of infinite input resistance, no current flows into either input terminal; (b) because of the infinite gain, when negative feedback is applied around the amplifier, the differential input voltage is zero. Proper use of these two simple, basic properties makes possible rapid, first-order analysis of any operational amplifier circuit, regardless of complexity. Refer to Figure 13, an error voltage at the output of an error amplifier with gain A is

$$E_{out} = A(E_{in_2} - E_{in_1}) \qquad \text{.....(2.19)}$$

or $$E_{in_2} - E_{in_1} = \frac{E_{out}}{A} \qquad \text{.....(2.20)}$$

since A is infinite for ideal operational amplifier, therefore

$$E_{in_2} - E_{in_1} = 0 \qquad \text{.....(2.21)}$$

or $$E_{in_2} = E_{in_1} \qquad \text{.....(2.22)}$$

Equation (2.22) illustrates that an IC operational amplifier with very high gain can make a good comparator.

2.5.1.2 Unity-Gain Buffer : Since the input impedance of an IC operational amplifier used as an error amplifier is not high enough, the unity-gain buffer

which give the high input impedance is used as the front-end circuit. Figure 14 shows schematic diagram of a unity-gain buffer. Input impedance is equal to the differential input impedance multiplied by the open-loop gain, in parallel with common-mode input impedance. The gain accuracy of this circuit is determined by the open-loop gain of the operational amplifier and by its common-mode rejection ratio. The expression for the gain accuracy is

$$\frac{e_o}{e_{in}} = \frac{1 + (1/CMRR)}{1 + (1/A_{oL})} \qquad \text{.....(2.23)}$$

where CMRR = common-mode rejection ratio

A_{oL} = open-loop gain

and the gain error in percentage is

$$\frac{e_o - e_{in}}{e_{in}} = \frac{(1/CMRR)-(1/A_{oL})}{1 + (1/A_{oL})} \times 100 \qquad \text{.....(2.24)}$$

Input bias current for the amplifier will cause an error at the amplifier input because of its voltage drop across the source resistance. In order to minimize this error, R_f should be chosen to be equal to the source resistance, R_s.

2.5.2 Pass Device

Figure 15 shows schematic diagram of a pass device. It comprises a series-pass transistor Q_{14} and driver transistor Q_{13} or Q_{15}. In a series-dissipative regulator, the excess voltage is dissipated in the series-pass transistor. Therefore, the power transistor used as the

series-pass transistor must possess sufficient capabilities in three areas:

a) Adequate current rating : The transistor must be able to carry maximum inverter current.

b) Adequate breakdown voltage rating : The transistor must have collector-emitter breakdown voltage in excess of the supply voltage delivered from dc power supply I.

c) Adequate power rating : The transistor must be able to withstand the maximum power excursions during delivering power to the inverter.

The transistor which is used as a driver must also has the same breakdown voltage rating as the series-pass transistor.

2.5.3 Feedback Network

A resistive divider shown in Figure 16(a) forms a voltage sampling feedback network to stabilize the high voltage output. An equivalent circuit of the feedback network is shown in Figure 16(b). Using Thevenin's theorem, the sampling voltage, $E_{eq.}$ and the sampling source resistance, $R_{eq.}$ are determined in the following expressions:

$$E_{eq.} = \frac{R_{32}}{R_{31}+R_{32}} \times H.V. \qquad \text{.....(2.25)}$$

$$R_{eq.} = R_{31} // R_{32} \qquad \text{.....(2.26)}$$

A modified circuit of the feedback network is shown in Figure 17. Capacitor C_{14} is used to improve the HV output response due to the loading effect. Because of the complexity in analyzing the circuit, proper dimensions of C_{13} in Figure 11 and C_{14} are obtained by "cut and try" method. Potentiometer P_4 is used to protect base-emitter junction of the input transistor of the comparator from overcurrent breakdown. The addition of this series RC network across R_{31} has no effect on dc performance of the feedback circuit.

2.5.4 Internal Reference

A basic internal reference circuit is shown in Figure 18. In order to achieve high stability of the output voltage independent from change in ambient temperature, a temperature compensated reference diode D_5 must be used. This diode is biased by dc power supply II through resistor R_9. A precision three turns potentiometer P_1 is used to alter the output voltage to desired value. Capacitor C_4 is used to eliminate any noise established on the reference diode. An IC operational amplifier is used to invert polarity of reference voltage when negative HV output is required.

2.6 DC POWER SUPPLY I [7],[8]

The schematic diagram of a dc power supply I is shown in Figure 19. This comprises a bridge rectifier D_{12}

and a filter capacitor C_{19} which are used to supply dc voltage from power transformer T_2 to the inverter through the pass device in the regulator. To provide good regulation of the output high voltage, the collector to emitter voltage of the pass device should be at least 3 volts.

2.7 DC POWER SUPPLY II [7], [8]

The schematic diagram of a dc power supply II is shown in Figure 20. This is used to supply the dc regulated voltage from the power transformer T_2 to the control circuit in the regulator and the protection circuit. The circuit comprises a bride rectifier, two filter capacitors, an IC positive voltage regulator and a discrete negative voltage regulator which together form a tracking regulated power supply. Owing to its tracking ability of positive and negative voltage outputs, thus common-mode signals originating in the supply voltage is eliminated. Therefore this supply is very suitable for powering the IC operational amplifier in the regulator and the protection circuit.

The following expressions are used to calculate the values of the resistors used in the circuit.

(1) For IC voltage regulator

$$V_{o_{pos}} = V_{ref} \times \frac{R_1 + R_2}{R_2} \qquad \text{.....(2.27)}$$

$$R_3 = R_1 // R_2 \qquad \text{.....(2.28)}$$

where V_{ref} = reference voltage of IC regulator pack

$V_{o_{pos}}$ = regulated output voltage

(2) For discrete voltage regulator

$$V_{o_{neg}} = -\left[V_{o_{pos}} \times \frac{R_4 + R_5}{R_4}\right] + V_{o_{pos}} \quad \text{.....(2.29)}$$

or

$$V_{o_{neg}} = -V_{o_{pos}} \left[\frac{R_5}{R_4}\right] \quad \text{.....(2.30)}$$

2.8 DC POWER SUPPLY III [7], [8]

An IC voltage regulator, a bridge rectifier, and a capacitor filter form dc power supply III to supply dc voltage from power transformer T_2 to the oscillator. Since the supply is well regulated, the frequency of the oscillator is stable. The schematic diagram of the supply is shown in Figure 21. The expressions used to calculate the value of resistors in the circuit are shown in section 2.6

2.9 PROTECTION CIRCUIT [7], [8]

A schematic diagram of the protection circuit is shown in Figure 22. This circuit is used to protect the output of the HV power supply from damage caused by output short-circuiting as well as over loading. The voltage which is developed across resistor R_{33} by the output current is sampled through the amplifier IC7 and compared with the reference voltage at the comparator IC6. If the output of the HV supply is short-circuited or overloaded, SCR_1 will be trigged to the conduction mode and the output voltage of the internal reference will become less than zero. This brings the regulator to shutdown and no more voltage is produced

at the output of the HV supply. A reset button is used to re-start the operation of the HV supply after the short-circuit or overload action is removed. The derivative expression of the protection circuit is as follows:

If V_Z = reference voltage at the comparator IC6

I_{Lm} = output limit current of the HV supply

R_{33} = the sensing resistance

A_f = feedback gain of the operational amplifier IC7

$$A_f = \frac{R_{36}}{R_{34}} \qquad \text{.....(2.31)}$$

$$A_f I_{Lm} R_{33} = V_Z \qquad \text{.....(2.32)}$$