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5.8.2 Presentation Format

A description of each 5500 instruction is given below. In order to simplify the presentation, the following symbols and abbreviations are used:

Operation:	Symbolic representation of instruction description.
Op Code:	Operation Code, expressed in octal.
Timing:	Execution time in microseconds. (Note: memory refresh overhead is 5% implying that a program will execute, on the average, 5% slower than the sum of the indicated tim ings.)
Length:	Number of bytes in the instruction. (Used when the ler gth may not be especially obvious from the op code or the instruction diagram.)
Stack:	Number of stack entries.
Entry:	Conditions necessary before execution.
Exit:	Conditions existing after execution.
Algorithm:	Steps taken to perform the instruction execution.
( )	The contents of.
←	Is replaced by
→	Is transferred to.
:	Is compared with.
V	Logical "Or" operation.
⊻	Logical "Exclusive Or" operation
∧	Logical "AND" operation.
A, B, C, D, E, H, L, X	8-bit processor registers
M	Memory location designated by the contents of HL or the designated register pair.
P	Program counter. (When shown P+X location relative to first byte of instruction).
Stack	Pushdown Stack
(OP)	One of the eight ALU operations (AD, AC, SU, SB ND, XR, OR, CP)
(rs)	A source general register (ABCDEHL)(s=0 to 6).
(rd)	A destination general register (ABCDEHL) (d=0 to 6).
(r)	A general register (ABCDEHLX). (s or d =0 to 7)
(rp)	One of the pairs of registers (BC DE HL XA)
r	A register select op code. No byte is necessary for selection of the A register. Otherwise: B=0111, C=062, D=0113, E=0174, H=0115 L=0176, X=022
rp	A register pair select op code. No byte is necessary for the selection of HL. Otherwise: BC=062, DE= 0174, XA=022.
(vvv)	An 8-bit value used in an instruction.
(adr)	A 16-bit value used in an instruction with the LSP first, followed by the MSP.
(cf)	Control flags (CZSP) (c=0 to 3) (Often called flip-flops).
(exp)	External command, listed in Table 5-1.
data	An expression reducing to an 8-bit immediate value.
loc	An expression reducing to a 16-bit address.

5.8.3 Category 1 — 2200 System Instructions

LOAD IMMEDIATE **L (r)**

Op Code: 0d6 (vvv)
Timing: 1.8
Operation: (vvv)→(r)

Transfers the contents of the operand given in the instruction to the register specified by bits 3-5 of the instruction word.

7 6	5 4 3	2 1 0	7 0
0	d	6	OPERAND

1. d is the destination designator.
2. None of the flag flip-flops are changed.

LOAD **L(rd)M, L(rd)(rs), LM(rs)**

For L(rd)M: Op Code: 3d7
Timing: 2.6
Operation: (M)→(rd) d≤6
For L(rd)(rs): Op Code: 3ds
Timing: 1.2
Operation: (rs)→(rd) s≤6, d≤6
For LM(rs): Op Code: 37s
Timing:2.6
Operation: (rs)→(M) s≤6

Transfers the operand from the source specified by bits 0-2 of the instruction word to the destination specified by bits 3-5 of the instruction word.

7 6	5 4 3	2 1 0
3	d	s

1. The data source is unaffected.
2. s and d both = 7 results in a HALT instruction.
3. None of the flag flip-flops are changed.

ADD IMMEDIATE **AD data**

Op Code: 004 (vvv)
Timing: 2.2
Operation: (A) + (P+1)→A

Adds the value of the (data) operand to the contents of the A register and retains the sum in the A register.

7 6	5 4 3	2 1 0	7 0
0	0	4	OPERAND

1. Carry flip-flop set if add overflow occurs; otherwise carry is reset.
2. The Sign, Zero and Parity flip-flops indicate the status of the A register at completion.

ADD **AD(rs), ADM**

For AD(rs): Op Code: 20s
Timing: 1.4
Operation: (A) + (rs)→A
For ADM: Op Code: 207
Timing: 2.6
Operation: (A) + (M)→A

This instruction is identical to ADD IMMEDIATE with the exception of operand source.

7 6	5 4 3	2 1 0
2	0	s

s specifies the operand source.

ADD WITH CARRY IMMEDIATE **AC data**

Op Code: 014 (vvv)
Timing: 2.2
Operation: (A) + (P+1) + (Carry)→A

Adds the Carry bit and contents of the operand to the contents of the A register and retains the sum in the A register.

7 6	5 4 3	2 1 0	7 0
0	1	4	OPERAND

1. If add overflow occurs, the Carry flip-flop is set; otherwise Carry is reset.
2. The Sign, Zero and Parity flip-flops indicate the status of the A register at completion.

ADD WITH CARRY **AC(rs), ACM**

For AC(rs): Op Code: 21s
Timing: 1.4
Operation: (A) + (Carry) + (rs)→A
For ACM: Op Code: 217
Timing: 2.6
Operation: (A) + (Carry) + (M)→A

This instruction is identical to ADD WITH CARRY IMMEDIATE with the exception of operand source.

7 6	5 4 3	2 1 0
2	1	s

s specifies the operand source.

SUBTRACT IMMEDIATE **SU data**

Op Code: 024 (vvv)
Timing: 2.0
Operation: (A) - (P+1) → A

Subtracts the value of the operand from the contents in the A register and retains the difference in the A register.

7 6	5 4 3	2 1 0	7 0
0	2	4	OPERAND

1. The Carry flip-flop is set if underflow occurs, otherwise carry is reset.
2. The Zero, Sign and Parity flip-flops represent the status of the A register at completion.

SUBTRACT **SU(rs), SUM**

For SU(rs): Op Code: 22s
Timing: 1.4
Operation: (A)-(rs)→A
For SUM: Op Code: 227
Timing: 2.6
Operation: (A)-(M)→A

This instruction is identical to SUBTRACT IMMEDIATE with the exception of operand source.

7 6	5 4 3	2 1 0
2	2	s

s specifies the operand source.

SUBTRACT WITH BORROW IMMEDIATE **SB data**

Op Code: 034 (vvv)
Timing: 2.2
Operation: (A)-(P+1) - (Carry)→A

Subtracts the value of the operand and the Carry bit from the contents of the A register, and retains the difference in the A register.

7 6	5 4 3	2 1 0	7 0
0	3	4	OPERAND

1. Sets the Carry flip-flop if underflow occurs; otherwise resets Carry.
2. The Zero, Sign, and Parity flip-flops represent the status of the A register at completion.

SUBTRACT WITH BORROW **SB(rs), SBM**

For SB(rs): Op Code: 23s
Timing: 1.4
Operation: (A)-(rs)-(Carry)→A
For SBM: Op Code: 237
Timing: 2.6
Operation: (A)-(M) - (Carry)→A

This instruction is identical to SUBTRACT WITH BORROW IMMEDIATE with the exception of the operand source.

7 6	5 4 3	2 1 0
2	3	s

s specifies the operand source.

AND IMMEDIATE **ND data**

Op Code: 044 (vvv)
Timing: 2.2
Operation: (A) $\wedge$ (P+1) $\rightarrow$ A

Forms the logical product of the contents of the A register with the value of the operand and places the result in the A register.

7 6	5 4 3	2 1 0	7 0
0	4	4	OPERAND

1. Resets the Carry flip-flop upon completion.
2. The Zero, Sign and Parity flip flops represent the status of the A register upon completion.

Sample Operation:

(A Reg)	0	0	0	0	1	1	1	1
(P+1)	0	1	1	0	0	1	1	0
(A Reg)	0	0	0	0	0	1	1	0

AND **ND(rs), NDM**

For ND(rs): Op Code: 24s
Timing: 1.4
Operation: (A) $\wedge$ (rs) $\rightarrow$ A
For NDM: Op Code: 247
Timing: 2.6
Operation: (A) $\wedge$ (M) $\rightarrow$ A

This instruction is identical to AND IMMEDIATE with the exception of operand source.

7 6	5 4 3	2 1 0
2	4	s

s specifies the operand source.

OR IMMEDIATE **OR data**

Op Code: 064 (vvv)
Timing: 2.0
Operation: (A) V (P+1) $\rightarrow$ A

Forms the logical sum of the contents of the A Register and the value of the operand, and places the result in the A register.

7 6	5 4 3	2 1 0	7 0
0	6	4	OPERAND

1. Resets the Carry flip-flop upon completion.
2. The Zero, Sign and Parity flip-flops represent the status of the A register upon completion.

Sample Operation:

(A Reg)	0	0	0	0	1	1	1	1
(P+1)	0	1	1	0	0	1	1	0
(A Reg)	0	1	1	0	1	1	1	1

OR **OR(rs),ORM**

For OR(rs): Op Code: 26s
Timing: 1.4
Operation: (A) V (rs) $\rightarrow$ A
For ORM: Op Code: 267
Timing: 2.6
Operation: (A) V (M) $\rightarrow$ A

This instruction is identical to OR IMMEDIATE with the exception of operand source.

7 6	5 4 3	2 1 0
2	6	s

s specifies operand source.

EXCLUSIVE OR IMMEDIATE **XR data**

Op Code: 054 (vvv)
Timing: 2.0
Operation: (A) $\forall$ (P+1) $\rightarrow$ A

Forms the logical difference of the contents of the A register and the value of the operand, and places the result in the A register.

7 6	5 4 3	2 1 0	7 0
0	5	4	OPERAND

1. Resets the Carry flip-flop at completion.
2. The Zero, Sign and Parity flip-flops represent the status of the A register upon completion.

Sample operation:

(A Reg)	0	0	1	1	0	1	0	1
(P+1)	0	1	0	1	1	1	0	0
(A Reg)	0	1	1	0	1	0	0	1

EXCLUSIVE OR **XR(rs), XRM**

For XR(rs): Op Code: 25s
Timing: 1.4
Operation: (A) $\forall$ (rs) $\rightarrow$ A
For XRM: Op Code: 257
Timing: 2.6
Operation: (A) $\forall$ (M) $\rightarrow$ A

This instruction is identical to EXCLUSIVE OR IMMEDIATE with the exception of operand source.

7 6	5 4 3	2 1 0
2	5	s

s specifies the operand source.

COMPARE IMMEDIATE **CP data**

Op Code: 074 (vvv)
Timing: 1.8
Operation: (A) : (P+1)

Compares the contents of the A register with the value of the operand.

7 6	5 4 3	2 1 0	7 0
0	7	4	OPERAND

1. The flag flip-flops assume the same state as they would for a Subtract instruction.
2. The contents of the A register are unaffected.

COMPARE **CP(rs), CPM**

For CP(rs): Op Code: 27s
Timing: 1.2
Operation: (A):(rs)
For CPM: Op Code: 277
Timing: 2.4
Operation: (A):(M)

This instruction is identical to COMPARE IMMEDIATE with the exception of operand source.

7 6	5 4 3	2 1 0
2	7	s

s specifies the operand sources

UNCONDITIONAL JUMP **JMP loc**

Op Code: 104 (adr)
Timing:2.8
Operation: (adr) ⟶ P

An unconditional transfer of control. The second byte of the instruction represents the least significant portion of the jump address, while the third byte of the instruction represents the most significant portion.

			P+1	P+2
7 6	5 4 3	2 1 0	7 0	7 0
1	0	4	LSP	MSP
	Op Code		Address	

JUMP IF CONDITION TRUE **JT(cf) loc**

Op Code: 1(c+4) 0 (adr)
Timing: 2.8 if condition true
1.4 if condition false
Operation: If condition true, (adr) ⟶ P

Examines the designated flip-flop. If set, transfers control to (adr). If reset, executes the next sequentially available instruction.

			P+1	P+2
7 6	5 4 3	2 1 0	7 0	7 0
1	c+4	0	LSP	MSP
	Op Code		Address	

1. c designates which flip-flop (condition) is to be tested.
2. The condition of the selected flip-flop is unchanged by this instruction.

JUMP IF CONDITION FALSE **JF(cf) loc**

Op Code: 1c0 (adr)
Timing: 2.8 if condition false
1.4 if condition true
Operation: if condition false, (adr) ⟶ P

Examines the designated flip-flop. If reset, transfers control to (adr). If set, executes the next sequentially available instruction.

			P+1	P+2
7 6	5 4 3	2 1 0	7 0	7 0
1	c	0	LSP	MSP
	Op Code		Address	

1. c designates which flip-flop (condition) is to be tested.
2. The condition of the selected flip-flop is unchanged by this instruction.

SUBROUTINE CALL **CALL loc**

Op Code: 106 (adr)
Timing: 2.8
Operation: P+3⟶ Stack, (adr) ⟶P

Transfers the address of the next sequentially available instruction to the pushdown Stack, and transfers control to the address specified by the contents of the two memory locations immediately following the Op Code.

			P+1	P+2
7 6	5 4 3	2 1 0	7 0	7 0
1	0	6	LSP	MSP
	Op Code		Address	

The Stack is open-ended in operation. If it is overfilled, the deepest address will be lost.

SUBROUTINE CALL IF CONDITION TRUE **CT(cf) loc**

Op Code: 1(c+4)2 (adr)
Timing: 3.2 if condition true
1.6 if condition false
Operation: If condition true, P+3⟶ Stack, (adr) ⟶ P

Examines the designated flip-flop. If set, transfers the address of the next sequentially available instruction to the pushdown Stack, and transfers control to (adr). If reset, executes the next sequentially available instruction.

			P+1	P+2
7 6	5 4 3	2 1 0	7 0	7 0
1	4	2	LSP	MSP
	Op Code		Address	

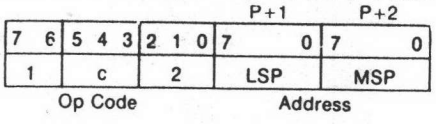
1. c designates which flip-flop (condition) is to be tested.
2. The condition of the selected flip-flop is unchanged by this instruction.
3. The Stack is open-ended in operation. If it is overfilled, the deepest address will be lost.

SUBROUTINE CALL IF CONDITION FALSE **CF(cf) loc**

Op Code: 1c2 (adr)
Timing: 3.2 if condition false
1.6 if condition true
Operation: If condition false, P+3⟶ Stack, (adr) ⟶ P

Examines the designated flip-flop. If reset, transfers the ad-

dress of the next sequentially available instruction to the pushdown Stack, and transfers control to (adr). If set, executes the next sequentially available instruction.

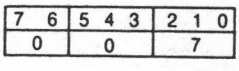


1. c designates which flip-flop (condition) is to be tested.
2. The condition of the selected flip-flop is unchanged by this instruction.
3. The Stack is open-ended in operation. If it is overfilled, the deepest address will be lost.

SUBROUTINE RETURN **RET**

Op Code: 007
Timing: 1.8
Operation: (Stack) ⟶ P

Transfers control to the address specified by the most recent entry into the pushdown Stack. Deletes the most recent entry from the Stack.

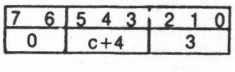


The effect of attempting more RETURN instructions than the Stack is capable of handling is undefined.

SUBROUTINE RETURN IF CONDITION TRUE RT(cf)

Op Code: 0 (c+4) 3
Timing: 2.0 if condition true
1.0 if condition false
Operation: If condition true, (Stack) ⟶ P.

Examines the designated flip-flop. If set, transfers control to the address specified by the most recent entry into the pushdown Stack and deletes the most recent entry into the Stack. If reset, executes the next sequentially available instruction.

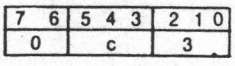


1. c designates which flip-flop (condition) is to be tested.
2. The condition of the selected flip-flop is unchanged by this instruction.
3. The effect of attempting more RETURN instructions than the Stack is capable of handling is undefined.

SUBROUTINE RETURN IF CONDITION FALSE RF(cf)

Op Code: 0c3
Timing: 2.0 if condition false
1.0 if condition true
Operation: If condition false, (Stack) ⟶ P

Examines the designated flip-flop. If reset, transfers control to the address specified by the most recent entry into the pushdown Stack and deletes the most recent entry into the Stack. If set, executes the next sequentially available instruction.

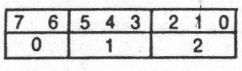


1. c designates which flip-flop (condition) is to be tested.
2. The condition of the selected flip-flop is unchanged by this instruction.
3. The effect of attempting more RETURN instructions than the Stack is capable of handling is undefined.

SHIFT RIGHT CIRCULAR **SRC**

Op Code: 012
Timing: 1.4
Operation: $A_{(N)} \longrightarrow A_{(N-1)}$, A0 ⟶ A7, A0 ⟶ Carry

Shifts the contents of the A register right in a circular fashion. Shifts the least significant bit into the most significant bit position. Upon completion of the operation, the Carry flip-flop is equal to the most significant bit.

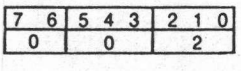


The Zero, Parity and Sign flip-flops are not affected by this instruction.

SHIFT LEFT CIRCULAR **SLC**

Op Code: 002
Timing: 1.4
Operation: $A_{(N-1)} \longrightarrow A_{(N)}$, A7 ⟶ A0 A7 ⟶ Carry

Shifts the contents of the A register left in a circular fashion. Shifts the most significant bit into the least significant bit position. Upon completion of the operation, the Carry flip-flop is equal to the least significant bit.

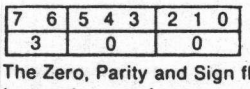


The Zero, Parity and Sign flip-flops are not affected by this instruction.

NO OPERATION **NOP**

Op Code: 300
Timing: 1.2
Operation: P+1 ⟶ P

No operation is performed



The Zero, Parity and Sign flip-flops are not affected by this instruction.

HALT **HALT**

Op Code: 000, 001, or 377
Timing: Execution stops
Operation: The processor halts

When the START button on the console is depressed, operation resumes at P+1.

If USER mode is set this instruction will cause a privileged instruction interrupt to occur.

POP **POP**

Op Code: 060
Timing: 2.2
Operation: (Stack)⟶H,L

Transfers the most recent Stack entry into the H & L registers. H=MSP, L=LSP.

7 6	5 4 3	2 1 0
0	6	0

PUSH **PUSH**

Op Code: 070
Timing: 1.8
Operation: H,L⟶Stack

Transfers the contents of the H & L registers into the pushdown Stack. H=MSP, L=LSP.

7 6	5 4 3	2 1 0
0	7	0

INPUT **INPUT**

Op Code: 101
Timing: 5.0
Operation: (I/O Bus)⟶A

Transfers the contents of the I/O Bus to the A register.

7 6	5 4 3	2 1 0
1	0	1

Priv. Note: If USER mode is set, this instruction will cause a privileged instruction interrupt to occur.

ENABLE INTERRUPTS **EI**

Op Code: 050
Timing: 1.4

Following the next instruction, EI will allow the interrupts to occur until a DISABLE INTERRUPT instruction is executed.

7 6	5 4 3	2 1 0
0	5	0

Priv. Note: If USER mode is set, this instruction will cause a privileged instruction interrupt to occur.

DISABLE INTERRUPTS **DI**

Op Code: 040
Timing: 1.4

Prevents interrupts from occurring until an ENABLE INTERRUPT instruction is executed.

7 6	5 4 3	2 1 0
0	4	0

Priv. Note: If USER mode is set, this instruction will cause a privileged instruction interrupt to occur.

SELECT ALPHA MODE **ALPHA**

Op Code: 030
Timing: 1.4

Selects the ALPHA MODE registers and control flip-flops.

7 6	5 4 3	2 1 0
0	3	0

Priv. Note: If USER mode is set, this instruction will cause a privileged instruction interrupt to occur.

SELECT BETA MODE **BETA**

Op Code: 020
Timing: 1.4

Selects the BETA MODE registers and control flip-flops.

7 6	5 4 3	2 1 0
0	2	0

Priv. Note: If USER mode is set, this instruction will cause a privileged instruction interrupt to occur.

EXTERNAL COMMAND **EX (exp)**

Op Code: 121 to 153
Timing: 9.2
Operation: Performs I/O control according to (exp)

These instructions perform the functions necessary for control of the I/O System and external devices. Many of these functions are specifically related to operation of particular devices. The device oriented commands for the Keyboard, CRT Display, and diskette drives are explained in the sections covering these devices.

7 6	5 4 3	2 1 0
0 1	x x x	x x 1

Priv. Note: If USER mode is set, this instruction will cause a privileged instruction interrupt to occur.

Table 5-1 is a list of the External Commands. For a detailed discussion of their use, reference should be made to Part 6 (Input/Output Operations) and to descriptions of the separate external devices. External Commands 155-177 are not listed, as they apply to systems with integral cassette units and are described in Part 4 (Cassette Tapes).

TABLE 5-1
EXTERNAL COMMANDS

EX (exp)

(exp)	OCTAL CODE	COMMAND	DESCRIPTION	DEVICE ADDRESS
ADR	121	Address	Selects device specified by A register	ALL
STATUS	123	Sense Status	Connects selected device status to input lines	
DATA	125	Sense Data	Connects selected device data to input lines	
WRITE	127	Write Strobe	Signals selected device that output data word is on output lines	
COM1	131	Command 1	Outputs a control function to selected device	
COM2	133	Command 2	Outputs a control function to selected device	
COM3	135	Command 3	Outputs a control function to selected device	
COM4	137	Command 4	Outputs a control function to selected device	ALL
—	141	(Unassigned)	—	-
—	143	(Unassigned)	—	-
—	145	(Unassigned)	—	-
—	147	(Unassigned)	—	-
BEEP	151	Beep	Activates tone producing mechanism	ALL
CLICK	153	Click	Activates audible click producing mechanism	ALL

5.8.4 Category 2 — Augmented Category 1 Instructions

LOAD REGISTER FROM MEMORY USING BC, DE, OR XA FOR THE ADDRESS **L(rd)M (rp)**

Op Code: rp 3d7
Timing: 3.4
Operation: (M) ⟶ (rp), d ≤ 7
Length: 2 bytes
Example: LEM BC

Identical to the L(rd)M instruction et that the specified register pair, instead of HL, is used for the memory address.

LOAD MEMORY FROM REGISTER USING BC, DE, OR XA FOR THE ADDRESS **LM(rs) (rp)**

Op Code: rp 37s
Timing: 3.4
Operation: (rs) ⟶ M, s ≤ 6
Length: 2 bytes
Example: LMB DE

Identical to the LM(rd) instruction except that the specified register pair, instead of HL, is used for the memory address.

ARITHMETIC AND LOGICAL OPERATIONS TO OTHER THAN THE A REGISTER

Mnemonics:	Examples:
(op)(rs) (r)	ADAB adds A to B
(op)M (r)	ADMC adds (HL) to C
(op)(r) (vvv)	SUC 20 subtracts 20 from C
SRC (r)	SRCB shifts B right
SLC (r)	SLCD shifts D left

Op Codes: r 2ps, r 0p7, r 0p4, r 012, r 002
Timing: Add 1.0 to equivalent category 1 instruction timing.
Length: Add 1 byte to the equivalent category 1 instruction

Identical to the equivalent category 1 arithmetic operations except that the specified register, instead of the A register is used.

SHIFT RIGHT EXTENDED **SRE, SRE(r)**

For SRE:
Op Code: 032
Timing: 1.4
Operation: $A_N \longrightarrow A_{(N-1)}$ Carry $\longrightarrow A_7$ $A_\phi \longrightarrow$ Carry
Length: 1 byte

For SRE(r): Op Code: r 032
Timing: 2.4
Operation: $(r)_N \longrightarrow (r)_{(N-1)}$ Carry $\longrightarrow (r)_7$, $(r)_0 \longrightarrow$ Carry
Length: 2 bytes

The register is shifted right one place with the left hand bit being replaced by the Carry and the Carry being replaced by the right-hand bit.

I/O USING OTHER THAN THE A REGISTER **IN(r), EX(rs) (•exp)**

For IN(r): Op Code: r 101
Timing: 6.0
Operation: (I/O Bus) $\longrightarrow$ (r)
Length: 2 bytes
For EX (rs) (exp): Op Code: r 121, r 123, etc.
Timing: 10.2
Operation: Performs I/O control with specified register according to (exp)
Length: 2 bytes

Identical to the 2200 I/O operations except that the specified register, instead of the A register, is used.
Priv. Note: If USER mode is set, this instruction will cause a privileged instruction interrupt to occur.

PARITY CHECKING INPUT **PIN, PIN(r)**

For PIN: Op Code: 103
Timing: 5.4
Length: 1 byte
For PIN (r): Op Code: r 103
Timing: 6.4
Length: 2 bytes

Identical to the INPUT instruction except that if the nine bits of the I/O Bus contain an even number of ones, an interrupt will occur.
Priv. Note: If USER mode is set, this instruction will cause a privileged instruction interrupt to occur.

PUSH USING BC, DE, OR XA **PUSH (rp)**

Op Code: rp 070
Timing: 2.6
Operation: (rp) $\longrightarrow$ Stack
Length: 2 bytes

Pushes the specified register pair onto the Stack.

PUSH IMMEDIATE **PUSH loc**

Op Code: 051 (adr)
Timing: 2.6
Operation: (adr) $\longrightarrow$ Stack
Length: 3 bytes

Pushes the contents of the operand onto the Stack.

POP USING BC, DE, OR XA **POP(rp)**

Op Code: rp 060
Timing: 3.0 usec.
Operation: (Stack) $\longrightarrow$ (rp)
Length: 2 bytes

Pops the Stack into the specified register pair.

5.8.5 Category 3 — Multi-byte (string) Operations

BLOCK TRANSFER OR BLOCK TRANSFER REVERSE **BT, BTR**

For BT: Op Code: 021
Timing: 4.8+N•3.2
+(N•0.2) if B≠0
—(0.8) if end check succeeds
N=number of steps done
Length: 1 byte
For BTR: Op Code: 111 021
Timing: 5.8+N•3.6
+(N•0.2) if B≠0
—(0.8) if end check succeeds.
N=number of steps done.
Length: 2 bytes

The Block Transfer instructions move the number of bytes specified in the C register from the field pointed to by HL to the field pointed to by DE while adding the contents of the A register to each byte transferred. BT causes the pointers to be incremented after each transfer while BTR causes the pointers to be decremented after each transfer. If the B register is not zero, the transfer will stop if a character which is equal to the 2's complement of the B register is stored in the destination field (stops after the matching character is moved).

Entry: HL=location of first source byte.
DE=location of first destination byte.
C=number of bytes to move (C=1 to 255; 0 for 256).
B=2's complement of terminating character if not 0.
A=8-bit value added to each byte as it is moved (for de-zoning and zoning decimal numbers).

Exit: HL=location past last source byte.
DE=location past last destination byte.
A=entry value.
B=entry value.
C=zero or count before terminator character found.
Condition flags are all altered.

Stack: 2 entries used.

Caution: Since BT and BTR instructions can take up to 820 microseconds to execute, care must be exercised in their use if time critical interrupt driven programs are to be simultaneously executed.

BLOCK CONVERT **BCV**

Op Code: 062 021
Timing: 5.8+N•4.8
+(N•0.2) if B=0
—(0.8) if end check succeeds.
N=number of steps done
Length: 2 bytes

BLOCK CONVERT is a variation of BLOCK TRANSFER where the field pointed to by the DE registers is translated byte-by-byte using the translate table pointed to by the HL register pair.

Entry: HL=location of the translate table (must not cross a page boundary).
DE=location of the first byte to be translated.
C=number of bytes to move
B=2's complement of terminating character if not 0.
A=no entry value used.

Exit: HL=undefined
DE=location past last destination byte
A=LSB of last table position used for translation.
B=entry value.
C=zero or count before termination character found.

Algorithm:
1. Get the byte pointed to by DE.
2. Set A to the result of the byte added to L.
3. Get the byte pointed to by HA. This is the table's translated byte.
4. Store the translated byte where DE points
5. Increment DE.
6. B is added to the translated byte.
7. Stop if the Carry and Zero conditions are true — a match is found.
8. Decrement the C register.
9. Go to Step 1 if result is non-zero.

Stack: 2 entries used

Caution: Since BCV instructions can take over 820 microseconds to execute, care must be taken in their use if time critical interrupt driven programs are to be simultaneously executed.

BINARY FIELD ADD WITH CARRY OR SUBTRACT WITH BORROW **BFAC, BFSB**

For BFAC: Op Code: 011
Timing: 5.0 + C•2.8
Length: 1 byte

For BFSB: Op Code: 031
Timing: 5.0 + C•2.8
Length: 1 byte

These instructions take the field pointed to by HL and either add it to or subtract it from the field pointed to by DE, leaving the result in the field pointed by DE. The fields may be 1 through 16 bytes in length.

Entry: HL=location of right hand byte of the operand field.
DE=location of right hand byte of the accumulator field
C=the field width (1 through 16; 0 or 16 implies 16).
Carry=carry or borrow into the operation.

Exit: HL=location to left of the left hand byte of the operand field.
DE=location to left of the left hand byte of the Accumulator field.
C=indeterminate.
Carry=carry or borrow out of the operation (all the condition flags are altered).

Algorithm:
1. Load the implicit register from C.
2. Get the byte pointed to by HL.
3. Add it with carry or subtract it with borrow from the byte pointed to by DE and store the result where DE points.
4. Decrement HL and DE by one.
5. Decrement the implicit register by one.
6. Go to step 2 if the implicit register is not now zero.

Stack: 2 entries used

BLOCK COMPARE **BCP**

Op Code: 041
Timing: 5.2 + N•2.6
—(0.8) if mismatch found.
N=number if steps done.
Length: 1 byte

This instruction matches two strings of bytes from left to right until either a mismatch is found or the specified maximum number of bytes have been scanned.

Entry: HL=location of left hand byte of the subtracting field.
DE=location of left hand byte of the subtracted from field.
C=the maximum number of bytes to scan (1 thru 255; 0 implies 256).

Exit: IF A MISMATCH WAS FOUND:
HL=location after the last byte examined in the subtracting field
DE=location after the last byte examined in the subtracted from field.
C=entry value minus number of bytes that matched
Condition flags all reflect the result of the subtract instruction that found the two bytes differing.
IF ALL BYTES MATCHED
HL=location after the last byte in the subtracting field
DE=location after the last byte in the subtracted from field
C=zero
Condition flags are all altered. (Zero condition being set true)

Algorithm:
1. Get the byte pointed to by HL.
2. Subtract it from the byte pointed to by DE.
3. Increment DE and HL.

4. Exit if the Zero condition is false.
5. Decrement C.
6. Go to Step 1 if C is not equal to zero.
7. Exit with the Zero condition true.

Stack: 2 entries used.

Caution: BCP can take up to 722 microseconds to execute.

DECIMAL FIELD ADD WITH CARRY **DFAC**

Op Code: 111 041
Timing: 6.4 + C•4.4 If a carry occurred on every digit, +(K•0.2) is if no carries occurred (K is number of carry outs).
Length: 2 bytes.

This instruction takes the field of zoned BCD digits pointed to by HL and adds it to the field of zoned BCD digits pointed to by DE, leaving the result in the field pointed to by DE. The zone bits of the result field are set to the zone bits in the B register. The fields may be 1 through 16 bytes in length.

Entry: Same as for the BFAC instruction except B=output zoning (right 4 bits must be 0; left 4 bits must be other than 0000).
Exit: Same as for the BFAC instruction except A register is destroyed. B=entry value.
Algorithm:
1. Load the implicit register from C.
2. Get the byte pointed to by HL.
3. Add it with carry to the byte pointed to by DE.
4. Strip away the zone bits.
5. Clear the Carry and go to step 7 if the result is less than 10.
6. Subtract 10 from the result and set the Carry.
7. Set the zoning bits.
8. Store the result where DE points.
9. Decrement HL and DE by one.
10. Decrement the implicit register by one.
11. Go to step 2 if the implicit register is not zero.

NOTE: The binary values for the zoned BCD digits with xxxx not equal to 0000 are as follows (the digits are not packed, i.e., only one digit per byte):

0:xxxx0000	5:xxxx0101
1:xxxx0001	6:xxxx0110
2:xxxx0010	7:xxxx0111
3:xxxx0011	8:xxxx1000
4:xxxx0100	9:xxxx1001

D
DECIMAL FIELD SUBTRACT WITH BORROW **BFSB**

Op Code: 062 041
Timing: 6.4+ C•3.6 if a borrow occurred on every digit; +(K•0.4) for each borrow that occurred (K is number of carry outs).
Length: 1 byte

This instruction takes the field of zoned BCD digits pointed to by HL and substracts it from the field of zoned BCD digits pointed to be DE, leaving the result in the field pointed to by DE. The zone bits of the two fields must be identical. The zone bits of the result field are set to the zone bits in the B register. The fields may be 1 through 16 bytes in length.

Entry: same as for the DFAC instruction.
Exit: same as for the DFAC instruction.
Algorithm:
1. Load the implicit register from C.
2. Get the byte pointed to by HL.
3. Subtract it, with borrow, from the byte pointed to by DE.
4. Go to Step 6 and clear the Carry if the byte result is not negative.
5. Add 10 to the result and set the Carry.
6. Set the zone bits to those in the B register.
7. Store the result where DE points.
8. Decrement HL and DE by one.
9. Decrement the implicit register by one.
10. Go to Step 2 if the implicit register is not zero.

Stack: 2 entries used.

BINARY FIELD SHIFT LEFT **BFSL**

Op Code: 075
Timing: 3.8+C•2.2
Length: 1 byte

This instruction shifts a field of bytes in memory left one bit position as if all of the bytes made up one continuous word.

Entry: HL=location of right-hand byte of the field.
C=the field width (1 through 16; 0 or 16 implies 16).
Carry=bit shifted out on the left
Exit: HL=location left of the left-hand byte of the field.
C=indeterminate.
A=indeterminate.
Carry=bit shifted out on the left.
All other flags are indeterminate.
Stack: 2 entries used.

BINARY FIELD SHIFT RIGHT **BFSR**

Op Code: 111 075
Timing: 4.6 + C • 2.0
Length: 2 bytes

This instruction is similar to BFSL except the shift is in the opposite direction.

Entry: HL=location of left-hand byte of the field.
C=the field width (1 through 16; 0 or 16 implies 16)
Carry=bit shifted in on left.
Exit: HL=location right of the right-hand byte of the field.
C=indeterminate.
A=indeterminate.
Carry=bit shifted out on the right.
All other flags are indeterminate.
Stack: 2 entries used.

MULTIPLE INPUT **MIN**

Op Code: 111 061
Timing: 3.0 + 8.4 per byte transferred
Length: 2 bytes

This instruction moves the number of bytes specified in the C register from a buffered input device to the field pointed to by L. The number of bytes moved is the number in the C register modulo 16. To make transferring up to 256 bytes easy yet interruptable, the full eight bit value of the C register is retained during loop counting and exit is made with the C register containing its entry value minus the number of bytes transferred, HL containing its entry value plus the number of bytes transferred, and the Zero condition code reflecting the eight bit result of the last decrementation of the C register. Thus the interruptable loop for transferring the number of bytes indicated by the eight bit value in the C register yet not inhibiting interrupts more than 155 microseconds would appear as follows:

```
LOOP    LA      DEVADR
        DI
        EX      ADR
        EX      DATA
        EI
        MIN
        JFZ     LOOP
```

Note that the device must be re-addressed for each execution of the MIN instruction if an interrupt could cause some other device to be addressed. The MIN instruction causes a parity checking input strobe to be executed every 8.4 microseconds. This execution operates without regard to any status bits of any kind. There is no existing 2200 system I/O device capable of using this instruction and it is included for use with 5500 system I/O devices with parity generation and faster buffers allowing them to be used as data rates equivalent to DMA channels. The MIN instruction has all of the advantages of a non-I/O device interrupting system (lower software overhead in high throughput situations, superior control over the occurrence of events allowing probability of correctness in the program logic and repeatability of event occurrence, and simpler hardware using lower speeds and noise filtered buses) and yet achieves DMA throughput rates.

Priv. Note: If USER mode is set, this instruction will cause a privileged instruction interrupt to occur.

Entry: HL=location of first destination byte
C=number of bytes to move (this number is taken modulo 16 and if it is 0 modulo 16 then 16 bytes will be moved).

Exit: HL=location of entry value plus number of bytes moved
C=entry value minus number of bytes moved

Algorithm:
1. Execute a parity checking INPUT.
2. Store the byte where HL points.
3. Increment HL.
4. Load the implicit register from C.
5. Decrement C using the ALU.
6. Decrement the implicit register.
7. Exit if the implicit register is zero.
8. Decrement the P-counter.
9. Re-fetch the instruction without allowing interrupts.

Stack: 1 entry used.

NOTE: To input a block of 256 bytes using the loop described above would take 2550 microseconds if no interrupts occurred (an average of 10 microseconds per byte).

MULTIPLE OUTPUT **MOUT**

Op Code: 111 071
Timing: 3.0 + 8.8 per byte transferred
Length: 2 bytes

This instruction is similar to the MIN instruction except for timing and the direction of information flow. MOUT moves the number of bytes specified in the C register from the field pointed to by HL to a buffered output device. A byte is written using the EX WRITE strobe every 8.8 microseconds and interrupts can be inhibited for a maximum of 161 microseconds. As with MIN there is no existing 2200 system I/O device capable of being used with the MOUT instruction.

NOTE: To output a block of 256 bytes using a loop similar to the one described for MIN (a MOUT instruction would appear where a MIN instruction appears in the example) would take 2650 microseconds if no interrupts occurred (an average of 10.4 microseconds per byte).

Priv. Note: If USER mode is set, this instruction will cause a privileged instruction interrupt to occur.

5.8.6 Category 4 — Processor State Save and Restore Instructions

STACK STORE **STKS**

Op Code: 065
Timing: 1.6+C•2.4
Length: 1 byte

The STACK STORE instruction POPs a specified number of Stack entries and stores them (LSB followed by MSB) in the field pointed to by HL. Upon entry, HL points to the left-hand byte.

Entry: HL=first location in the storage area
C=the number of entries to be POPPED and stored (1 through 16; 0 or 16 implies 16)

Exit: HL and C indeterminate
Condition flags unchanged

STACK LOAD **STKL**

Op Code: 111 065
Timing: 4.4+C•2.2
Length: 2 bytes

The STACK LOAD instruction pushes onto the Stack the specified number of entries from the field pointed to by HL. Upon entry HL points to the right hand byte and the entries are loaded in reverse order to allow restoring the Stack from locations stored using the STKS instruction.

Entry: HL=last location in the storage area
C=the number of entries to be PUSHED (1 through 16; 0 or 16 implies 16)

Exit: HL=indeterminate

C=indeterminate
Condition flags unchanged.

REGISTER STORE **REGS**

Op Code: 055
Timing: 13.2
Length: 1 byte

The REGISTER STORE instruction stores all of the registers for the currently selected mode (ALPHA or BETA) in the field pointed to by the top entry of the Stack. This entry points to the right-hand byte of the field and the registers are stored in reverse order moving to the left. When the instruction terminates, the top entry of the Stack points to the left of the left-hand byte in the field. For example, if entry is made with the top entry of the Stack pointing to location 02007 (octal), the registers are stored as follows:

02000:A
02001:B
02002:C
02003:D
02004:E
02005:H
02006:L
02007:X

In the above example, the top entry of the Stack will be 01777 when the instruction terminates. The contents of neither the registers nor the condition flags for the given mode are altered by this instruction.

REGISTER LOAD **REGL**

Op Code: 111 055
Timing: 12.2
Length: 2 bytes

The REGISTER LOAD instruction loads all of the registers for a given mode (ALPHA or BETA) from the field pointed to by HL. Upon entry, HL points to the right-hand byte of the field. The registers are loaded in reverse order moving to the left in the field. In this manner, the registers can be reloaded from values stored by the REGS instruction. In the example given for the REGS instruction, if the REGL instruction were entered with HL=02007, the registers shown would be loaded from the locations shown. The condition flags are not altered by this instruction.

CONDITION CODE SAVE **CCS, CCS(r)**

Op Code: 042, r 042
Timing 2.4 if Zero true and Carry false;
2.6 if Zero and Carry true;
3.0 for other cases.
Add 1.0 if r specified.
Length: 1 byte or 2 bytes if r specified.

This instruction loads the register (r) with a value such that if the value is added to itself using the AD operation, the condition flags will all be restored to their state before the CCS instruction was executed. The logic equations for the value loaded into (r) are:

A7=Carry
A6=Sign
A5=A4=A3=A2=0
A1=Not Zero and Not Sign
A0=Not Zero and Not Parity

This instruction does not alter the state of any of the condition flags. If (r) is not specified, the A register is used.

5.8.7 Category 5 — Address Manipulation Instructions

INCREMENT REGISTER PAIR **INCP**

Mnemonics	Op Codes	Timing
INCP HL	015	2.8
INCP HL,2	117 015	3.8
INCP HL,A	017	3.0
INCP BC	062 015	3.6
INCP BC,2	113 015	3.8
INCP BC,A	062 017	3.8
INCP DE	174 015	3.6
INCP DE,2	115 015	3.8
INCP DE,A	174 017	3.8
INCP XA	022 015	3.6
INCP XA,2	111 015	3.8
INCP XA,A	022 017	3.8

These instructions increment the indicated register pair by either one, two or the contents of the A register. The increment value is added to the LSP register and then the carry is added to the MSP register. The Carry Condition flag reflects the carry from the incrementation. The rest of the flags are indeterminate. The A register is not changed, except in the XA case.

DECREMENT REGISTER PAIR **DECP**

Mnemonics	Op Codes	Timing
DECP HL	035	2.8
DECP HL,2	117 035	3.8
DECP HL,A	037	3.0
DECP BC	062 035	3.6
DECP BC,2	113 035	3.8
DECP BC,A	062 037	3.8
DECP DE	174 035	3.6
DECP DE,2	115 035	3.8
DECP DE,A	174 037	3.8
DECP XA	022 035	3.6
DECP XA,2	111 035	3.8
DECP XA,A	022 037	3.8

These instructions decrement the indicated register pair by either one, two, or the contents of the A register. The decrement value is subtracted from the LSP register and then the borrow is subtracted from the MSP register. The Carry Condition flag relects the borrow from the decrementation. The rest of the flags are indeterminate. The A register is not changed, except in the case of XA.

DOUBLE LOAD **DL**

Mnemonics	Op Codes	Timing
DL DE,HL	047	3.6
DL BC,HL	111 047	5.4

DL BC,BC	062 047	4.8
DL BC,DE	113 047	5.2
DL DE,BC	174 047	4.8
DL DE,DE	115 047	5.2
DL HL,BC	176 047	4.8
DL HL,DE	117 047	5.2
DL HL,HL	057	3.6

These instructions load the register pair specified by the first operand from the memory location pointed to by the register pair specified by the second operand. The LSP register (C, E, or L) is loaded from the specified memory location and the MSP register (B,D, or H) is loaded from the next higher memory location. Note that indirect addressing can be accomplished by loading a register pair from the locations that the pair specify (DL HL,HL for example).

DOUBLE STORE **DS**

Mnemonics	Op Codes	Timing
DS DE,HL	027	3.6
DS BC,HL	111 027	5.4
DS BC,DE	113 027	5.2
DS DE,BC	174 027	4.8
DS HL,BC	176 027	4.8
DS HL,DE	117 027	5.2

These instructions store the register pair specified by the first operand into the memory locations pointed to by the register pair specified by the second operand. The LSP register (C,E, or L) is stored in the specified memory location and the MSP register (B,D or H) is stored in the next higher location.

PAGED LOAD **PL**

Mnemonics	Op Codes	Timing
PL A,(loc)	105 LSP	3.0
PL B,(loc)	114 LSP	3.0
PL C,(loc)	124 LSP	3.0
PL D,(loc)	134 LSP	3.0
PL E,(loc)	144 LSP	3.0
PL H,(loc)	154 LSP	3.0
PL L,(loc)	164 LSP	3.0

These instructions load the specified register from the memory location specified by the LSP given in the instruction and the X register.

PAGED STORE **PS**

Mnemonics	Op Codes	Timing
PS A,(loc)	107 LSP	3.0
PS B,(loc)	116 LSP	3.0
PS C,(loc)	126 LSP	3.0
PS D,(loc)	136 LSP	3.0
PS E,(loc)	146 LSP	3.0
PS H,(loc)	156 LSP	3.0
PS L,(loc)	166 LSP	3.0

These instructions store the specified register in the memory location specified by the LSP given in the instruction and the MSP given in the X register.

DOUBLE PAGED LOAD **DPL**

Mnemonics	Op Codes	Timing
DPL BC,(loc)	111 124 LSP	5.0
DPL DE,(loc)	113 144 LSP	5.0
DPL HL,(loc)	115 164 LSP	5.0

These instructions load the specified register pair from the memory locations specified by the LSP given in the instruction and the MSP given in the X register. The C,E, or L register is loaded from the specified memory location and the B,D, or H register is loaded from the next higher location.

DOUBLE PAGED STORE **DPS**

Mnemonics	Op Codes	Timing
DPS BC,(loc)	111 126 LSP	5.0
DPS DE,(loc)	113 146 LSP	5.0
DPS HL,(loc)	115 166 LSP	5.0

These instructions store the specified register pair in the locations specified by the LSP given in the instruction and the MSP given in the X register. The C, E or L register is stored in the specified location and the B, D or H register is stored in the next higher location.

INCREMENT AND DECREMENT INDEX **INCI, DECI**

Mnemonics	Op Codes	Timing
INCI (disp), (index)	005 LSP(i)	7.4
DECI (disp), (index)	025 LSP(i)	7.6
INCI*(disp), (index)	111 005 LSP MSP(i)	9.4
DECI*(disp),(index)	111 025 LSP MSP(i)	9.6

The processor has a construct called an index which is a 16-bit value kept in memory. The concept is similar to index registers except that all the values are kept in the page of memory pointed to by the X register. The index is specified by a single byte in the instructions (shown as (i) above) which points to the memory location containing the LSP of the index value, the MSP being in the next higher memory location ((i) specifies the LSP of the index address while the X register specifies the MSP of the index address). The instruction also contains a displacement (shown as (disp) above) that is either one or two bytes in length (depending upon the op code). These instructions either increment or decrement the value of the index by the displacement. The Carry condition flag reflects the carry or borrow from the incrementation or decrementation. The rest of the condition flags are indeterminate.

Stack: 1 entry used

LOAD FROM INDEX INCREMENTED OR DECREMENTED **LFII, LFID**

Mnemonics	Op Codes	Timing
LFII BC,(disp), (index)	062 005 LSP(i)	7.4
LFID BC,(disp),(index)	062 025 LSP(i)	7.6
LFII BC,*(disp),(index)	113 005 LSP MSP(i)	8.4
LFID BC,*(disp),(index)	113 025 LSP MSP(i)	8.6
LFII DE,(disp),(index)	174 005 LSP(i)	7.4
LFID DE,(disp),(index)	174 025 LSP(i)	7.6

LFII DE,*(disp),(index)	115 005 LSP MSP(i)	8.4
LFID DE,*(disp),(index)	115 025 LSP MSP(i)	8.6
LFII HL,(disp),(index)	176 005 LSP(i)	7.4
LFID HL,(disp),(index)	176 025 ISP(i)	7.6
LFII HL,*(disp),(index)	117 005 LSP MSP(i)	8.4
LFID HL,*(disp),(index)	117 025 LSP MSP(i)	8.6

These instructions are similar to the INCI and DECI instructions except that they load the specified pair of registers with the result of adding or subtracting the displacement to or from the index value of the index. The condition flags are similarly affected.
Stack: 1 entry used.

5.8.8 Category 6 - Operating System Control

BASE REGISTER LOAD **BRL, BRL(r)**

Op Code: 072, r 072
Timing: 1.2 or 2.2 if r specified.
Length: 1 or 2 if r specified

This instruction loads the base register from the specified register. Note that the base register cannot be saved. For this reason, loading the base register will normally be a monitor function, allowing the monitor to keep within itself the value of the base register for user state storage purposes. This instruction will cause a privileged instruction interrupt if the USER mode flag is set. If (r) is not specified, the A register is used.

NOP JUMP **NOJ loc**

Op Code: 045
Timing: 1.4
Length: 3 bytes.

This instruction increments the P-counter twice. It is useful for overstoring jump instructions which might be executed while being overstored. The procedure to overstore a jump instruction would be to first overstore the op code with an 045 (NOP JUMP) and then update the address portion. Then the op code could be overstored with the appropriate jump instruction. The primary use of this instruction is for overstoring the interrupt vector jump instructions for the interrupts which cannot be disabled (such as MEMORY PARITY FAULT) and which might happen while the jump is being overstored.

SYSTEM CALL **SC**

Op Code: 067
Timing: 1.8

This instruction causes the USER mode flag to be cleared, the last entry in the sector table to be set to the last 4K section of *physical* memory space with access protection, and a CALL to be performed to location 0167452 (in the ROM). This is the mechanism via which the user would communicate with an operating system that used the USER mode.

USER RETURN **UR**

Op Code: 111 102
Timing: 2.0

This instruction is identical to the RETURN instruction (op code 007) except that additionally the USER mode flag is set.

SECTOR TABLE LOAD **STL**

Op Code: 077
Timing: 3.2+C•1.8
Length: 1 byte

This instruction loads up to the first 15 entries in the sector table. This table contains six bits for each entry. The right hand two bits are not used and should always be set to zero. Bit 2 is set for access enable. Bit 3 is set for write enable. The left-hand four bits are used to map that entry into a particular 4K section of *physical* memory space. This instruction will cause a privileged instruction interrupt if the USER mode flag is set.

Entry: HL=location of first byte in table
of up to 15 to load.
C=number of entries to load (0 to 15).
Exit: No registers or conditions changed.
Stack: 1 entry used.

BREAKPOINT **BP**

Op Code: 052
Timing: 2.2
Length: 1 byte

This instruction is similar to a SYSTEM CALL (SC) instruction except the call is performed to location 0167460 of system RAM. This will cause entry into the system DEBUG routine if the location is not changed.

ENABLE INTERRUPTS AND JUMP **EJMP**

Op Code: 111 050
Timing: 4.4
Length: 4 bytes

This instruction is identical to the ENABLE INTERRUPTS (EI) instruction except that additionally a jump is performed to the (LSP, MSP) address.

ENABLE INTERRUPTS AND RETURN **EUR**
ERU

Op Code: 062 050
Timing: 3.8
Length: 2 bytes

This instruction is identical to the combination of the ENABLE INTERRUPTS, Set USER Mode Flag and RETURN instructions.

ภาคผนวก ข

CONFIGURATION OPTIONS MODE

The 8200 Terminal has provisions to establish twenty terminal configuration options. These options are keyed into the terminal ROM memory. The terminal will always power up in a configuration determined by these options. Some of the options can be temporarily changed during terminal operation; however, on the next power up, the terminal configuration will revert to the options stored in the terminal ROM memory. The configuration option mode can be accessed only when the terminal is OFF LINE. Control sequences to select the options are given in Paragraph 3.11. All control sequences are made through the keyboard. The available options are as follows:

a. Display brightness
b. Double key
c. Transmit baud rate select
d. Receive baud rate select
e. Parity select
f. Control key
g. Upper case character set only
h. Print additional characters
i. Line feed and carriage return after printing character "80"
j. Auto roll up with bottom line feed
k. Roll down
l. Cursor increment with delete character
m. Cursor off
n. Bell on printing character "64"
o. Local display (half duplex)
p. Local erase
q. Transmit erase
r. Local home
s. Transmit home
t. Local break

After the terminal has entered the configuration mode, the configuration mode display will appear on the terminal screen. A message describing each option is displayed, along with the current setting of the option. Baud rate information is displayed in its numeric value i.e., if the receive baud rate is set at 9600 baud, the display will show 'RX BAUD 9600'. Parity option information will be displayed with the word 'PARITY' followed by a '1' for one parity, a '0' for zero parity, an 'E' for even parity, or an 'O' for odd parity. The remaining options are displayed with a brief message followed by a 'Y' or an 'N' depending on whether the option is enabled or not. If an option is to be skipped, depressing the ENTER key will cause the cursor to skip to the next option. Each of the configuration options are discussed below. Keyboard codes for each option are given in parenthesis after the option name. The first word(s) in capitol letters in each explanation shows the way the option is displayed on the terminal screen.

a. Display Brightness (No select code)

This option (not displayed on terminal screen), allows the display brightness to be set at one of sixteen brightness levels. To adjust the brightness, hold the CTRL key down and repeatedly depress the blank key either above or below the CTRL key. When the configuration mode is terminated, the existing brightness level will be stored in the terminal EAROM memory. This option can be overridden during ON LINE terminal operation, but on the next terminal power up, the brightness will revert to that selected by this display brightness option.

b. Double Key (Y, N)

DBL KEY causes the F1 and F5 keys to have the same function as their adjacent control keys (NEW LINE and INT). This option may be changed by down line load.

1) Y - This code causes the F1 and F5 keys to have the same function as the NEW LINE and INT keys respectively.

2) N - This code causes the F1 and F5 keys to have their standard or normal functions as assigned by the code chart (Table 3-7), as in the PROM option, or as down line loaded.

c. Baud Rate Select

TX BAUD and RX BAUD allows the transmit and receive baud rates to be set at one of fourteen values. The baud rates are set by keying in the decimal numbers for each desired baud rate. Baud rates may be set from 50 baud to 9600 baud. This option can not be changed by down line load.

d. Parity Select (E, O, 1, Ø)

PARITY permits selection of the type of parity bit to be appended to the seven bits of data transmitted to the host computer. The terminal ignores the parity bit on receive data. Parity options are as follows:

1) E - even parity
2) O - odd parity
3) 1 - "1" parity
4) Ø - "0" parity

e. Control Key (Y, N)

CTRL KEY provides the capability to generate all the ASCII control characters for transmission to the host processor as system's key codes.

1) Y - This code alters the system's key code (changes 6th and 7th bits to 0) transmitted to the host processor for any alphanumeric key (excludes other control keys) that is depressed while the CTRL key is held down. Other functions of the CTRL key will not change.

2) N - This code allows the CTRL key to be used in the OFF LINE mode or to enter or exit from it.

f. Upper Case Character Set Only (Y, N)

UP CASE permits transmission of standard upper case/lower case or upper case characters only.

1) Y - This code causes the terminal to substitute upper case key codes for lower case key codes before transmitting to the host processor. Only the twenty-six alphabetic codes are changed. Display data from the host processor is not effected.

2) N - This code causes the terminal to transmit the standard upper case/lower case character set to the host processor.

g. Print Additional Characters (Y, N)

PRINT ALL provides the means to increase the number of displayable characters.

1) Y - This code allows the terminal to display ASCII characters below octal 040 if they have been defined in option PROM or have been down line loaded in a special character set.

2) N - This code causes the terminal to ignore all ASCII characters received from the host processor below octal 040 except the control characters.

h. Line Feed and Carriage Return After Printing Character "80" (Y, N)

AUTO CR/LF provides the means to control the display action when the 81st character of a line is received. When the 80th character is received, the cursor will remain at that position and be displayed alternately with the character.

1) Y - This code causes the terminal to move the cursor to the first character position on the next line after displaying a character in the 80th position of a line. After displaying a character in the 80th position of the 24th line, the cursor will move to the first position of the 24th line. Additional characters will then overwrite the characters on the 24th line. However, if the Auto Roll Up with bottom line feed option has also been selected, then displaying a character in the 80th position of the 24th line will cause the screen to be rolled up one line and the cursor to be positioned at the first character position of the 24th line.

2) N - This code inactivates line feed and carriage return. When an 81st character (or more) is received without an intervening control character to move the cursor, the last character received is displayed in the 80th position. Characters

previously displayed in the 80th position are lost. Characters in positions 1 through 79 are not disturbed.

i. Auto Roll Up With Bottom Line Feed (Y, N)

AUTO ROLL allows the displayed data to move up when the cursor is on the 24th line and a LINE FEED control character is received.

1) Y - This code causes the display to move up one line leaving the 24th line blank if the cursor is on the 24th line and a LINE FEED control character has been received. The data previously displayed on line one is lost.

2) N - This code causes the terminal to ignore the LINE FEED control character while the cursor is on the 24th line.

j. Roll Down (Y, N)

ROLL DN allows the displayed data to be moved down leaving line one blank.

1) Y - This code causes the display to move down one line leaving the first line blank if a ROLL DOWN control character is received. Data previously displayed on line twenty-four is lost. The cursor position is not effected.

2) N - This code causes the terminal to ignore the ROLL DOWN control character.

k. Cursor Increment with Delete Character (Y, N)

PRINT DEL allows a selection of alternate controls over the cursor movement when it receives a delete character.

1) Y - This code causes the terminal to display the delete symbol and move the cursor to the next character position when a DEL character is received.

2) N - This code causes the cursor to remain in it's present position when the DEL character is received.

l. Cursor Off (Y, N)

CURS OFF allows the host processor to turn the cursor on or off.

1) Y - This code causes the terminal to respond to CURSOR ON and CURSOR OFF control characters. Cursor position is not effected by these control characters.

2) N - This code causes the terminal to ignore the CURSOR ON and CURSOR OFF control characters. The cursor will always be displayed.

m. Bell On Printing Character "64" (Y, N)

BELL allows a selection of alternate controls over sounding the bell.

1) Y - This code causes the terminal to sound the bell whenever a character is displayed in the 64th character position of any display line and sound the bell when the BELL control character is received from the host processor.

2) N - This code causes the terminal to sound the bell when the BELL control character is received from the host processor.

n. Local Display (Y, N)

LOC DISP is the same as half duplex operation. This option allows a selection of half or full duplex operation. This option should be selection only when the host processor is not echoing characters back to the terminal.

1) Y - This code causes the terminal to display displayable characters that are transmitted to the host processor. The terminal will continue to display characters received.

2) N - This code causes the terminal to display only those displayable characters that are received from the host processor.

o. Local Erase (Y, N)

LOC ERASE provides a means for the operator to initiate the EEOF (erase to end of frame) function which causes the screen to be erased from the current cursor position to the last character of the last line.

1) Y - This code causes the terminal to erase the screen from the current cursor position to tne last character of the last line whenever the operator depresses the designated ERASE key (blank key betwemn the INT and CTRL keys). An EEOF system key code is not transmitted to the host processor. Characters received while the erase function is in process will be buffered and no data will be lost.

2) N - This code permits the terminal to respond only to an EEOF character received from the host processor.

p. Transmit Erase (Y, N)

TX ERASE provides a means for the operator to initiate an EEOF (erase to end of frame) system key code to the host processor.

1) Y - This code causes the terminal to generate an EEOF system key code and transmit it to the host processor whenever the operator depresses the designated ERASE key (blank key between the INT and CTRL keys).

2) N - This code negates the Transmit Erase function.

q. Local Home (Y, N)

LOC HOME permits the operator to move the cursor to the "home up" position (first character of first line).

1) Y - This code allows the cursor to be moved to the home up position whenever the designated HOME key (blank key between CTRL and NEW LINE keys), is depressed. No system key code is transmitted to the host processor.

2) N - This code causes the terminal to respond only to the HOME UP character received from the host processor.

r. Transmit Home (Y, N)

TX HOME provides a means for the operator to transmit a HOME UP system key code to the host processor.

1) Y - This code causes the terminal to generate a HOME UP system key code and transmit it to the host processor whenever the operator depresses the designated HOME key (blank key between the CTRL and the NEW LINE keys).

2) N - This code negates the Transmit Home function.

s. Local Break (Y, N)

BREAK provides a means to generate a "break" condition at the terminal. A break occurs when the "transmit data line" in the I/O connector goes to the spacing condition (positive voltage, data bits all zero) for a period of time longer than the normal character time. This condition is sometimes used as a means of signalling between devices that communicate serially.

1) Y - This code causes the terminal to generate a break condition whenever the BREAK key (F3) is depressed. The duration of the break condition is independent of the length of time that the BREAK key is depressed.

2) N - This code causes the terminal to take no local action when the BREAK key (F3) is depressed. However, the terminal will transmit the F3 key currently assigned system key code to the host processor.

```
OFF LINE                VER 1.1

RX BAUD 9600
TX BAUD 9600
PARITY E
DBL KEY Y
UP CASE N
BREAK N
LOC ERASE N
TX ERASE N
LOC HOME N
TX HOME N
LOC DISP N
CTRL KEY N
AUTO ROLL N
AUTO CR/LF N
ROLL DN N
PRINT ALL N
PRINT DEL N
CURS OFF Y
BELL N
```

Configuration Option Mode Sample Display

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intel®

8080A/8080A-1/8080A-2
8-BIT N-CHANNEL MICROPROCESSOR

The 8080A is functionally and electrically compatible with the Intel® 8080.

- **TTL Drive Capability**
- **2 μs (– 1:1.3 μs, – 2:1.5 μs) Instruction Cycle**
- **Powerful Problem Solving Instruction Set**
- **6 General Purpose Registers and an Accumulator**
- **16-Bit Program Counter for Directly Addressing up to 64K Bytes of Memory**
- **16-Bit Stack Pointer and Stack Manipulation Instructions for Rapid Switching of the Program Environment**
- **Decimal, Binary, and Double Precision Arithmetic**
- **Ability to Provide Priority Vectored Interrupts**
- **512 Directly Addressed I/O Ports**

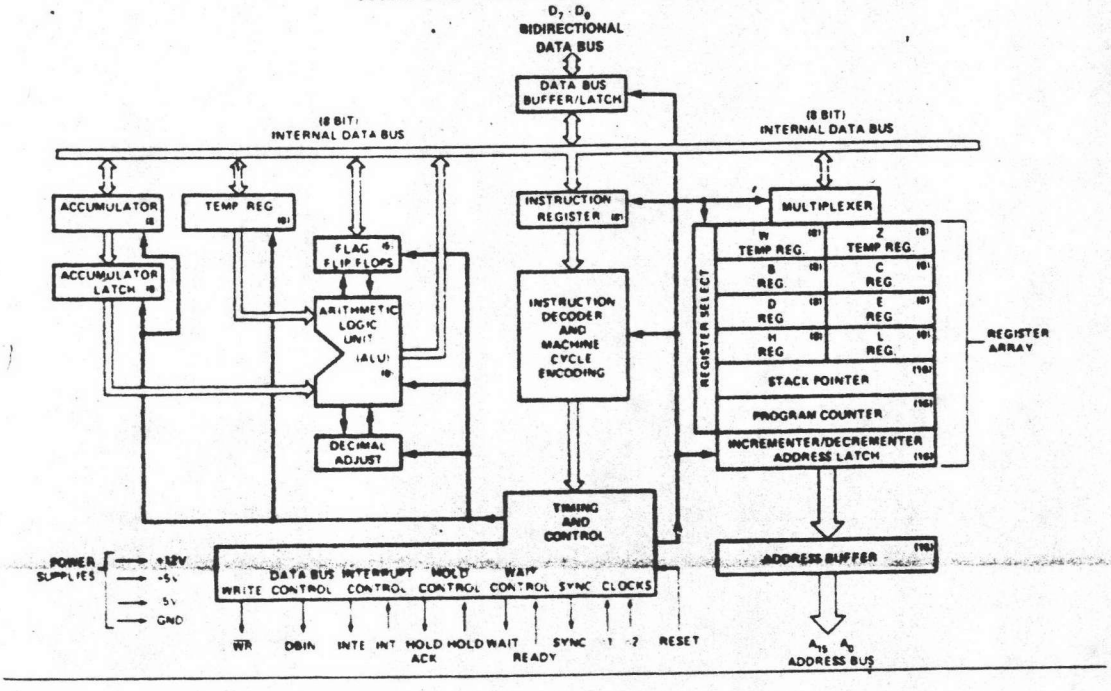
The Intel®.8080A is a complete 8-bit parallel central processing unit (CPU). It is fabricated on a single LSI chip using Intel's n-channel silicon gate MOS process. This offers the user a high performance solution to control and processing applications.

The 8080A contains 6 8-bit general purpose working registers and an accumulator. The 6 general purpose registers may be addressed individually or in pairs providing both single and double precision operators. Arithmetic and logical instructions set or reset 4 testable flags. A fifth flag provides decimal arithmetic operation.

The 8080A has an external stack feature wherein any portion of memory may be used as a last in/first out stack to store/retrieve the contents of the accumulator, flags, program counter, and all of the 6 general purpose registers. The 16-bit stack pointer controls the addressing of this external stack. This stack gives the 8080A the ability to easily handle multiple level priority interrupts by rapidly storing and restoring processor status. It also provides almost unlimited subroutine nesting.

This microprocessor has been designed to simplify systems design. Separate 16-line address and 8-line bidirectional data busses are used to facilitate easy interface to memory and I/O. Signals to control the interface to memory and I/O are provided directly by the 8080A. Ultimate control of the address and data busses resides with the HOLD signal. It provides the ability to suspend processor operation and force the address and data busses into a high impedance state. This permits OR-tying these busses with other controlling devices for (DMA) direct memory access or multiprocessor operation.

8080A CPU FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

The following describes the function of all of the 8080A I/O pins. Several of the descriptions refer to internal timing periods.

A_{15}-A_0 (output three-state)
ADDRESS BUS; the address bus provides the address to memory (up to 64K 8-bit words) or denotes the I/O device number for up to 256 input and 256 output devices. A_0 is the least significant address bit.

D_7-D_0 (input/output three-state)
DATA BUS; the data bus provides bi-directional communication between the CPU, memory, and I/O devices for instructions and data transfers. Also, during the first clock cycle of each machine cycle, the 8080A outputs a status word on the data bus that describes the current machine cycle. D_0 is the least significant bit.

SYNC (output)
SYNCHRONIZING SIGNAL; the SYNC pin provides a signal to indicate the beginning of each machine cycle.

DBIN (output)
DATA BUS IN; the DBIN signal indicates to external circuits that the data bus is in the input mode. This signal should be used to enable the gating of data onto the 8080A data bus from memory or I/O.

READY (input)
READY; the READY signal indicates to the 8080A that valid memory or input data is available on the 8080A data bus. This signal is used to synchronize the CPU with slower memory or I/O devices. If after sending an address out the 8080A does not receive a READY input, the 8080A will enter a WAIT state for as long as the READY line is low. READY can also be used to single step the CPU.

WAIT (output)
WAIT; the WAIT signal acknowledges that the CPU is in a WAIT state.

$\overline{WR}$ (output)
WRITE; the $\overline{WR}$ signal is used for memory WRITE or I/O output control. The data on the data bus is stable while the $\overline{WR}$ signal is active low ($\overline{WR}$ = 0).

HOLD (input)
HOLD; the HOLD signal requests the CPU to enter the HOLD state. The HOLD state allows an external device to gain control of the 8080A address and data bus as soon as the 8080A has completed its use of these buses for the current machine cycle. It is recognized under the following conditions:

- the CPU is in the HALT state.
- the CPU is in the T2 or TW state and the READY signal is active.

As a result of entering the HOLD state the CPU ADDRESS BUS (A_{15}-A_0) and DATA BUS (D_7-D_0) will be in their high impedance state. The CPU acknowledges its state with the HOLD ACKNOWLEDGE (HLDA) pin.

HLDA (output)
HOLD ACKNOWLEDGE; the HLDA signal appears in response to the HOLD signal and indicates that the data and address bus will go to the high impedance state. The HLDA signal begins at

- T3 for READ memory or input.
- The Clock Period following T3 for WRITE memory or OUTPUT operation.

In either case, the HLDA signal appears after the rising edge of ϕ_1 and high impedance occurs after the rising edge of ϕ_2.

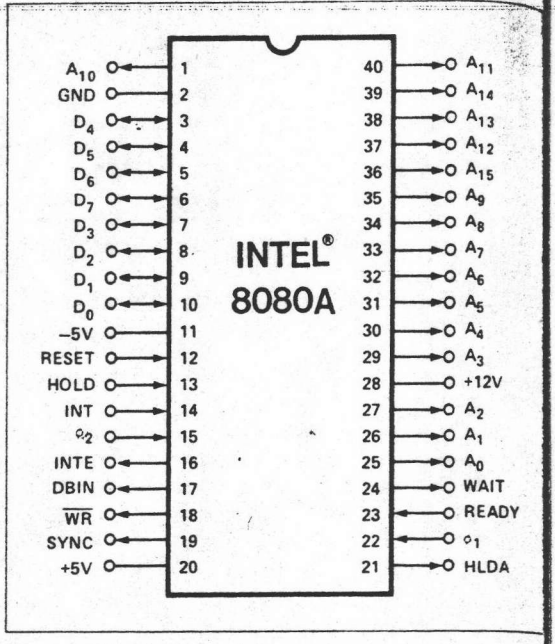


Figure 1. Pin Configuration

INTE (output)
INTERRUPT ENABLE; indicates the content of the internal interrupt enable flip/flop. This flip/flop may be set or reset by the Enable and Disable Interrupt instructions and inhibits interrupts from being accepted by the CPU when it is reset. It is automatically reset (disabling further interrupts) at time T1 of the instruction fetch cycle (M1) when an interrupt is accepted and also reset by the RESET signal.

INT (input)
INTERRUPT REQUEST; the CPU recognizes an interrupt request on this line at the end of the current instruction or while halted. If the CPU is in the HOLD state or if the Interrupt Enable flip/flop is reset it will not honor the request.

RESET (input) [1]
RESET, while the RESET signal is activated, the content of the program counter is cleared. After RESET, the program will start at location 0 in memory. The INTE and HLDA flip/flops are also reset. Note that the flags, accumulator, stack pointer, and registers are not cleared.

V_{SS}	Ground Reference.
V_{DD}	+12 ± 5% Volts
V_{CC}	+5 ± 5% Volts
V_{BB}	-5 ±5% Volts (substrate bias)
ϕ_1, ϕ_2	2 externally supplied clock phases (non TTL compatible)

MCS-80/85

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to +70° C
Storage Temperature	-65°C to +150°C
All Input or Output Voltages With Respect to V_{BB}	-0.3V to +20V
V_{CC}, V_{DD} and V_{SS} With Respect to V_{BB}	-0.3V to +20V
Power Dissipation	1.5W

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = -5V ± 5%, V_{SS} = 0V, Unless Otherwise Noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	$V_{SS}-1$		$V_{SS}+0.8$	V	
V_{IHC}	Clock Input High Voltage	9.0		$V_{DD}+1$	V	
V_{IL}	Input Low Voltage	$V_{SS}-1$		$V_{SS}+0.8$	V	
V_{IH}	Input High Voltage	3.3		$V_{CC}+1$	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.9mA on all outputs, I_{OH} = -150μA.
V_{OH}	Output High Voltage	3.7			V	
$I_{DD\,(AV)}$	Avg. Power Supply Current (V_{DD})		40	70	mA	Operation T_{CY} = .48 μsec
$I_{CC\,(AV)}$	Avg. Power Supply Current (V_{CC})		60	80	mA	
$I_{BB\,(AV)}$	Avg. Power Supply Current (V_{BB})		.01	1	mA	
I_{IL}	Input Leakage			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
I_{CL}	Clock Leakage			±10	μA	$V_{SS} \leq V_{CLOCK} \leq V_{DD}$
I_{DL} [2]	Data Bus Leakage in Input Mode			-100 -2.0	μA mA	$V_{SS} \leq V_{IN} \leq V_{SS}+0.8V$ $V_{SS}+0.8V \leq V_{IN} \leq V_{CC}$
I_{FL}	Address and Data Bus Leakage During HOLD			+10 -100	μA	$V_{ADDR/DATA} = V_{CC}$ $V_{ADDR/DATA} = V_{SS}$ + 0.45V

CAPACITANCE

T_A = 25°C $V_{CC} = V_{DD} = V_{SS}$ = 0V, V_{BB} = -5V

Symbol	Parameter	Typ.	Max.	Unit	Test Condition
C_ϕ	Clock Capacitance	17	25	pf	f_c = 1 MHz
C_{IN}	Input Capacitance	6	10	pf	Unmeasured Pins
C_{OUT}	Output Capacitance	10	20	pf	Returned to V_{SS}

NOTES:

1. The RESET signal must be active for a minimum of 3 clock cycles.
2. When DBIN is high and $V_{IN} > V_{IH}$ an internal active pull up will be switched onto the Data Bus.
3. ΔI supply / ΔT_A = -0.45%/°C.

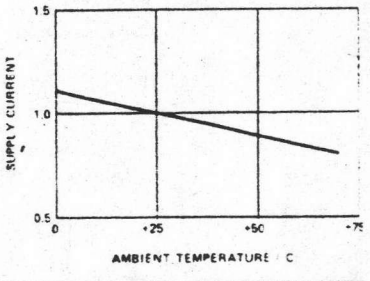


Figure 2. Typical Supply Current vs. Temperature, Normalized[3]

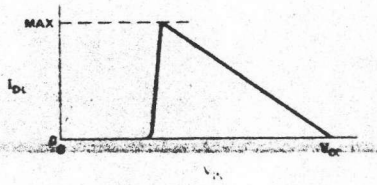


Figure 3. Data Bus Characteristic During DBIN

INSTRUCTION SET

The accumulator group instructions include arithmetic and logical operators with direct, indirect, and immediate addressing modes.

Move, load, and store instruction groups provide the ability to move either 8 or 16 bits of data between memory, the six working registers and the accumulator using direct, indirect, and immediate addressing modes.

The ability to branch to different portions of the program is provided with jump, jump conditional, and computed jumps. Also the ability to call to and return from subroutines is provided both conditionally and unconditionally. The RESTART (or single byte call instruction) is useful for interrupt vector operation.

Double precision operators such as stack manipulation and double add instructions extend both the arithmetic and interrupt handling capability of the 8080A. The ability to increment and decrement memory, the six general registers and the accumulator is provided as well as extended increment and decrement instructions to operate on the register pairs and stack pointer. Further capability is provided by the ability to rotate the accumulator left or right through or around the carry bit.

Input and output may be accomplished using memory addresses as I/O ports or the directly addressed I/O provided for in the 8080A instruction set.

The following special instruction group completes the 8080A instruction set: the NOP instruction, HALT to stop processor execution and the DAA instructions provide decimal arithmetic capability. STC allows the carry flag to be directly set, and the CMC instruction allows it to be complemented. CMA complements the contents of the accumulator and XCHG exchanges the contents of two 16-bit register pairs directly.

Data and Instruction Formats

Data in the 8080A is stored in the form of 8-bit binary integers. All data transfers to the system data bus will be in the same format.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

DATA WORD

The program instructions may be one, two, or three bytes in length. Multiple byte instructions must be stored in successive words in program memory. The instruction formats then depend on the particular operation executed.

One Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE

TYPICAL INSTRUCTIONS

Register to register, memory reference, arithmetic or logical, rotate, return, push, pop, enable or disable Interrupt instructions

Two Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OPERAND

Immediate mode or I/O instructions

Three Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	LOW ADDRESS OR OPERAND 1
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HIGH ADDRESS OR OPERAND 2

Jump, call or direct load and store instructions

For the 8080A a logic "1" is defined as a high level and a logic "0" is defined as a low level.

8080 INSTRUCTION SET

Summary of Processor Instructions

Mnemonic	Description	Instruction Code[1] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[2] Cycles
MOVE, LOAD, AND STORE										
MOVr1,r2	Move register to register	0	1	D	D	D	S	S	S	5
MOV M,r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r,M	Move memory to register	0	1	D	D	D	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
XCHG	Exchange D & E H & L Registers	1	1	1	0	1	0	1	1	4
STACK OPS										
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	11
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	11
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	11
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	11
POP B	Pop register Pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register Pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register Pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10
XTHL	Exchange top of stack H & L	1	1	1	0	0	0	1	1	18
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	5
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	5
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	5
JUMP										
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JC	Jump on carry	1	1	0	1	1	0	1	0	10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	10
JZ	Jump on zero	1	1	0	0	1	0	1	0	10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	10
JP	Jump on positive	1	1	1	1	0	0	1	0	10
JM	Jump on minus	1	1	1	1	1	0	1	0	10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	10
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	5
CALL										
CALL	Call unconditional	1	1	0	0	1	1	0	1	17
CC	Call on carry	1	1	0	1	1	1	0	0	11/17
CNC	Call on no carry	1	1	0	1	0	1	0	0	11/17
CZ	Call on zero	1	1	0	0	1	1	0	0	11/17
CNZ	Call on no zero	1	1	0	0	0	1	0	0	11/17
CP	Call on positive	1	1	1	1	0	1	0	0	11/17
CM	Call on minus	1	1	1	1	1	1	0	0	11/17
CPE	Call on parity even	1	1	1	0	1	1	0	0	11/17
CPO	Call on parity odd	1	1	1	0	0	1	0	0	11/17
RETURN										
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	5/11
RNC	Return on no carry	1	1	0	1	0	0	0	0	5/11
RZ	Return on zero	1	1	0	0	1	0	0	0	5/11
RNZ	Return on no zero	1	1	0	0	0	0	0	0	5/11
RP	Return on positive	1	1	1	1	0	0	0	0	5/11
RM	Return on minus	1	1	1	1	1	0	0	0	5/11
RPE	Return on parity even	1	1	1	0	1	0	0	0	5/11
RPO	Return on parity odd	1	1	1	0	0	0	0	0	5/11
RESTART										
RST	Restart	1	1	A	A	A	1	1	1	11
INCREMENT AND DECREMENT										
INR r	Increment register	0	0	D	D	D	1	0	0	5
DCR r	Decrement register	0	0	D	D	D	1	0	1	5
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	5
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	5
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	5
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	5
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	5
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	5
ADD										
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10

NOTES 1 DDD or SSS B 000 C 001 D 010 E 011 H 100 L 101 Memory 110 A 111

2 Two possible cycle times (6/12) indicate instruction cycles dependent on condition flags

Summary of Processor Instructions (Cont.)

Mnemonic	Description	Instruction Code[1] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[2] Cycles
SUBTRACT										
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7
LOGICAL										
ANA r	And register with A	1	0	1	0	0	S	S	S	4
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
ROTATE										
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
SPECIALS										
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
INPUT/OUTPUT										
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
CONTROL										
EI	Enable interrupts	1	1	1	1	1	0	1	1	4
DI	Disable interrupt	1	1	1	1	0	0	1	1	4
NOP	No-operation	0	0	0	0	0	0	0	0	4
HLT	Halt	0	1	1	1	0	1	1	0	7

NOTES 1 DDD or SSS B=000 C=001 D=010 E=011 H=100 L=101 Memory=110 A=111
2 Two possible cycle times (6/12) indicate instruction cycles dependent on condition flags

intel

8224
CLOCK GENERATOR AND DRIVER FOR 8080A CPU

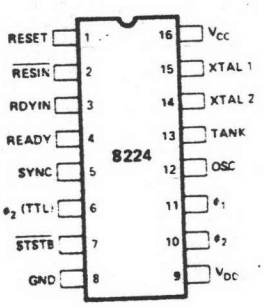
- Single Chip Clock Generator/Driver for 8080A CPU
- Power-Up Reset for CPU
- Ready Synchronizing Flip-Flop
- Advanced Status Strobe
- Oscillator Output for External System Timing
- Crystal Controlled for Stable System Operation
- Reduces System Package Count

The Intel® 8224 is a single chip clock generator/driver for the 8080A CPU. It is controlled by a crystal, selected by the designer to meet a variety of system speed requirements.

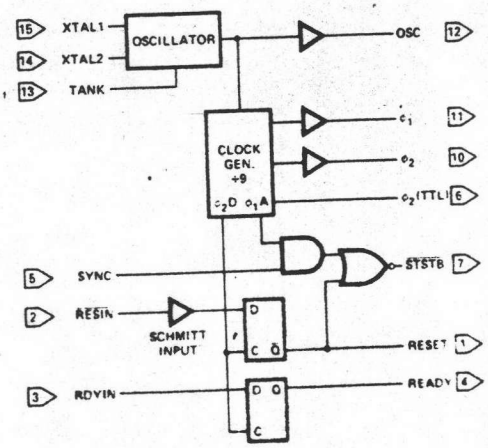
Also included are circuits to provide power-up reset, advance status strobe, and synchronization of ready.

The 8224 provides the designer with a significant reduction of packages used to generate clocks and timing for 8080A.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

RESIN	RESET INPUT
RESET	RESET OUTPUT
RDYIN	READY INPUT
READY	READY OUTPUT
SYNC	SYNC INPUT
STSTB	STATUS STB (ACTIVE LOW)
Φ1	8080 CLOCKS
Φ2	

XTAL 1	CONNECTIONS FOR CRYSTAL
XTAL 2	
TANK	USED WITH OVERTONE XTAL
OSC	OSCILLATOR OUTPUT
Φ2 (TTL)	Φ2 CLK (TTL LEVEL)
VCC	+5V
VDD	+12V
GND	0V

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to 70°C
Storage Temperature . . . . . −65°C to 150°C
Supply Voltage, V_{CC} . . . . . −0.5V to +7V
Supply Voltage, V_{DD} . . . . . −0.5V to +13.5V
Input Voltage . . . . . −1.5V to +7V
Output Current 100mA

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to 70°C; V_{CC} = +5.0V ±5%; V_{DD} = +12V ±5%.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_F	Input Current Loading			-.25	mA	V_F = .45V
I_R	Input Leakage Current			10	μA	V_R = 5.25V
V_C	Input Forward Clamp Voltage			1.0	V	I_C = -5mA
V_{IL}	Input "Low" Voltage			.8	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage	2.6 2.0			V	Reset Input All Other Inputs
V_{IH}-V_{IL}	RESIN Input Hysteresis	.25			V	V_{CC} = 5.0V
V_{OL}	Output "Low" Voltage			.45 .45	V V	(ϕ_1,ϕ_2), Ready, Reset, $\overline{STSTB}$ I_{OL} =2.5mA All Other Outputs I_{OL} = 15mA
V_{OH}	Output "High" Voltage ϕ_1 , ϕ_2 READY, RESET All Other Outputs	 9.4 3.6 2.4			 V V V	 I_{OH} = -100μA I_{OH} = -100μA I_{OH} = -1mA
I_{SC}[1]	Output Short Circuit Current (All Low Voltage Outputs Only)	-10		-60	mA	V_O = 0V V_{CC} = 5.0V
I_{CC}	Power Supply Current			115	mA	
I_{DD}	Power Supply Current			12	mA	

Note: 1. Caution, ϕ_1 and ϕ_2 output drivers do not have short circuit protection

Crystal Requirements

Tolerance: 0.005% at 0°C-70°C
Resonance: Series (Fundamental)*
Load Capacitance: 20-35 pF
Equivalent Resistance: 75-20 ohms
Power Dissipation (Min): 4 mW

*With tank circuit use 3rd overtone mode.

8228/8238
SYSTEM CONTROLLER AND BUS DRIVER FOR 8080A CPU

- **Single Chip System Control for MCS-80™ Systems**
- **Built-In Bidirectional Bus Driver for Data Bus Isolation**
- **Allows the Use of Multiple Byte Instructions (e.g. CALL) for Interrupt Acknowledge**
- **User Selected Single Level Interrupt Vector (RST 7)**
- **28-Pin Dual In-Line Package**
- **Reduces System Package Count**
- ***8238 Has Advanced IOW/MEMW for Large System Timing Control**

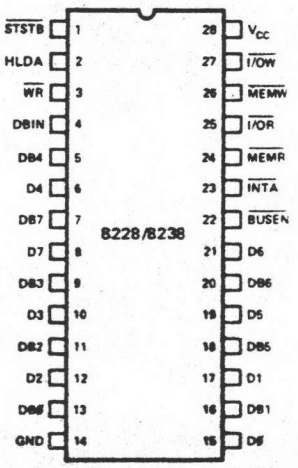
The Intel® 8228 is a single chip system controller and bus driver for MCS-80. It generates all signals required to directly interface MCS-80 family RAM, ROM, and I/O components.

A bidirectional bus driver is included to provide high system TTL fan-out. It also provides isolation of the 8080 data bus from memory and I/O. This allows for the optimization of control signals, enabling the systems designer to use slower memory and I/O. The isolation of the bus driver also provides for enhanced system noise immunity.

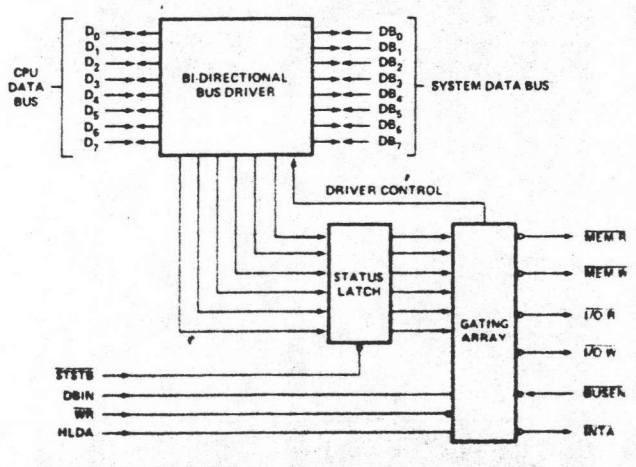
A user selected single level interrupt vector (RST 7) is provided to simplify real time, interrupt driven, small system requirements. The 8228 also generates the correct control signals to allow the use of multiple byte instructions (e.g., CALL) in response to an interrupt acknowledge by the 8080A. This feature permits large, interrupt driven systems to have an unlimited number of interrupt levels.

The 8228 is designed to support a wide variety of system bus structures and also reduce system package count for cost effective, reliable design of the MCS-80 systems.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

D7-D0	DATA BUS (8080 SIDE)	INTA	INTERRUPT ACKNOWLEDGE
DB7-DB0	DATA BUS (SYSTEM SIDE)	HLDA	HLDA (FROM 8080)
MEMR	MEMORY READ	WR	WR (FROM 8080)
I/OW	I/O WRITE	BUSEN	BUS ENABLE INPUT
MEMR	MEMORY READ	STSTB	STATUS STROBE (FROM 8224
MEMW	MEMORY WRITE	VCC	+5V
DBIN	DBIN (FROM 8080	GND	0 VOLTS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . −0°C to 70°C
Storage Temperature . . . . . −65°C to 150°C
Supply Voltage, V_{CC} . . . . . −0.5V to +7V
Input Voltage . . . . . −1.5V to +7V
Output Current 100mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS T_A = 0°C to 70°C; V_{CC} = 5V ±5%.

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
V_C	Input Clamp Voltage, All Inputs		.75	-1.0	V	V_{CC}=4.75V; I_C=-5mA
I_F	Input Load Current, $\overline{STSTB}$			500	µA	V_{CC} = 5.25V
	D_2 & D_6			750	µA	V_F = 0.45V
	D_0, D_1, D_4, D_5, & D_7			250	µA	
	All Other Inputs			250	µA	
I_R	Input Leakage Current $\overline{STSTB}$			100	µA	V_{CC} = 5.25V
	DB_0-DB_7			20	µA	V_R = 5.25V
	All Other Inputs			100	µA	
V_{TH}	Input Threshold Voltage, All Inputs	0.8		2.0	V	V_{CC} = 5V
I_{CC}	Power Supply Current		140	190	mA	V_{CC}=5.25V
V_{OL}	Output Low Voltage, D_0-D_7			.45	V	V_{CC}=4.75V; I_{OL}=2mA
	All Other Outputs			.45	V	I_{OL} = 10mA
V_{OH}	Output High Voltage, D_0-D_7	3.6	3.8		V	V_{CC}=4.75V; I_{OH}=-10µA
	All Other Outputs	2.4			V	I_{OH} = -1mA
I_{OS}	Short Circuit Current, All Outputs	15		90	mA	V_{CC}=5V
$I_{O(off)}$	Off State Output Current, All Control Outputs			100	µA	V_{CC}=5.25V; V_O=5.25
				-100	µA	V_O=.45V
I_{INT}	INTA Current			5	mA	(See Figure below)

Note 1: Typical values are for T_A = 25°C and nominal supply voltages.

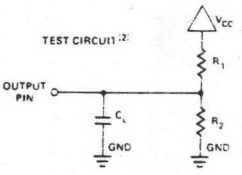
CAPACITANCE

This parameter is periodically sampled and not 100% tested.

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit
C_{IN}	Input Capacitance		8	12	pF
C_{OUT}	Output Capacitance Control Signals		7	15	pF
I/O	I/O Capacitance (D or DB)		8	15	pF

Test Conditions: NS: $V_{BIAS} = 2.5V$, $V_{CC} = 5.0V$, $T_A = 25°C$, f = 1MHz.

Note 2: For D_0-D_7: $R_1 = 4K\Omega$, $R_2 = \infty\Omega$, $C_L = 25pF$. For all other outputs: $R_1 = 500\Omega$, $R_2 = 1K\Omega$, $C_L = 100pF$.



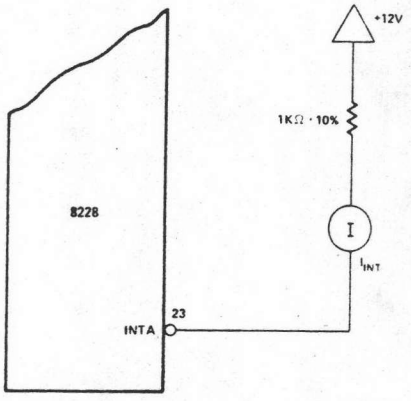


Figure 1. INTA Test Circuit (for RST 7)

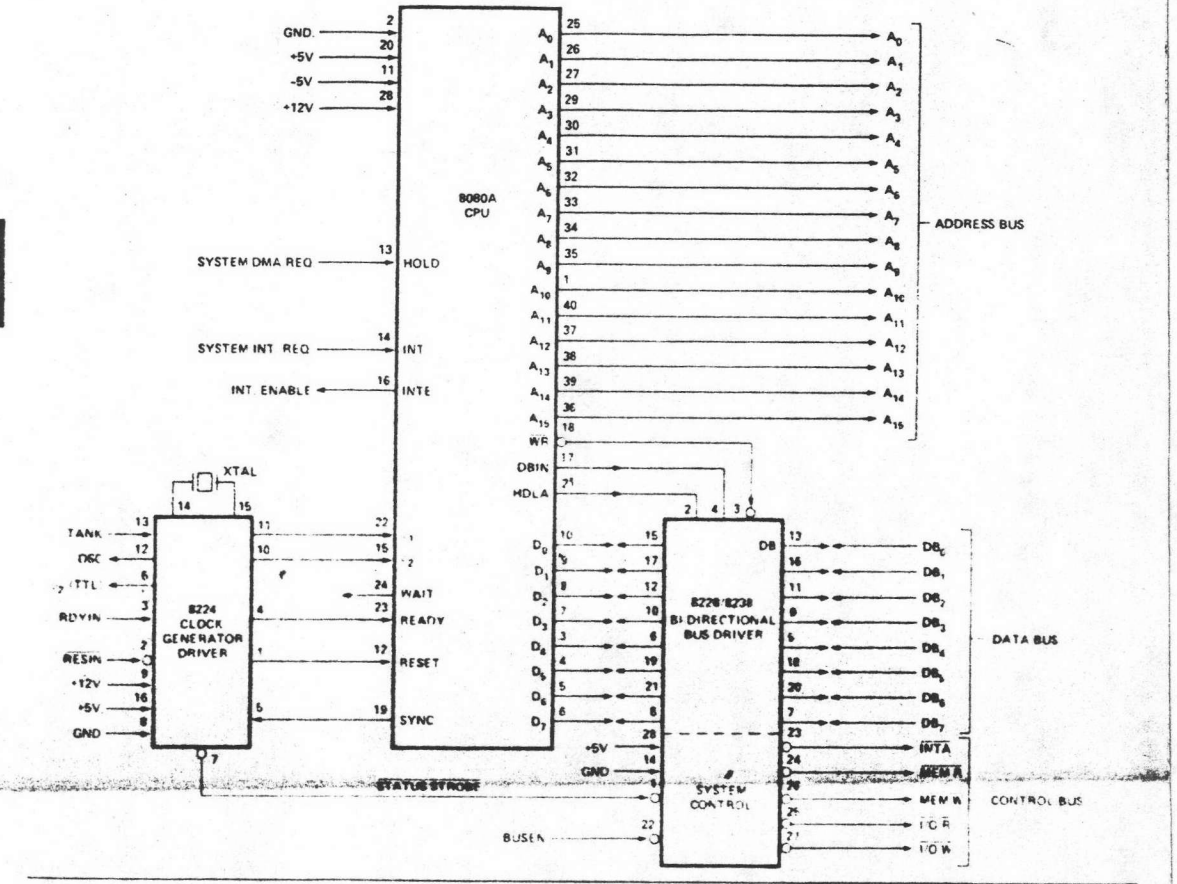


Figure 2. CPU Standard Interface

2708/8708*
8K AND 4K UV ERASABLE PROM

	Max. Power	Max. Access	Organization
2708	800 mW	450 ns	1K x 8
2708L	425 mW	450 ns	1K x 8
2708-1	800 mW	350 ns	1K x 8
2704	800 mW	450 ns	512 x 8

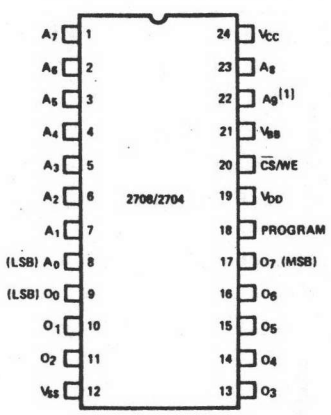
- **Low Power Dissipation — 425 mW Max. (2708L)**
- **Fast Access Time — 350 ns Max. (2708-1)**
- **Static — No Clocks Required**
- **Data Inputs and Outputs TTL Compatible during both Read and Program Modes**
- **Three-State Outputs — OR-Tie Capability**

The Intel® 2708 is a 8192-bit ultraviolet light erasable and electrically reprogrammable EPROM, ideally suited where fast turnaround and pattern experimentation are important requirements. All data inputs and outputs are TTL compatible during both the read and program modes. The outputs are three-state, allowing direct interface with common system bus structures.

The 2708L at 425 mW is available for systems requiring lower power dissipation than from the 2708. A power dissipation savings of over 50%, without any sacrifice in speed, is obtained with the 2708L. The 2708L has high input noise immunity and is specified at 10% power supply tolerance. A high-speed 2708-1 is also available at 350 ns for microprocessors requiring fast access times. For smaller size systems there is the 4096-bit 2704 which is organized as 512 words by 8 bits. All these devices have the same programming and erasing specifications of the 2708. The 2704 electrical specifications are the same as the 2708.

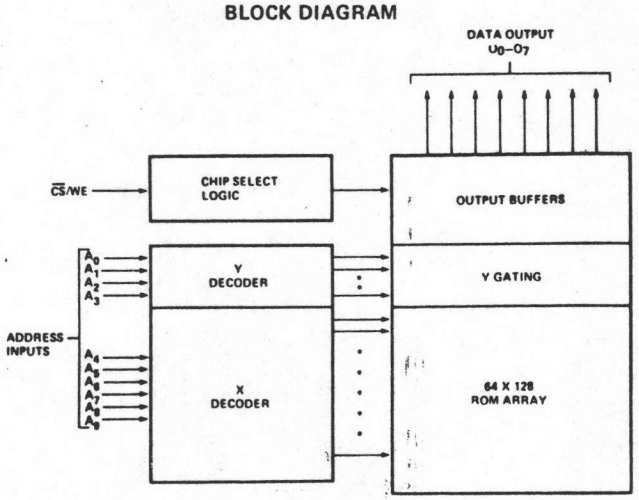
The 2708 family is fabricated with the N-channel silicon gate FAMOS technology and is available in a 24-pin dual in-line package.

PIN CONFIGURATION



NOTE 1: PIN 22 MUST BE CONNECTED TO V_{SS} FOR THE 2704.

BLOCK DIAGRAM



PIN NAMES

A_0-A_9	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS/INPUTS
$\overline{CS}$/WE	CHIP SELECT/WRITE ENABLE INPUT

PIN CONNECTION DURING READ OR PROGRAM

	PIN NUMBER							
MODE	DATA I/O 9-11, 13-17	ADDRESS INPUTS 1-8, 22, 23	V_{SS} 12	PROGRAM 18	V_{DD} 19	$\overline{CS}$/WE 20	V_{BB} 21	V_{CC} 24
READ	D_{OUT}	A_{IN}	GND	GND	+12	V_{IL}	-5	+5
DESELECT	HIGH IMPEDANCE	DON'T CARE	GND	GND	+12	V_{IH}	-5	+5
PROGRAM	D_{IN}	A_{IN}	GND	PULSED 26V	+12	V_{IHW}	-5	+5

*All 8708 specifications are identical to the 2708 specifications.

PROGRAMMING

The programming specifications are described in the Data Catalog PROM/ROM Programming Instructions Section.

Absolute Maximum Ratings*

Temperature Under Bias	−25°C to +85°C
Storage Temperature	−65°C to +125°C
V_{DD} With Respect to V_{BB}	+20V to −0.3V
V_{CC} and V_{SS} With Respect to V_{BB}	+15V to −0.3V
All Input or Output Voltages With Respect to V_{BB} During Read	+15V to −0.3V
$\overline{CS}$/WE Input With Respect to V_{BB} During Programming	+20V to −0.3V
Program Input With Respect to V_{BB}	+35V to −0.3V
Power Dissipation	1.5W

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PROM/ROM

DC and AC Operating Conditions During Read

	2708	2708-1	2708L
Temperature Range	0°C – 70°C	0°C – 70°C	0°C – 70°C
V_{CC} Power Supply	5V ± 5%	5V ± 5%	5V ± 10%
V_{DD} Power Supply	12V ± 5%	12V ± 5%	12V ± 10%
V_{BB} Power Supply	−5V ± 5%	−5V ± 5%	−5V ± 10%

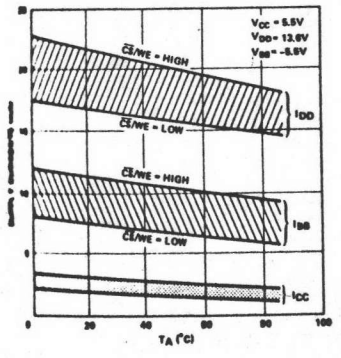
READ OPERATION

D.C. and Operating Characteristics

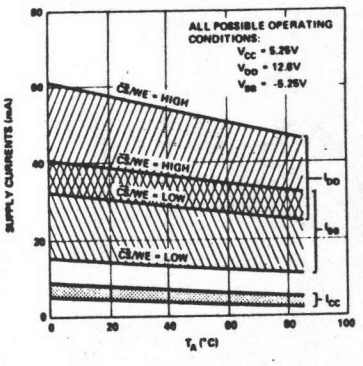
Symbol	Parameter	2708, 2708-1 Limits			2708L Limits			Units	Test Conditions
		Min.	Typ.[2]	Max.	Min.	Typ.[2]	Max.		
I_{LI}	Address and Chip Select Input Sink Current		1	10		1	10	μA	V_{IN} = 5.25V or V_{IN} = V_{IL}
I_{LO}	Output Leakage Current		1	10		1	10	μA	V_{OUT} = 5.5V, CS/WE = 5V
I_{DD}[3]	V_{DD} Supply Current		50	65		21	28	mA	Worst Case Supply Currents[4]:
I_{CC}[3]	V_{CC} Supply Current		6	10		2	4	mA	All Inputs High;
I_{BB}[3]	V_{BB} Supply Current		30	45		10	14	mA	$\overline{CS}$/WE = 5V; T_A = 0°C
V_{IL}	Input Low Voltage	V_{SS}		0.65	V_{SS}		0.65	V	
V_{IH}	Input High Voltage	3.0		V_{CC}+1	2.2		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45			0.4	V	I_{OL} = 1.6mA (2708, 2708-1)
									I_{OL} = 2mA (2708L)
V_{OH1}	Output High Voltage	3.7			3.7			V	I_{OH} = −100 μA
V_{OH2}	Output High Voltage	2.4			2.4			V	I_{OH} = −1 mA
PD	Power Dissipation			800			325	mW	T_A = 70°C
							425	mW	T_A = 0°C

NOTES:
1. V_{BB} must be applied prior to V_{CC} and V_{DD}. V_{BB} must also be the last power supply switched off
2. Typical values are for T_A = 25°C and nominal supply voltages.
3. The total power dislipation is not calculated by summing the various currents (I_{DD}, I_{CC}, and I_{BB}) multiplied by their respective voltages since current paths exist between the various power supplies and V_{SS}. The I_{DD}, I_{CC}, and I_{BB} currents should be used to determine power supply capacity only.
4. I_{BB} for the 2708L is specified in the programmed state and is 18 mA maximum in the unprogrammed state.

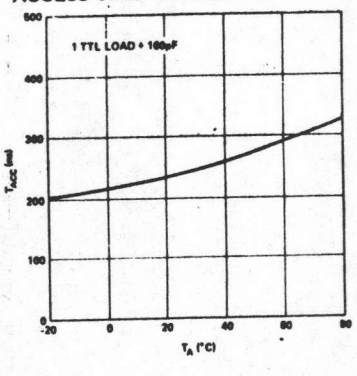
2708L RANGE OF SUPPLY CURRENTS VS. TEMPERATURE



2708 AND 2708-1 RANGE OF SUPPLY CURRENTS VS. TEMPERATURE



ACCESS TIME VS. TEMPERATURE



A. C. Characteristics

Symbol	Parameter	2708-1 Limits Min.	Typ.	Max.	2708, 2708L, Limits Min.	Typ.	Max.	Units
t_{ACC}	Address to Output Delay		280	350		280	450	ns
t_{CO}	Chip Select to Output Delay		60	120		60	120	ns
t_{DF}	Chip Deselect to Output Float	0		120	0		120	ns
t_{OH}	Address to Output Hold	0			0			ns

CAPACITANCE[1] $T_A = 25°C$, f = 1 MHz

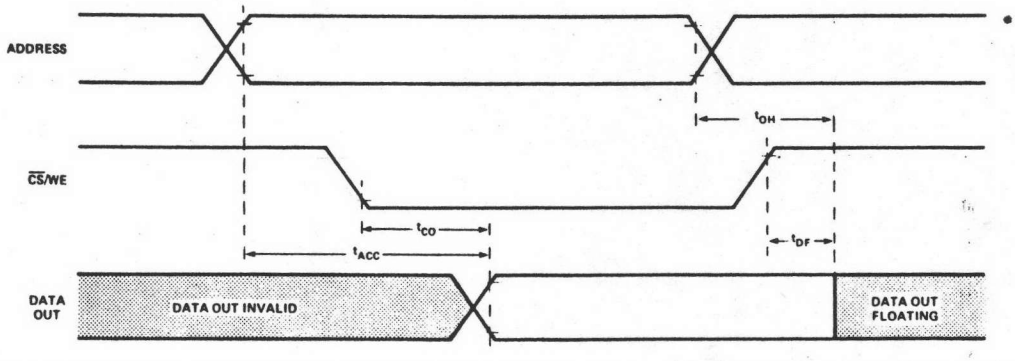
Symbol	Parameter	Typ.	Max.	Unit.	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

Note: 1. This parameter is periodically sampled and is not 100% tested.

A.C. TEST CONDITIONS:

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤20 ns
Timing Measurement Reference Levels: 0.8V and 2.8V for inputs; 0.8V and 2.4V for outputs.
Input Pulse Levels: 0.65V to 3.0V

Waveforms



ERASURE CHARACTERISTICS

The erasure characteristics of the 2708 family are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000–4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical device in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the 2708 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available form Intel which should be placed over the 2708 window to prevent unintentional erasure.

The recommended erasure procedure (see Data Catalog PROM/ROM Programming Instructions Section) for the 2708 family is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The device should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

intel

2114
1024 X 4 BIT STATIC RAM

	2114-2	2114-3	2114	2114L2	2114L3	2114L
Max. Access Time (ns)	200	300	450	200	300	450
Max. Power Dissipation (mw)	525	525	525	370	370	370

- **High Density 18 Pin Package**
- **Identical Cycle and Access Times**
- **Single +5V Supply**
- **No Clock or Timing Strobe Required**
- **Completely Static Memory**
- **Directly TTL Compatible: All Inputs and Outputs**
- **Common Data Input and Output Using Three-State Outputs**
- **Pin-Out Compatible with 3605 and 3625 Bipolar PROMs**

The Intel® 2114 is a 4096-bit static Random Access Memory organized as 1024 words by 4-bits using N-channel Silicon-Gate MOS technology. It uses fully DC stable (static) circuitry throughout — in both the array and the decoding — and therefore requires no clocks or refreshing to operate. Data access is particularly simple since address setup times are not required. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

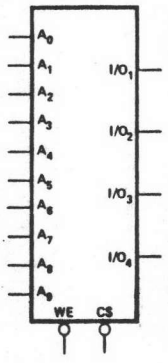
The 2114 is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. The 2114 is placed in an 18-pin package for the highest possible density.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are or-tied.

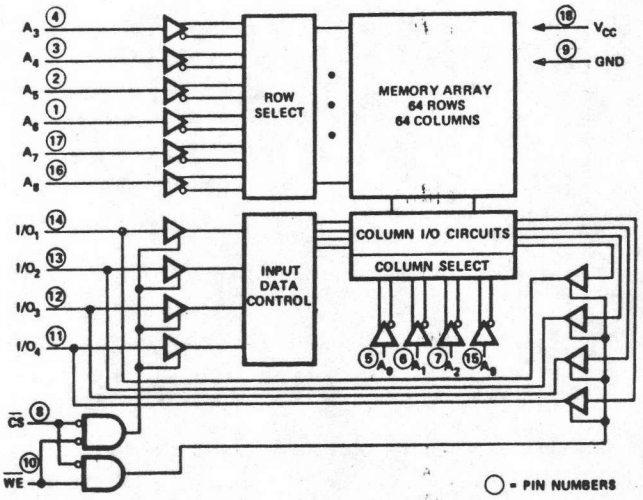
The 2114 is fabricated with Intel's N-channel Silicon-Gate technology — a technology providing excellent protection against contamination permitting the use of low cost plastic packaging.

PIN CONFIGURATION

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0–A_9	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND	GROUND
$\overline{CS}$	CHIP SELECT		
I/O_1–I/O_4	DATA INPUT/OUTPUT		

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -10°C to 80°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin
With Respect to Ground ..... -0.5V to +7V
Power Dissipation 1.0W
D.C. Output Current 5mA

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise noted.

SYMBOL	PARAMETER	2114-2, 2114-3, 2114 Min.	Typ.[1]	Max.	2114L2, 2114L3, 2114L Min.	Typ.[1]	Max.	UNIT	CONDITIONS
I_{LI}	Input Load Current (All Input Pins)			10			10	µA	V_{IN} = 0 to 5.25V
$\|I_{LO}\|$	I/O Leakage Current			10			10	µA	$\overline{CS}$ = 2.4V, $V_{I/O}$ = 0.4V to V_{CC}
I_{CC1}	Power Supply Current		80	95			65	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0 mA, T_A = 25°C
I_{CC2}	Power Supply Current			100			70	mA	V_{IN} = 5.25V, $I_{I/O}$ = 0 mA, T_A = 0°C
V_{IL}	Input Low Voltage	-0.5		0.8	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		6.0	2.0		6.0	V	
I_{OL}	Output Low Current	2.1	6.0		2.1	6.0		mA	V_{OL} = 0.4V
I_{OH}	Output High Current	-1.0	-1.4		-1.0	-1.4		mA	V_{OH} = 2.4V
I_{OS}[2]	Output Short Circuit Current			40			40	mA	

NOTE: 1. Typical values are for T_A = 25°C and V_{CC} = 5.0V.
2. Duration not to exceed 30 seconds.

CAPACITANCE

T_A = 25°C, f = 1.0 MHz

SYMBOL	TEST	MAX	UNIT	CONDITIONS
$C_{I/O}$	Input/Output Capacitance	5	pF	$V_{I/O}$ = OV
C_{IN}	Input Capacitance	5	pF	V_{IN} = OV

NOTE: This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels ..... 0.8 Volt to 2.4 Volt
Input Rise and Fall Times ..... 10 nsec
Input and Output Timing Levels ..... 1.5 Volts
Output Load ..... 1 TTL Gate and C_L = 100 pF

TEST NOTE: This circuit employs a self starting oscillator and a charge pump which require a certain amount of time after POWER ON to start functioning properly. This 2114 circuit is conservatively specified as requiring 500 µsec after V_{CC} reaches its specified limits (4.75V).

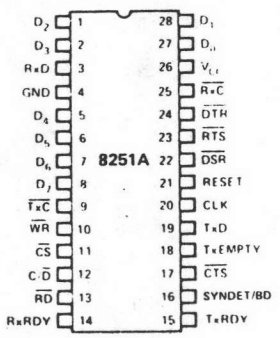
intel

8251A
PROGRAMMABLE COMMUNICATION INTERFACE

- Synchronous and Asynchronous Operation
- Synchronous 5-8 Bit Characters; Internal or External Character Synchronization; Automatic Sync Insertion
- Asynchronous 5-8 Bit Characters; Clock Rate—1, 16 or 64 Times Baud Rate; Break Character Generation; 1, 1½, or 2 Stop Bits; False Start Bit Detection; Automatic Break Detect and Handling; 19.2K Baud.
- Baud Rate — DC to 64K Baud
- Full Duplex, Double Buffered, Transmitter and Receiver
- Error Detection — Parity, Overrun and Framing
- Fully Compatible with 8080/8085 CPU
- 28-Pin DIP Package
- All Inputs and Outputs are TTL Compatible
- Single +5V Supply
- Single TTL Clock

The Intel® 8251A is the enhanced version of the industry standard, Intel® 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART), designed for data communications with Intel's new high performance family of microprocessors such as the 8085. The 8251A is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM "bi-sync"). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data ,transmission errors and control signals such as SYNDET, TxEMPTY. The chip is constructed using N-channel silicon gate technology.

PIN CONFIGURATION

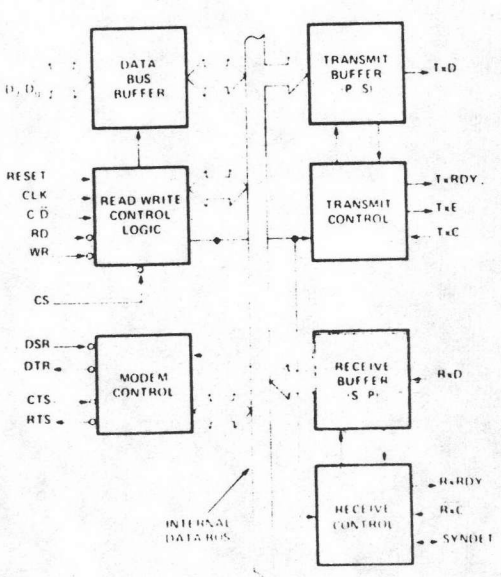


PIN NAMES

D_7 D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
RD	Read Data Command
WR	Write Data or Control Command
CS	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
$\overline{TxC}$	Transmitter Clock
TxD	Transmitter Data
$\overline{RxC}$	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)

$\overline{DSR}$	Data Set Ready
$\overline{DTR}$	Data Terminal Ready
SYNDET/BD	Sync Detect/ Break Detect
$\overline{RTS}$	Request to Send Data
$\overline{CTS}$	Clear to Send Data
TxE	Transmitter Empty
V_{CC}	+5 Volt Supply
GND	Ground

BLOCK DIAGRAM



FEATURES AND ENHANCEMENTS

8251A is an advanced design of the industry standard USART, the Intel® 8251. The 8251A operates with an extended range of Intel microprocessors that includes the new 8085 CPU and maintains compatibility with the 8251. Familiarization time is minimal because of compatibility and involves only knowing the additional features and enhancements, and reviewing the AC and DC specifications of the 8251A.

The 8251A incorporates all the key features of the 8251 and has the following additional features and enhancements:

- 8251A has double-buffered data paths with separate I/O registers for control, status, Data In, and Data Out, which considerably simplifies control programming and minimizes CPU overhead.
- In asynchronous operations, the Receiver detects and handles "break" automatically, relieving the CPU of this task.
- A refined Rx initialization prevents the Receiver from starting when in "break" state, preventing unwanted interrupts from a disconnected USART.
- At the conclusion of a transmission, TxD line will always return to the marking state unless SBRK is programmed.
- Tx Enable logic enhancement prevents a Tx Disable command from halting transmission until all data previously written has been transmitted. The logic also prevents the transmitter from turning off in the middle of a word.
- When External Sync Detect is programmed, Internal Sync Detect is disabled, and an External Sync Detect status is provided via a flip-flop which clears itself upon a status read.
- Possibility of false sync detect is minimized by ensuring that if double character sync is programmed, the characters be contiguously detected and also by clearing the Rx register to all ones whenever Enter Hunt command is issued in Sync mode.
- As long as the 8251A is not selected, the $\overline{RD}$ and $\overline{WR}$ do not affect the internal operation of the device.
- The 8251A Status can be read at any time but the status update will be inhibited during status read.
- The 8251A is free from extraneous glitches and has enhanced AC and DC characteristics, providing higher speed and better operating margins.
- Baud rate from DC to 64K.
- Fully compatible with Intel's new industry standard, the MCS-85.

8251A BASIC FUNCTIONAL DESCRIPTION

General

The 8251A is a Universal Synchronous/Asynchronous Receiver/Transmitter designed specifically for the 80/85 Microcomputer Systems. Like other I/O devices in a Microcomputer System, its functional configuration is programmed by the system's software for maximum flexibility. The 8251A can support virtually any serial data technique currently in use including bi-sync.

In a communication environment an interface device must convert parallel format system data into serial format for transmission and convert incoming serial format data into parallel system data for reception. The interface device must also delete or insert bits or characters that are functionally unique to the communication technique. In essence, the interface should appear "transparent" to the CPU, a simple input or output of byte-oriented system data.

Data Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the 8251A to the system Data Bus. Data is transmitted or received by the buffer upon execution of INput or OUTput instructions of the CPU. Control words, Command words and Status information are also transferred through the Data Bus Buffer. The command status and data in, and data out are separate 8-bit registers to provide double buffering.

This functional block accepts inputs from the system Control bus and generates control signals for overall device operation. It contains the Control Word Register and Command Word Register that store the various control formats for the device functional definition.

RESET (Reset)

A "high" on this input forces the 8251A into an "Idle" mode. The device will remain at "Idle" until a new set of control words is written into the 8251A to program its functional definition. Minimum RESET pulse width is 6 t_{CY} (clock must be running).

CLK (Clock)

The CLK input is used to generate internal device timing and is normally connected to the Phase 2 (TTL) output of the 8224 Clock Generator. No external inputs or outputs are referenced to CLK but the frequency of CLK must be greater than 30 times the Receiver or Transmitter data bit rates.

$\overline{WR}$ (Write)

A "low" on this input informs the 8251A that the CPU is writing data or control words to the 8251A.

$\overline{RD}$ (Read)

A "low" on this input informs the 8251A that the CPU is reading data or status information from the 8251A.

C/$\overline{D}$ (Control/Data)

This input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs the 8251A that the word on the Data Bus is either a data character, control word or status information.
1 = CONTROL/STATUS 0 = DATA

$\overline{CS}$ (Chip Select)

A "low" on this input selects the 8251A. No reading or writing will occur unless the device is selected. When $\overline{CS}$ is high, the Data Bus in the float state and $\overline{RD}$ and $\overline{WR}$ will have no effect on the chip.

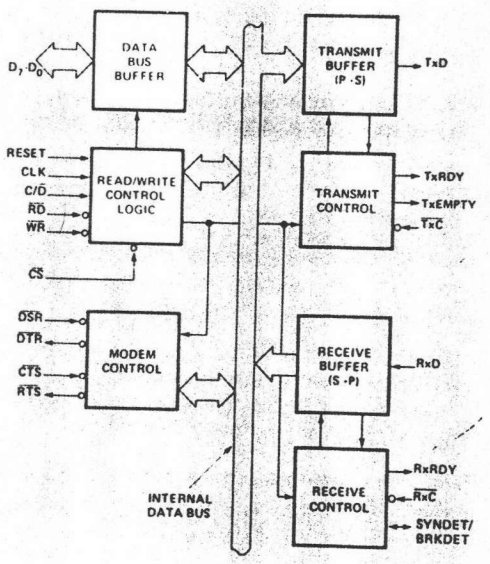


Figure 1. 8251A Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions

C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	8251A DATA → DATA BUS
0	1	0	0	DATA BUS → 8251A DATA
1	0	1	0	STATUS → DATA BUS
1	1	0	0	DATA BUS → CONTROL
X	1	1	0	DATA BUS → 3-STATE
X	X	X	1	DATA BUS → 3-STATE

Modem Control

The 8251A has a set of control inputs and outputs that can be used to simplify the interface to almost any modem. The modem control signals are general purpose in nature and can be used for functions other than modem control, if necessary.

$\overline{DSR}$ (Data Set Ready)

The $\overline{DSR}$ input signal is a general purpose, 1-bit inverting input port. Its condition can be tested by the CPU using a Status Read operation. The $\overline{DSR}$ input is normally used to test modem conditions such as Data Set Ready.

$\overline{DTR}$ (Data Terminal Ready)

The $\overline{DTR}$ output signal is a general purpose, 1-bit inverting output port. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{DTR}$ output signal is normally used for modem control such as Data Terminal Ready or Rate Select.

$\overline{RTS}$ (Request to Send)

The $\overline{RTS}$ output signal is a general purpose, 1-bit inverting output port. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{RTS}$ output signal is normally used for Modem control such as Request to Send.

$\overline{CTS}$ (Clear to Send)

A "low" on this input enables the 8251A to transmit serial data if the Tx Enable bit in the Command byte is set to a "one." If either a Tx Enable off or CTS off condition occurs while the Tx is in operation, the Tx will transmit all the data in the USART, written prior to Tx Disable command before shutting down.

Transmitter Buffer

The Transmitter Buffer accepts parallel data from the Data Bus Buffer, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin on the falling edge of $\overline{TxC}$. The transmitter will begin transmission upon being enabled if $\overline{CTS}$ = 0. The TxD line will be held in the marking state immediately upon a master Reset or when Tx Enable/$\overline{CTS}$ off or TxEMPTY.

Transmitter Control

The transmitter Control manages all activities associated with the transmission of serial data. It accepts and issues signals both externally and internally to accomplish this function.

TxRDY (Transmitter Ready)

This output signals the CPU that the transmitter is ready to accept a data character. The TxRDY output pin can be used as an interrupt to the system, since it is masked by Tx Disabled, or, for Polled operation, the CPU can check TxRDY using a Status Read operation. TxRDY is automatically reset by the leading edge of $\overline{WR}$ when a data character is loaded from the CPU.

Note that when using the Polled operation, the TxRDY status bit is *not* masked by Tx Enabled, but will only indicate the Empty/Full Status of the Tx Data Input Register.

TxE (Transmitter Empty)

When the 8251A has no characters to transmit, the TxEMPTY output will go "high". It resets automatically upon receiving a character from the CPU. TxEMPTY can be used to indicate the end of a transmission mode, so that the CPU "knows" when to "turn the line around" in the half-duplexed operational mode. TxEMPTY is independent of the Tx Enable bit in the Command instruction.

In SYNChronous mode, a "high" on this output indicates that a character has not been loaded and the SYNC character or characters are about to be or are being transmitted automatically as "fillers". TxEMPTY does not go low when the SYNC characters are being shifted out.

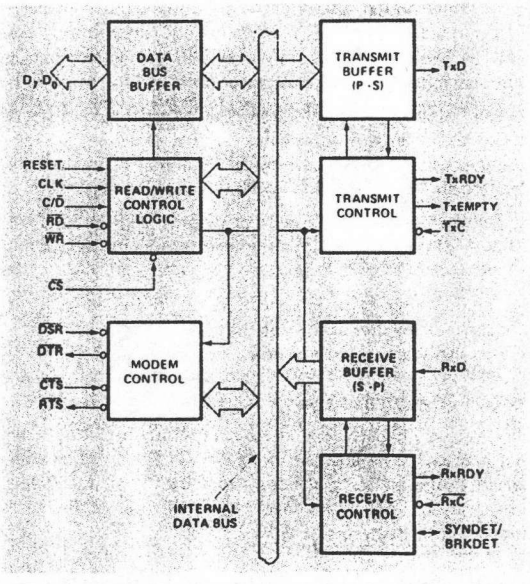


Figure 2. 8251A Block Diagram Showing Modem and Transmitter Buffer and Control Functions

$\overline{TxC}$ (Transmitter Clock)

The Transmitter Clock controls the rate at which the character is to be transmitted. In the Synchronous transmission mode, the Baud Rate (1x) is equal to the $\overline{TxC}$ frequency. In Asynchronous transmission mode the baud rate is a fraction of the actual $\overline{TxC}$ frequency. A portion of the mode instruction selects this factor; it can be 1, 1/16 or 1/64 the $\overline{TxC}$.

For Example:

If Baud Rate equals 110 Baud,
$\overline{TxC}$ equals 110 Hz (1x)
$\overline{TxC}$ equals 1.76 kHz (16x)
$\overline{TxC}$ equals 7.04 kHz (64x).

The falling edge of $\overline{TxC}$ shifts the serial data out of the 8251A.

Receiver Buffer

The Receiver accepts serial data, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to the CPU. Serial data is input to RxD pin, and is clocked in on the rising edge of $\overline{RxC}$.

Receiver Control

This functional block manages all receiver-related activities which consist of the following features:

The RxD initialization circuit prevents the 8251A from mistaking an unused input line for an active low data line in the "break condition". Before starting to receive serial characters on the RxD line, a valid "1" must first be detected after a chip master Reset. Once this has been determined, a search for a valid low (Start bit) is enabled. This feature is only active in the asynchronous mode, and is only done once for each master Reset.

The False Start bit detection circuit prevents false starts due to a transient noise spike by first detecting the falling edge and then strobing the nominal center of the Start bit (RxD = low).

The Parity Toggle F/F and Parity Error F/F circuits are used for parity error detection and set the corresponding status bit.

The Framing Error Flag F/F is set if the Stop bit is absent at the end of the data byte (asynchronous mode), and also sets the corresponding status bit.

RxRDY (Receiver Ready)

This output indicates that the 8251A contains a character that is ready to be input to the CPU. Rx RDY can be connected to the interrupt structure of the CPU or, for Polled operation, the CPU can check the condition of RxRDY using a Status Read operation.

Rx Enable off both masks and holds RxRDY in the Reset Condition. For Asynchronous mode, to set RxRDY, the Receiver must be Enabled to sense a Start Bit and a complete character must be assembled and transferred to the Data Output Register. For Synchronous mode, to set RxRDY, the Receiver must be enabled and a character must finish assembly and be transferred to the Data Output Register.

Failure to read the received character from the Rx Data Output Register prior to the assembly of the next Rx Data character will set overrun condition error and the previous character will be written over and lost. If the Rx Data is being read by the CPU when the internal transfer is occurring, overrun error will be set and the old character will be lost.

$\overline{RxC}$ (Receiver Clock)

The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode, the Baud Rate (1x) is equal to the actual frequency of $\overline{RxC}$. In Asynchronous Mode, the Baud Rate is a fraction of the actual $\overline{RxC}$ frequency. A portion of the mode instruction selects this factor: 1, 1/16 or 1/64 the $\overline{RxC}$.

For Example:

Baud Rate equals 300 Baud, if
$\overline{RxC}$ equals 300 Hz (1x)
$\overline{RxC}$ equals 4800 Hz (16x)
$\overline{RxC}$ equals 19.2 kHz (64x).

Baud Rate equals 2400 Baud, if
$\overline{RxC}$ equals 2400 Hz (1x)
$\overline{RxC}$ equals 38.4 kHz (16x)
$\overline{RxC}$ equals 153.6 kHz (64x).

Data is sampled into the 8251A on the rising edge of $\overline{RxC}$.

NOTE: In most communications systems, the 8251A will be handling both the transmission and reception operations of a single link. Consequently, the Receive and Transmit Baud Rates will be the same. Both $\overline{TxC}$ and $\overline{RxC}$ will require identical frequencies for this operation and can be tied together and connected to a single frequency source (Baud Rate Generator) to simplify the interface.

SYNDET (SYNC Detect)/BRKDET (Break Detect)

This pin is used in SYNChronous Mode for SYNDET and may be used as either input or output, programmable through the Control Word. It is reset to output mode low upon RESET. When used as an output (internal Sync mode), the SYNDET pin will go "high" to indicate that the 8251A has located the SYNC character in the Receive mode. If the 8251A is programmed to use double Sync characters (bisync), then SYNDET will go "high" in the middle of the last bit of the second Sync character. SYNDET is automatically reset upon a Status Read operation.

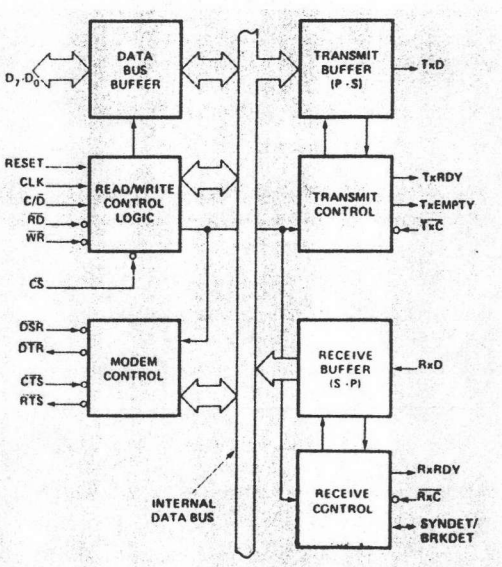


Figure 3. 8251A Block Diagram Showing Receiver Buffer and Control Functions

Mode Instruction Definition

The 8251A can be used for either Asynchronous or Synchronous data communication. To understand how the Mode Instruction defines the functional operation of the 8251A, the designer can best view the device as two separate components sharing the same package, one Asynchronous the other Synchronous. The format definition can be changed only after a master chip Reset. For explanation purposes the two formats will be isolated.

NOTE: When parity is enabled it is not considered as one of the data bits for the purpose of programming the word length. The actual parity bit received on the Rx Data line cannot be read on the Data Bus. In the case of a programmed character length of less than 8 bits, the least significant Data Bus bits will hold the data; unused bits are "don't care" when writing data to the 8251A, and will be "zeros" when reading the data from the 8251A.

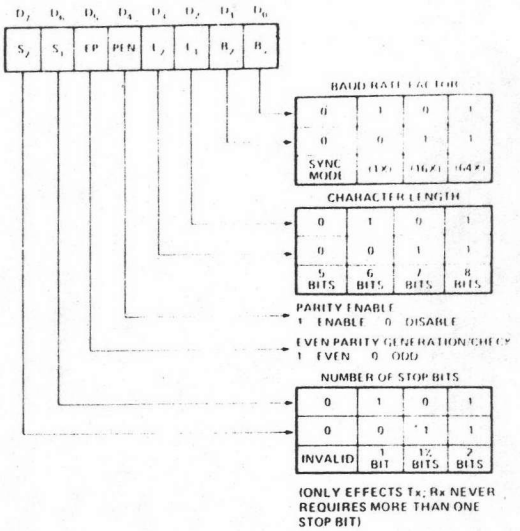


Figure 6. Mode Instruction Format, Asynchronous Mode

Asynchronous Mode (Transmission)

Whenever a data character is sent by the CPU the 8251A automatically adds a Start bit (low level) followed by the data bits (least significant bit first), and the programmed number of Stop bits to each character. Also, an even or odd Parity bit is inserted prior to the Stop bit(s), as defined by the Mode Instruction. The character is then transmitted as a serial data stream on the TxD output. The serial data is shifted out on the falling edge of $\overline{TxC}$ at a rate equal to 1, 1/16, or 1/64 that of the $\overline{TxC}$, as defined by the Mode Instruction. BREAK characters can be continuously sent to the TxD if commanded to do so.

When no data characters have been loaded into the 8251A the TxD output remains "high" (marking) unless a Break (continuously low) has been programmed.

Asynchronous Mode (Receive)

The RxD line is normally high. A falling edge on this line triggers the beginning of a START bit. The validity of this START bit is checked by again strobing this bit at its nominal center (16X or 64X mode only). If a low is detected again, it is a valid START bit, and the bit counter will start counting. The bit counter thus locates the center of the data bits, the parity bit (if it exists) and the stop bits. If parity error occurs, the parity error flag is set. Data and parity bits are sampled on the RxD pin with the rising edge of $\overline{RxC}$. If a low level is detected as the STOP bit, the Framing Error flag will be set. The STOP bit signals the end of a character. Note that the *receiver* requires only *one* stop bit, regardless of the number of stop bits programmed. This character is then loaded into the parallel I/O buffer of the 8251A. The RxRDY pin is raised to signal the CPU that a character is ready to be fetched. If a previous character has not been fetched by the CPU, the present character replaces it in the I/O buffer, and the OVERRUN Error flag is raised (thus the previous character is lost). All of the error flags can be reset by an Error Reset Instruction. The occurrence of any of these errors will not affect the operation of the

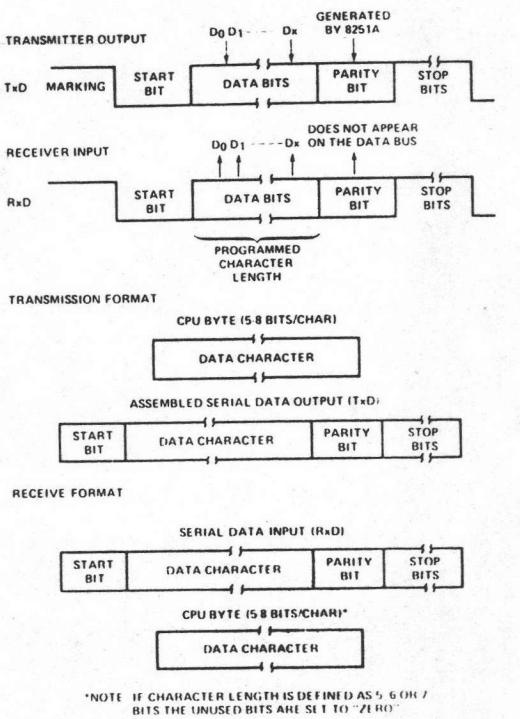
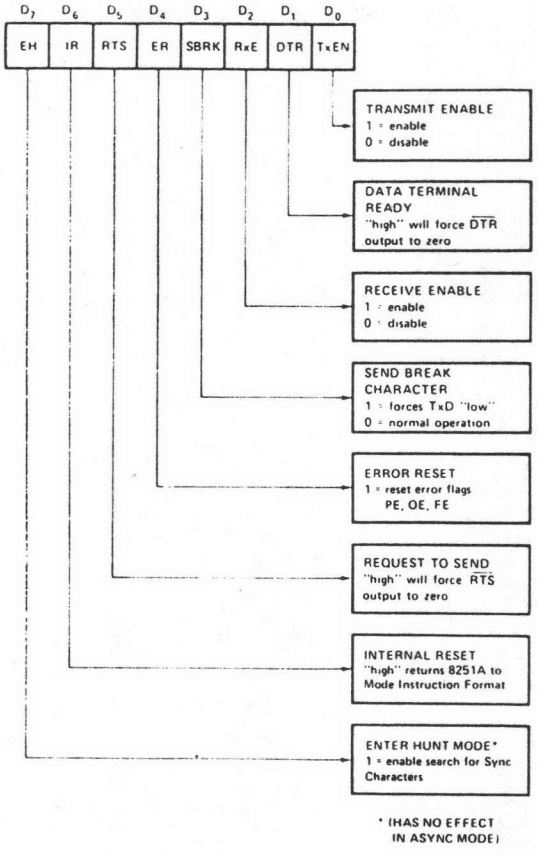


Figure 7. Asynchronous Mode

COMMAND INSTRUCTION DEFINITION

Once the functional definition of the 8251A has been programmed by the Mode Instruction and the Sync Characters are loaded (if in Sync Mode) then the device is ready to be used for data communication. The Command Instruction controls the actual operation of the selected format. Functions such as: Enable Transmit/Receive, Error Reset and Modem Controls are provided by the Command Instruction.

Once the Mode Instruction has been written into the 8251A and Sync characters inserted, if necessary, then all further "control writes" ($C/\overline{D}$ = 1) will load a Command Instruction. A Reset Operation (internal or external) will return the 8251A to the Mode Instruction format.



Note: Error Reset must be performed whenever RxEnable and Enter Hunt are programmed.

Figure 10. Command Instruction Format

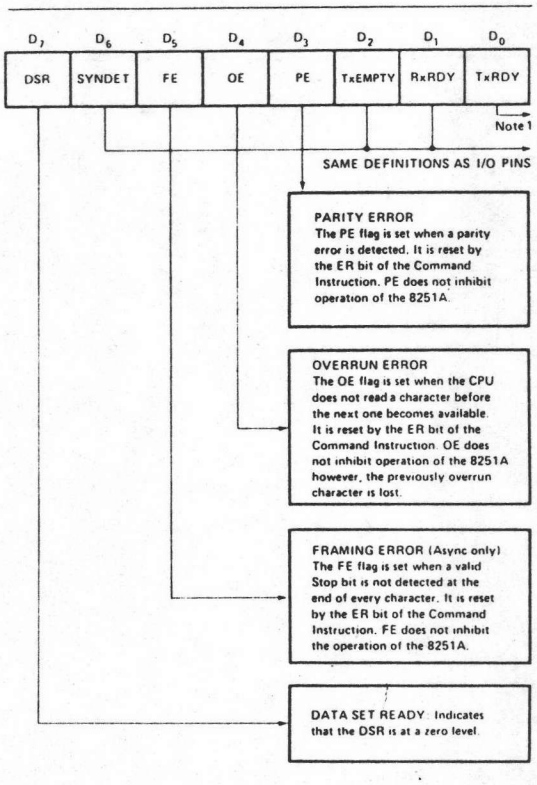
STATUS READ DEFINITION

In data communication systems it is often necessary to examine the "status" of the active device to ascertain if errors have occurred or other conditions that require the processor's attention. The 8251A has facilities that allow the programmer to "read" the status of the device at any time during the functional operation. (The status update is inhibited during status read).

A normal "read" command is issued by the CPU with $C/\overline{D}$ = 1 to accomplish this function.

Some of the bits in the Status Read Format have identical meanings to external output pins so that the 8251A can be used in a completely Polled environment or in an interrupt driven environment. TxRDY is an exception.

Note that status update can have a maximum delay of 28 clock periods from the actual event affecting the status.



Note 1: TxRDY status bit has different meanings from the TxRDY output pin. The former is not conditioned by $\overline{CTS}$ and TxEN; the latter is conditioned by both $\overline{CTS}$ and TxEN.

i.e. TxRDY status bit = DB Buffer Empty

TxRDY pin out = DB Buffer Empty · (CTS = 0) · (TxEN = 1)

Figure 11. Status Read Format

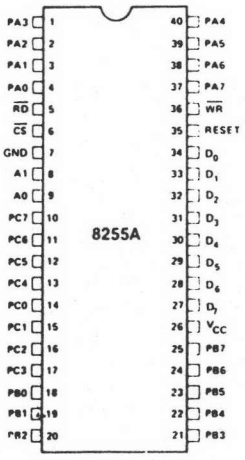
intel

8255A/8255A-5
PROGRAMMABLE PERIPHERAL INTERFACE

- MCS-85™ Compatible 8255A-5
- 24 Programmable I/O Pins
- Completely TTL Compatible
- Fully Compatible with Intel® Microprocessor Families
- Improved Timing Characteristics
- Direct Bit Set/Reset Capability Easing Control Application Interface
- 40-Pin Dual In-Line Package
- Reduces System Package Count
- Improved DC Driving Capability

The Intel® 8255A is a general purpose programmable I/O device designed for use with Intel® microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

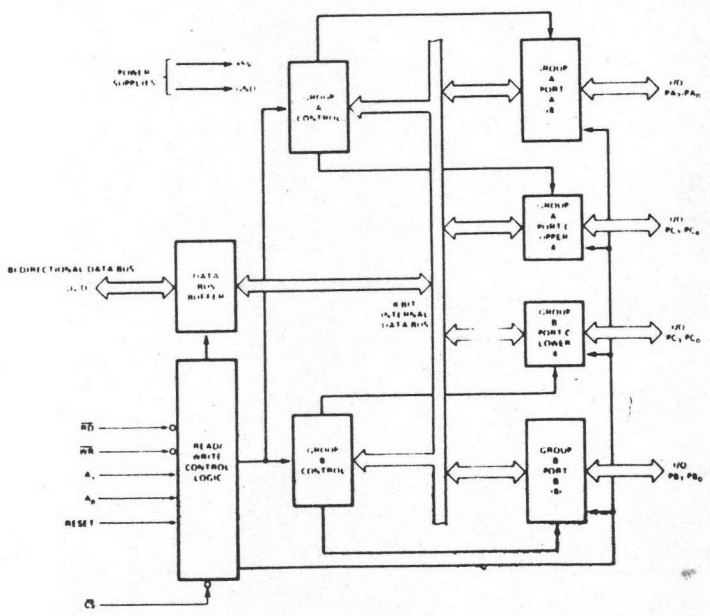
PIN CONFIGURATION



PIN NAMES

D_7–D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS

8255A BLOCK DIAGRAM



8255A FUNCTIONAL DESCRIPTION

General

The 8255A is a programmable peripheral interface (PPI) device designed for use in Intel® microcomputer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 8255A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 8255A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

($\overline{CS}$)

Chip Select. A "low" on this input pin enables the communiction between the 8255A and the CPU.

($\overline{RD}$)

Read. A "low" on this input pin enables the 8255A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 8255A.

($\overline{WR}$)

Write. A "low" on this input pin enables the CPU to write data or control words into the 8255A.

(A_0 and A_1)

Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus (A_0 and A_1).

8255A BASIC OPERATION

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL
					DISABLE FUNCTION
X	X	X	X	1	DATA BUS → 3-STATE
1	1	0	1	0	ILLEGAL CONDITION
X	X	1	1	0	DATA BUS → 3-STATE

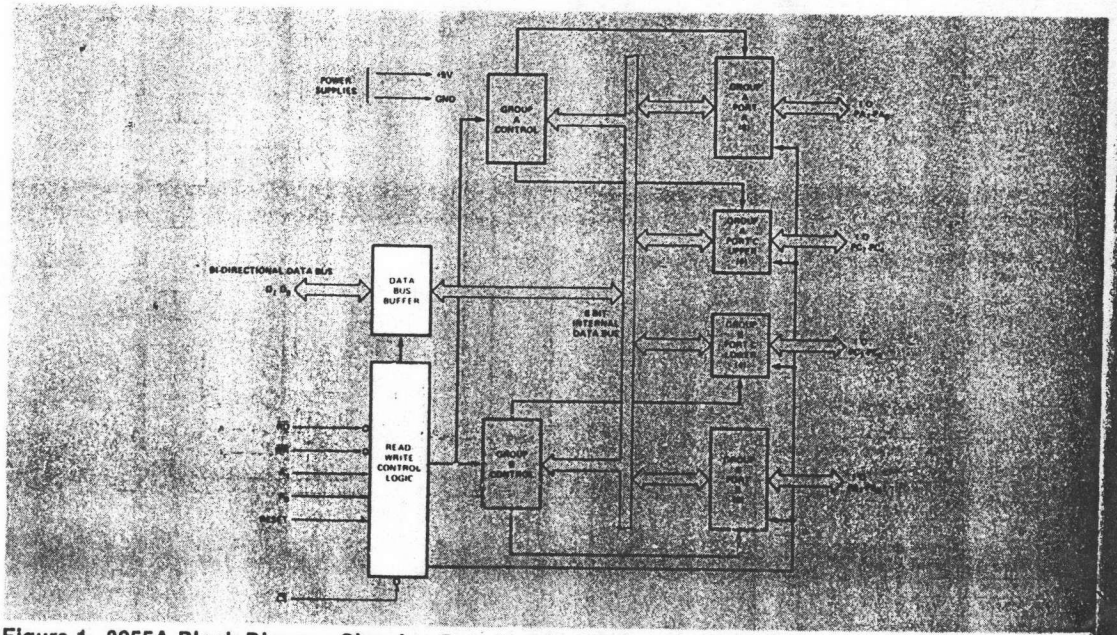


Figure 1. 8255A Block Diagram Showing Data Bus Buffer and Read/Write Control Logic Functions

(RESET)

Reset. A "high on this input clears the control register and all ports (A, C, C) are set to the input mode.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 8255A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 8255.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A – Port A and Port C upper (C7-C4)
Control Group B – Port B and Port C lower (C3-C0)

The Control Word Register can Only be written into. No Read operation of the Control Word Register is allowed.

Ports A, B, and C

The 8255A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255A.

Port A. One 8-bit data output latch/buffer and one 8-bit data input latch.

Port B. One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C. One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

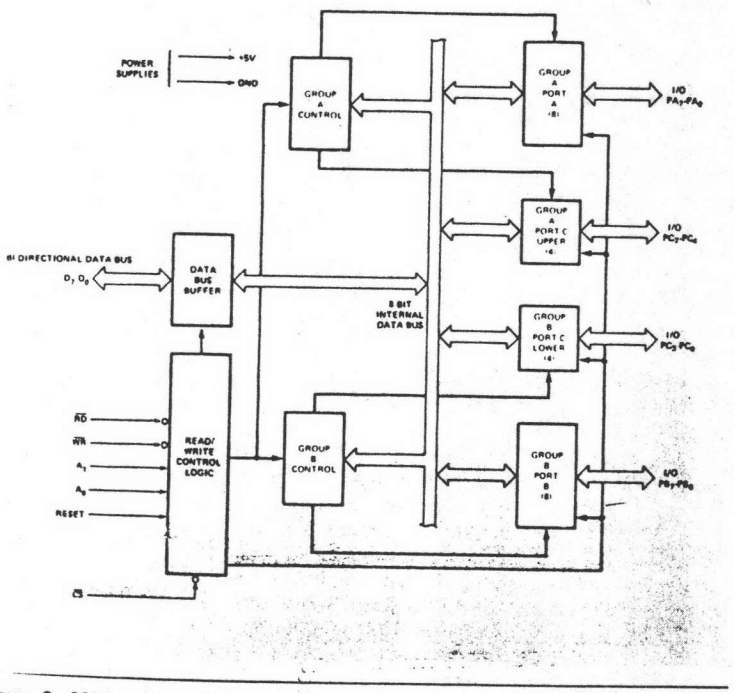
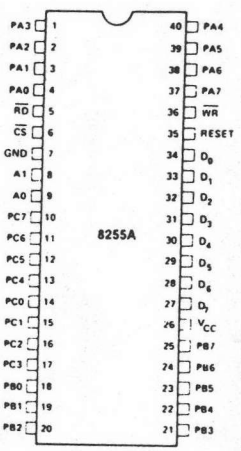


Figure 2. 8225A Block Diagram Showing Group A and Group B Control Functions

PIN CONFIGURATION



PIN NAMES

D_7-D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	0 VOLTS

8255A OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0 – Basic Input/Output
Mode 1 – Strobed Input/Output
Mode 2 – Bi-Directional Bus

When the reset input goes "high" all ports will be set to the input mode (i.e., all 24 lines will be in the high impedance state). After the reset is removed the 8255A can remain in the input mode with no additional initialization required. During the execution of the system program any of the other modes may be selected using a single output instruction. This allows a single 8255A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

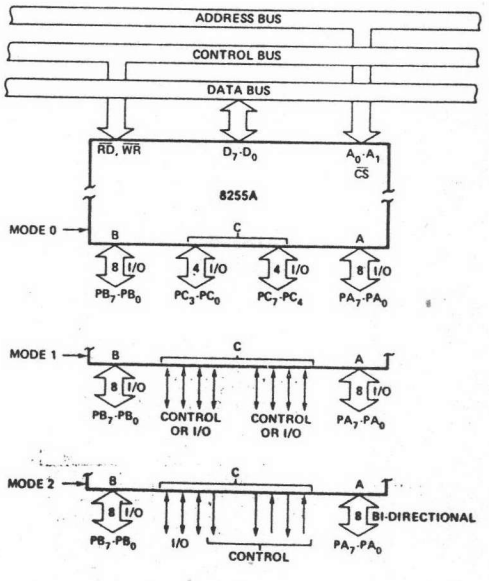


Figure 3. Basic Mode Definitions and Bus Interface

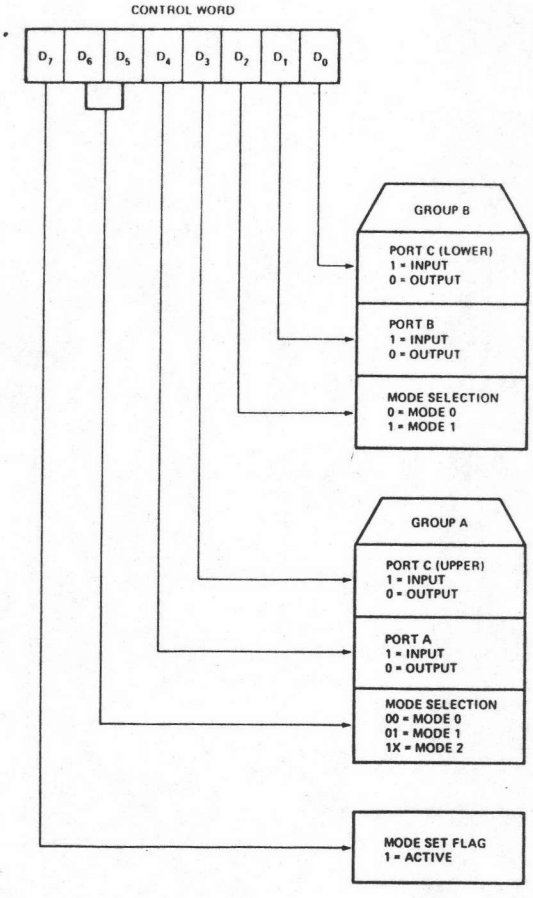


Figure 4. Mode Definition Format

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 8255A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . . -65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . -0.5V to +7V
Power Dissipation . . . . . 1 Watt

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ±5%; GND = 0V

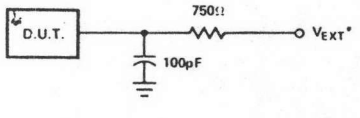
SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL} (DB)	Output Low Voltage (Data Bus)		0.45	V	I_{OL} = 2.5mA
V_{OL}(PER)	Output Low Voltage (Peripheral Port)		0.45	V	I_{OL} = 1.7mA
V_{OH}(DB)	Output High Voltage (Data Bus)	2.4		V	I_{OH} = -400μA
V_{OH}(PER)	Output High Voltage (Peripheral Port)	2.4		V	I_{OH} = -200μA
I_{DAR}[1]	Darlington Drive Current	-1.0	-4.0	mA	R_{EXT} = 750Ω; V_{EXT} = 1.5V
I_{CC}	Power Supply Current		120	mA	
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to 0V

Note 1: Available on any 8 pins from Port B and C.

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND



*V_{EXT} is set at various voltages during testing to guarantee the specification.

Figure 24. Test Load Circuit (for dB)

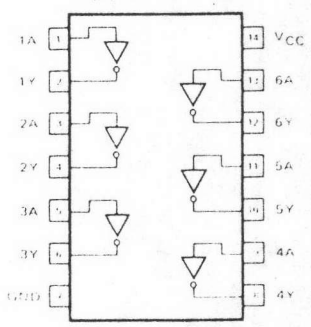
HEX INVERTER 54/7404

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54H	F,W	74H	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

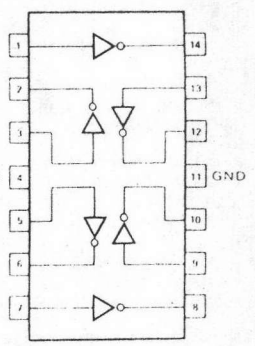
PIN CONFIGURATION

74,74H, 54/74LS,54S
A,F,W PACKAGE



Positive logic: $Y = \overline{A}$

54,54H
W PACKAGE



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L = 15pF, R_L = 400Ω			54/74H C_L = 25pF, R_L = 280Ω			54/74LS C_L = 15pF, R_L = 2kΩ			54/74S C_L = 15pF, R_L = 280Ω			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time t_{PLH} Low-to-high		12	22		6	10		5	15	2	3 (C_L = 50pF: 4.5)	4.5	ns
t_{PHL} High-to-low		8	15		6.5	10		9	15	2	3 (C_L = 50pF: 5)	5	ns

Load circuit and typical waveforms are shown at the front of section.

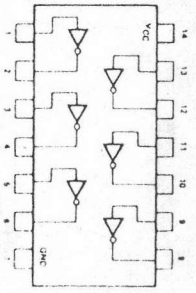
HEX INVERTER BUFFER/DRIVER 54/7406

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F

PIN CONFIGURATION

A,F,W PACKAGE



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L = 15pF, R_L = 110Ω			
PARAMETER	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time t_{PLH} Low-to-high		10	15	ns
t_{PHL} High-to-low				

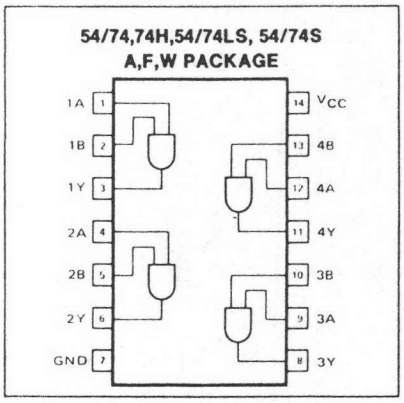
Load circuit and typical waveforms are shown at the front of section.

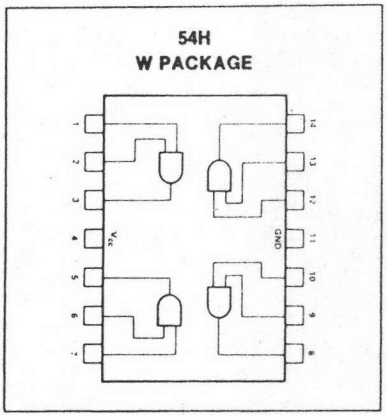
QUAD 2-INPUT AND GATE — 54/7408

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54H	F,W	74H	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

PIN CONFIGURATION





SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L = 15pF, R_L = 400Ω			54/74H C_L = 25pF, R_L = 280Ω			54/74LS C_L = 15pF, R_L = 2kΩ			54/74S C_L = 15pF, R_L = 280Ω			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time													
t_{PLH} Low-to-high		17.5	27		7.6	12		8.5	15		4.5 (C_L = 50pF: 6)	7	ns
t_{PHL} High-to-low		12	19		8.8	12		8	20		5 (C_L = 50pF: 7.5)	7.5	ns

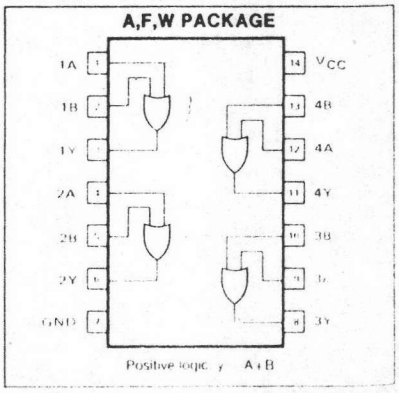
Load circuit and typical waveforms are shown at the front of section.

QUAD 2-INPUT OR GATE — 54/7432

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54LS	F,W	74LS	A,F

PIN CONFIGURATION



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L 15pF, R_L 400Ω			54/74LS C_L = 15pF, R_L = 2kΩ			
PARAMETER	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time							
t_{PLH} Low-to-high		10	15		9	22	ns
t_{PHL} High-to-low		14	22		9	22	ns

Load circuit and typical waveforms are shown at the front of section.

DECADE COUNTER 54/7490

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54LS	F,W	74LS	A,F

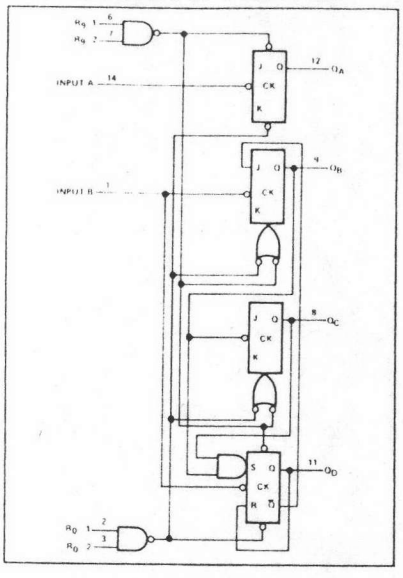
DESCRIPTION

This monolithic counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five.

The 54/74LS90 also has a gated zero reset and gated set-to-nine inputs for use in BCD nine's complement applications.

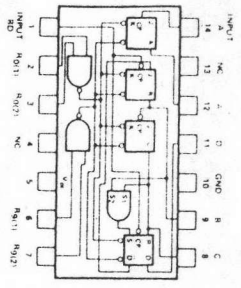
To use its maximum count length of this counter, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the function table. A symmetrical divide-by-ten count can be obtained by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

BLOCK DIAGRAM 54LS/74LS

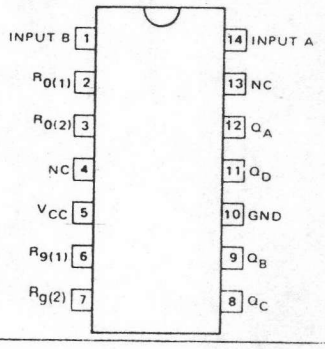


PIN CONFIGURATION

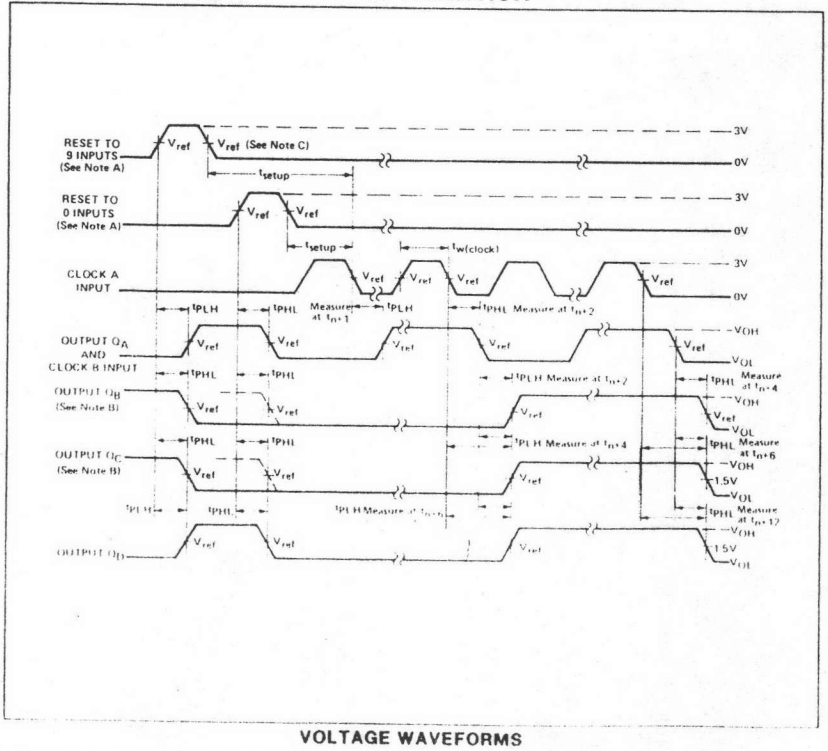
54/74
A,F,W PACKAGE



54LS/74LS
A,F,W PACKAGE



PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

A. Each reset input is tested separately with the other reset at 4.5 V.
B. Reference waveforms are shown with dashed lines.
C. V_{ref} = 1.5 V.
Load circuit is shown at front of section (for totem pole outputs).

DECADE COUNTER 54/7490

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L = 15pF R_L = 400Ω			54/74LS C_L = 15pF R_L = 2kΩ			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Count} Count frequency			10	18					MHz
	A	Q_A				32	42		
	B	Q_B				16			
$t_{w(Clock)}$ Width of clock pulse			50						ns
	A	Q				15			
	B	Q				30			
	Reset	Q				15			
$t_{w(Reset)}$ Width of reset pulse			50			25			ns
Propagation delay time									
t_{PLH} Low-to-high	Input Count Pulse	Q_C		60	100				ns
t_{PHL} High-to-low				60	100				
t_{PLH} Low-to-high	A	Q_A					10	16	
t_{PHL} High-to-low							12	18	
t_{PLH} Low-to-high	A	Q_D					32	48	
t_{PHL} High-to-low							34	50	
t_{PLH} Low-to-high	B	Q_B					10	16	
t_{PHL} High-to-low							14	21	
t_{PLH} Low-to-high	B	Q_C					21	32	
t_{PHL} High-to-low							23	35	
t_{PLH} Low-to-high	B	Q_D					21	32	
t_{PHL} High-to-low							23	35	
t_{PHL} High-to-low	Set-to-0	Any					26	40	
t_{PLH} Low-to-high	Set-to-9	Q_A,Q_D					20	30	
t_{PHL} High-to-low	Set-to-9	Q_B,Q_C					26	40	

Load circuit and typical waveforms shown at front of section.

BCD COUNT SEQUENCE (See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2) (See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

NOTES:
A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. Output Q_A is connected to input B.
D. H = high level, L = low level, X = irrelevant.

DIVIDE-BY-TWELVE COUNTER

54/7492

SPEED/PACKAGE AVAILABILITY

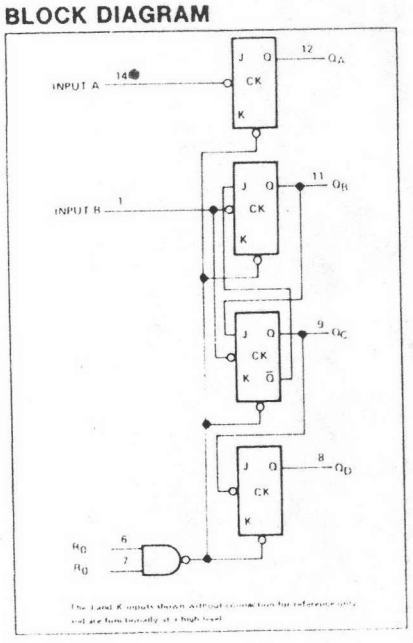
54 F,W 74 A,F

DESCRIPTION

This monolithic counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three stage binary counter for which the count cycle length is divide-by-six.

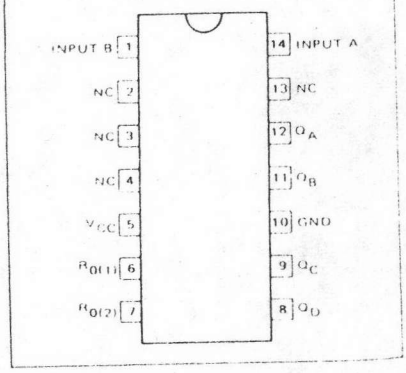
To use its maximum count length of this counter, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the function table.

BLOCK DIAGRAM

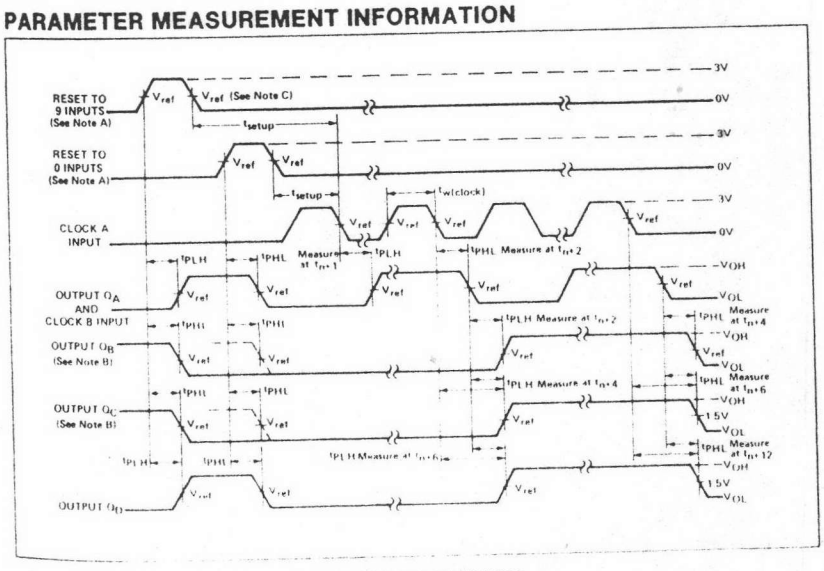


PIN CONFIGURATION

A,F,W PACKAGE



PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES:

A. Each reset input is tested separately with the other reset at 4.5 V.

B. Reference waveforms are shown with dashed lines.

C. V_{ref} = 1.5 V

Load circuit shown at front of book (for indicated application)

DIVIDE-BY-TWELVE COUNTER 54/7492

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L = 15pF R_L = 400			54/74LS C_L = 15pF R_L = 2k			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Count} Count frequency			10	18					MHx
	A	Q_A				32	42		
	B	Q_B				16			
t_w Width of pulse	A	Q				15			ns
	B	Q				30			
	Reset	Q				15			
t_{Setup} Input setup time						25			ns
Propagation delay time									
t_{PLH} Low-to-high	Input Count Pulse	Q_D		60	100				ns
t_{PHL} High-to-low				60	100				
t_{PLH} Low-to-high	A	Q_A					10	16	
t_{PHL} High-to-low							12	18	
t_{PLH} Low-to-high	A	Q_D					32	48	
t_{PHL} High-to-low							34	50	
t_{PLH} Low-to-high	B	Q_B					10	16	
t_{PHL} High-to-low							14	21	
t_{PLH} Low-to-high	B	Q_C					10	16	
t_{PHL} High-to-low							14	21	
t_{PLH} Low-to-high	B	Q_D					21	32	
t_{PHL} High-to-low							23	35	
t_{PHL} High-to-low	Set-to-0	Any					26	40	

RESET/COUNT FUNCTION TABLE

RESET INPUTS		OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

COUNT SEQUENCE

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

Output Q_A is connected to Input B.

4-BIT BINARY COUNTER

SPEED/PACKAGE AVAILABILITY

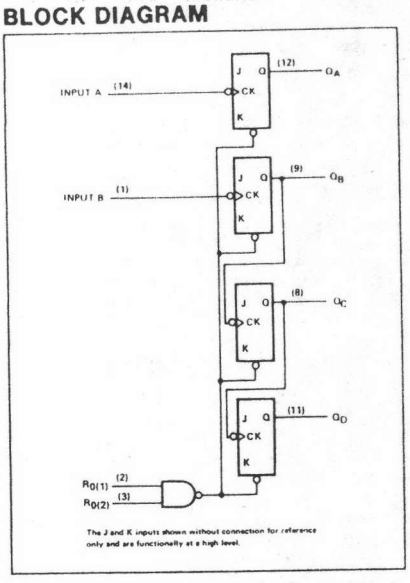
54	A,F,W	74	A,F
54LS	F,W	74LS	A,F

DESCRIPTION

This monolithic counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three stage binary counter for which the count cycle length is divide-by-eight.

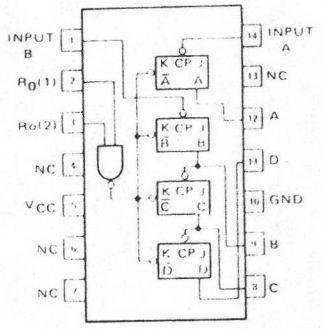
To use its maximum count length of this counter, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the function table.

BLOCK DIAGRAM

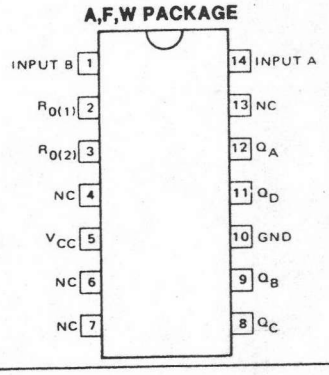


PIN CONFIGURATION

54/74
A,F,W PACKAGE



54/74LS
A,F,W PACKAGE



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L = 15pF, R_L = 400Ω			54/74LS C_L = 15pF, R_L = 2kΩ			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Count}	Count frequency	A	Q_A	10	18		32	42		MHz
		B	Q_B				16			
t_w	Width of pulse	A	Q	50			15			ns
		B	Q				30			
		Reset	Q	50			15			
t_{Setup}	Input setup time						25			ns
Propagation delay time										
t_{PLH}	Low-to-high	Input Count Pulse	Q_D		75	135				ns
t_{PHL}	High-to-low				75	135				
t_{PLH}	Low-to-high	A	Q_A					10	16	
t_{PHL}	High-to-low							12	18	
t_{PLH}	Low-to-high	A	Q_D					46	70	
t_{PHL}	High-to-low							46	70	
t_{PLH}	Low-to-high	B	Q_B					10	16	
t_{PHL}	High-to-low							14	21	
t_{PLH}	Low-to-high	B	Q_C					21	32	
t_{PHL}	High-to-low							23	35	
t_{PLH}	Low-to-high	B	Q_D					34	51	
t_{PHL}	High-to-low							34	51	
t_{PHL}	High-to-low	Set-to-0	Any					26	40	

COUNT SEQUENCE

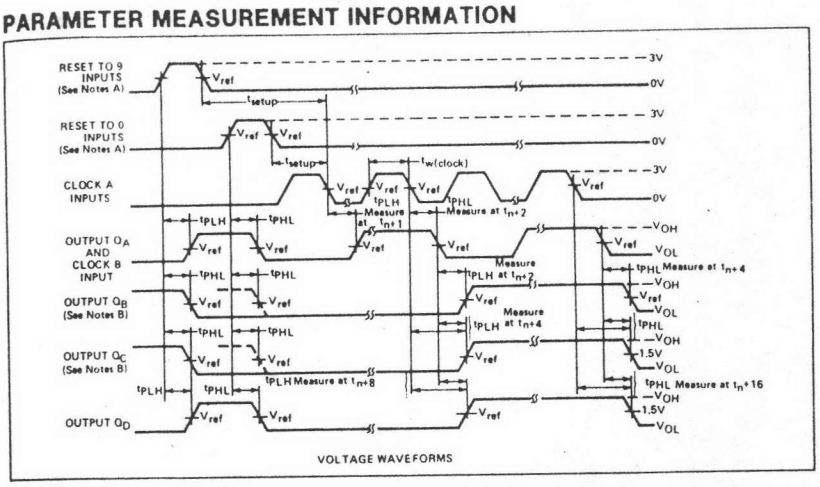
COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Output Q_A is connected to input B

RESET/COUNT FUNCTION TABLE

RESET INPUTS		OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES:

A. Each reset input is tested separately with the other reset at 4.5 V.

B. Reference waveforms are shown with dashed lines.

C. $V_{ref} = 1.8$ V.

Load circuit shown at front of book (for totem pole outputs).

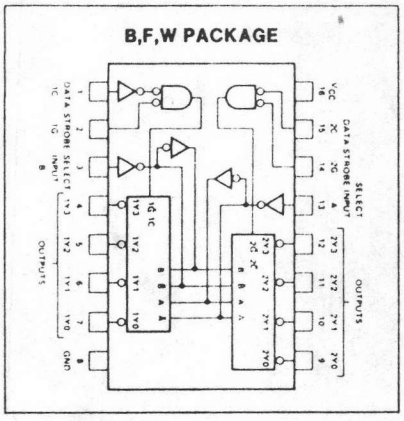
DUAL 2-LINE TO 4-LINE DECODER/DEMULTIPLEXER 54/74155

SPEED/PACKAGE AVAILABILITY

54 F,W 74 B,F

PIN CONFIGURATION

B,F,W PACKAGE



TRUTH TABLE

2-LINE TO 4-LINE DECODER							
INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

1-LINE TO 4-LINE DEMULTIPLEXER							
INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

†C = inputs 1C and 2C connected together
‡G = inputs 1G and 2G connected together

3-LINE TO 8-LINE DECODER TO 1-LINE TO 8-LINE DEMULTIPLEXER											
INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

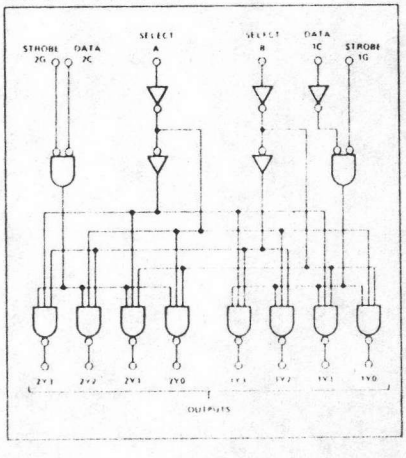
†C = inputs 1C and 2C connected together
‡G = inputs 1G and 2G connected together

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L = 15pF, R_L = 400Ω				
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	LEVELS OF LOGIC	UNIT
Propagation delay time							
t_{PLH} Low-to-high	A,B,2C, 1G,2G	Y		13	20	2	ns
t_{PHL} High-to-low				18	27		
t_{PLH} Low-to-high	A,B	Y		21	32	3	
t_{PHL} High-to-low				21	32		
t_{PLH} Low-to-high	1C	Y		16	24	3	
t_{PHL} High-to-low				20	30		

Load circuit and typical waveforms are shown at the front of section

LOGIC DIAGRAM



QUAD D-TYPE EDGE-TRIGGERED FLIP-FLOP 54/74175

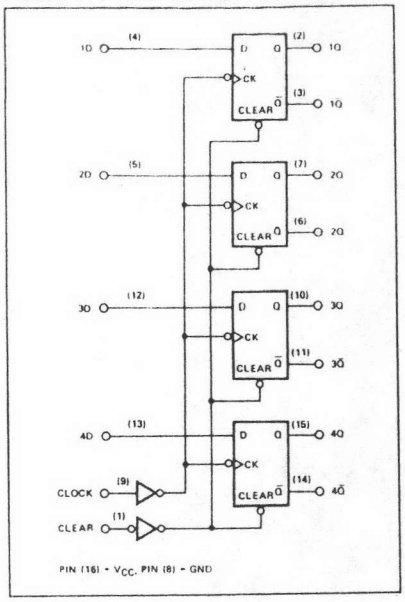
SPEED/PACKAGE AVAILABILITY

54	F,W	74	B
54LS	F,W	74LS	B
		74S	B

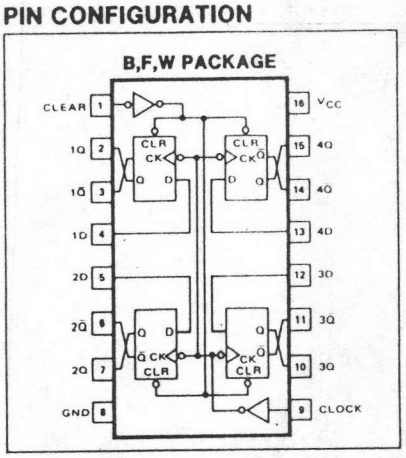
DESCRIPTION

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



TRUTH TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L = 15pF R_L = 400Ω			54/74LS C_L = 15pF R_L = 2kΩ			54/74S C_L = 15pF R_L = 280Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			25	35		30	40		75	110		MHz
t_w	Width of pulse									12			ns
	Clock			20			20						
	Clear												
t_{Setup}	Input setup time												ns
	Data			20			20			8			
	Clear inactive			25			25			15			
t_{Hold}	Input hold time			0			5			2			ns
Propagation delay time													
t_{PLH}	Low-to-high	Clear			16	25		16	25				ns
t_{PHL}	High-to-low				23	35		23	35				
t_{PLH}	Low-to-high	Clock			20	30		20	30		9	12	
t_{PHL}	High-to-low				21	30		21	35		11	17	
t_{PLH}	Low-to-high	Clear	$\bar{Q}$								13	15	
t_{PHL}	High-to-low	Clear	Q								13	22	

Load circuit and typical waveforms are shown at the front of section.

QUAD LINE DRIVER

MC1488

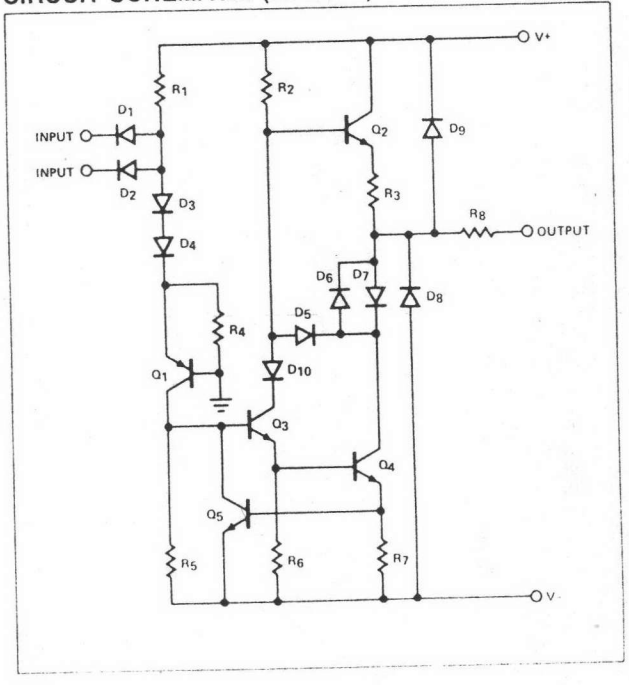
FEATURES

- CURRENT LIMITED OUTPUT: ±10mA TYP
- POWER-OFF SOURCE IMPEDANCE: 300Ω MIN
- SIMPLE SLEW RATE CONTROL WITH EXTERNAL CAPACITOR
- FLEXIBLE OPERATING SUPPLY RANGE
- INPUTS ARE DTL/TTL COMPATIBLE

ABSOLUTE MAXIMUM RATINGS (Note 1)

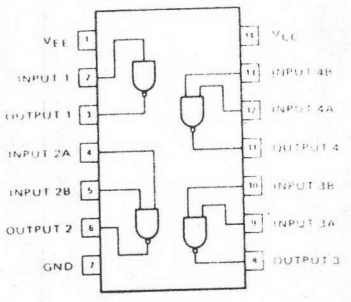
Supply Voltage V+	+15V
V−	−15V
Input Voltage (VIN)	−15V ≤ VIN ≤ 7.0V
Output Voltage	±15V
Power Dissipation	1000mW
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +175°C
Lead Temperature (Soldering, 10 sec)	300°C

CIRCUIT SCHEMATIC (¼CIRCUIT)

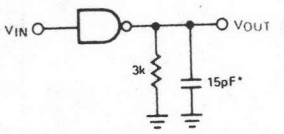


PIN CONFIGURATION

F PACKAGE

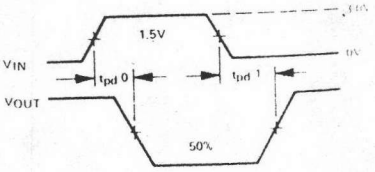


AC LOAD CIRCUIT



*CL INCLUDES PROBE AND JIG CAPACITANCE

SWITCHING WAVEFORMS



tr and tf ARE MEASURED BETWEEN 10% AND 90% OF THE OUTPUT

SWITCHING CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX
Propagation Delay to "1" (tpd1)	RL = 3.0kΩ, CL = 15pF, TA = 25°C		230	300
Propagation Delay to "0" (tpd0)	RL = 3.0kΩ, CL = 15pF, TA = 25°C		70	175
Rise Time (tr)	RL = 3.0kΩ, CL = 15pF, TA = 25°C		75	100
Fall Time (tf)	RL = 3.0kΩ, CL = 15pF, TA = 25°C		40	75

NOTES

1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. These specifications apply for V+ = +9.0V ± 1%, V− = −9.0V ± 1%, TA = 0°C to +75°C unless otherwise noted. All typicals are for V+ = +9.0V, V− = −9.0V, TA = 25°C.

QUAD LINE DRIVER — MC1488

APPLICATIONS

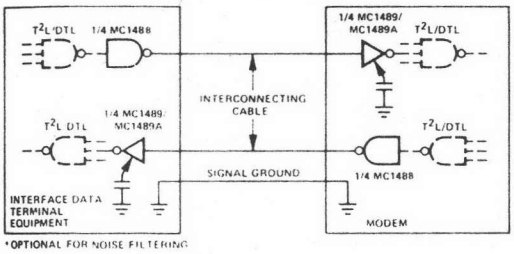
By connecting a capacitor to each driver output the slew rate can be controlled utilizing the output current limiting characteristics of the MC1488. For a set slew rate the appropriate capacitor value may be calculated using the following relationship

$$C = I_{SC}\,(\Delta T/\Delta V)$$

where C is the required capacitor, I_{SC} is the short circuit current value, and $\Delta V/\Delta T$ is the slew rate.

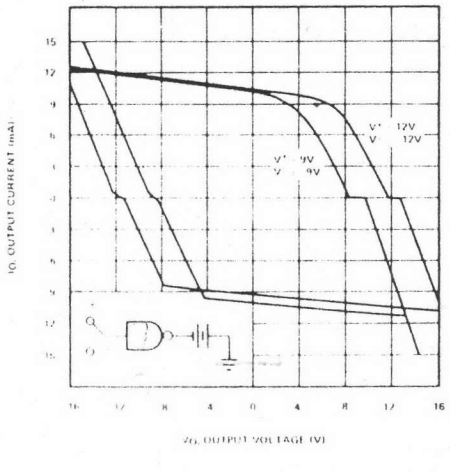
RS232C specifies that the output slew rate must not exceed 30V per microsecond. Using the worst case output short circuit current of 12mA in the above equation, calculations result in a required capacitor of 400pF connected to each output.

RS232C DATA TRANSMISSION



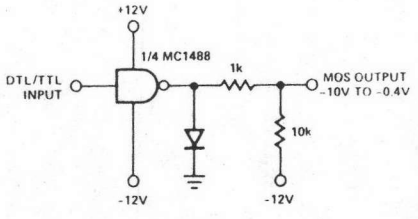
CHARACTERISTIC CURVES

OUTPUT VOLTAGE AND CURRENT-LIMITING CHARACTERISTICS

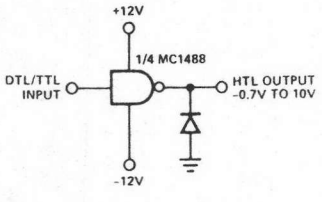


TYPICAL APPLICATIONS

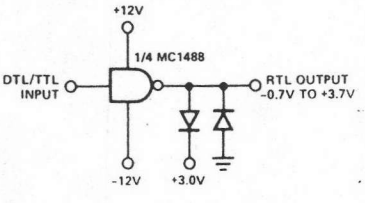
DTL/TTL-TO-MOS TRANSLATOR



DTL/TTL-TO-HTL TRANSLATOR



DTL/TTL-TO-RTL TRANSLATOR



QUAD LINE RECEIVERS

MC1489/MC1489A

MC1489F MC1489A

FEATURES

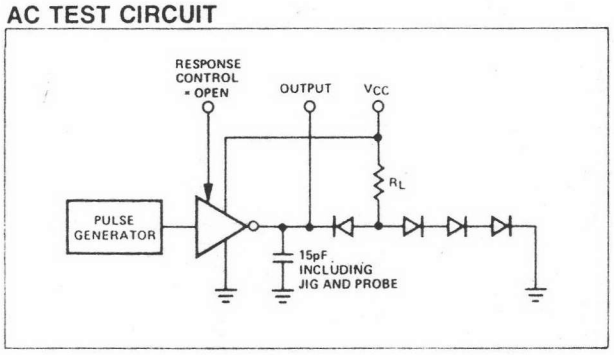
- FOUR TOTALLY SEPARATE RECEIVERS PER PACKAGE
- PROGRAMMABLE THRESHOLD
- BUILT-IN INPUT THRESHOLD HYSTERESIS
- "FAIL SAFE" OPERATING MODE
- INPUTS WITHSTAND ±30V

ABSOLUTE MAXIMUM RATINGS

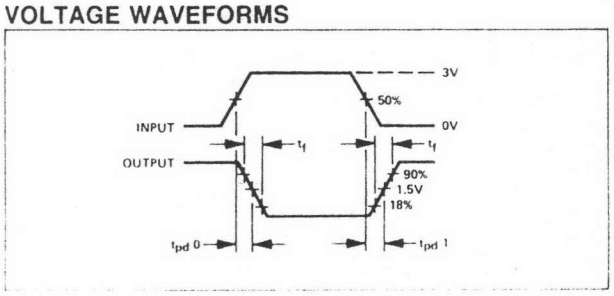
The following apply for TA = 25°C unless otherwise specified.

Power Supply Voltage	10V
Input Voltage Range	±30V
Output Load Current	20mA
Power Dissipation	1W
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +175°C

AC TEST CIRCUIT

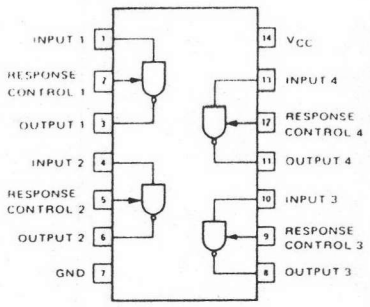


VOLTAGE WAVEFORMS

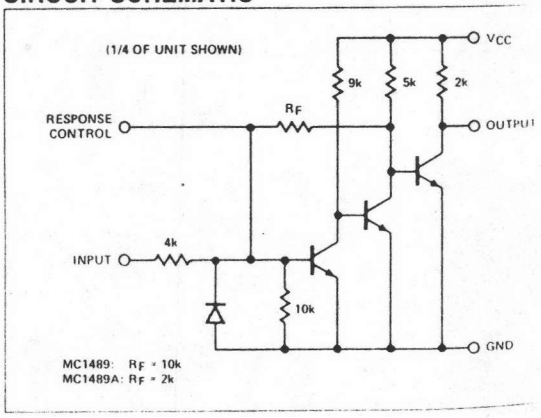


PIN CONFIGURATION

F PACKAGE



CIRCUIT SCHEMATIC

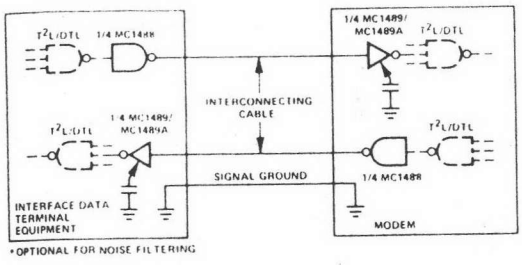


SWITCHING CHARACTERISTICS MC1489/MC1489A V_{CC} = 5.0V ±1%, T_A = 25°C

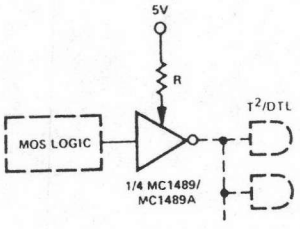
PARAMETER	CONDITIONS	MC1489			MC1489A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input to Output "High" Propagation Delay (t_{pd1})	R_L = 3.9k (AC Test Circuit)		25	85		25	85	
Input to Output "Low" Propagation Delay (t_{pd0})	R_L = 390Ω (AC Test Circuit)		20	50		20	50	
Output Rise time	R_L = 3.9k (AC Test Circuit)		110	175		110	175	
Output Fall Time	R_L = 390Ω (AC Test Circuit)		9	20		9	20	

TYPICAL APPLICATIONS

RS232C DATA TRANSMISSION



MOS TO T²L/DTL TRANSLATOR



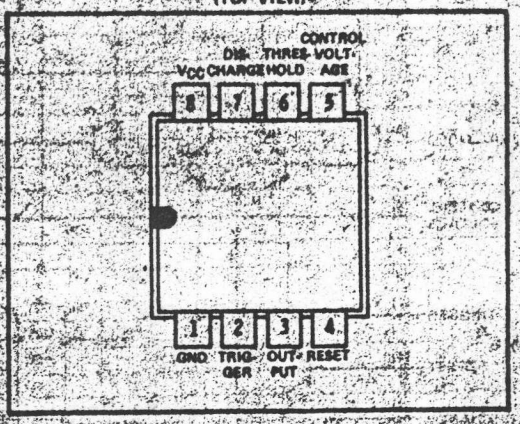
LINEAR INTEGRATED CIRCUITS

TYPES SN52555, SN72555 PRECISION TIMERS

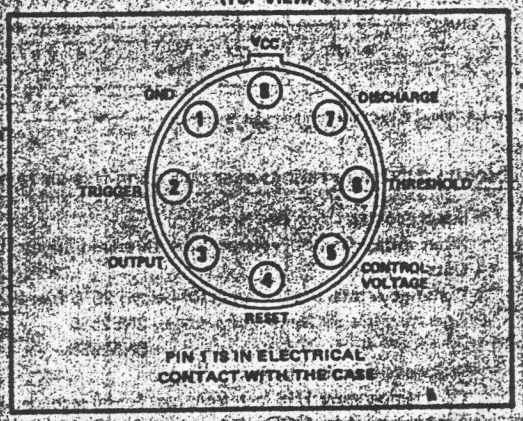
BULLETIN NO. DL-S 7312063, SEPTEMBER 1973

- Timing from Microseconds to Hours
- Astable or Monostable Operation
- Adjustable Duty Cycle
- Up to 200-mA Sink or Source Output Current
- TTL Compatible Output
- Designed to be Interchangeable with Signetics SE555/NE555

J OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



L PLUG-IN PACKAGE
(TOP VIEW)



PIN 1 IS IN ELECTRICAL CONTACT WITH THE CASE

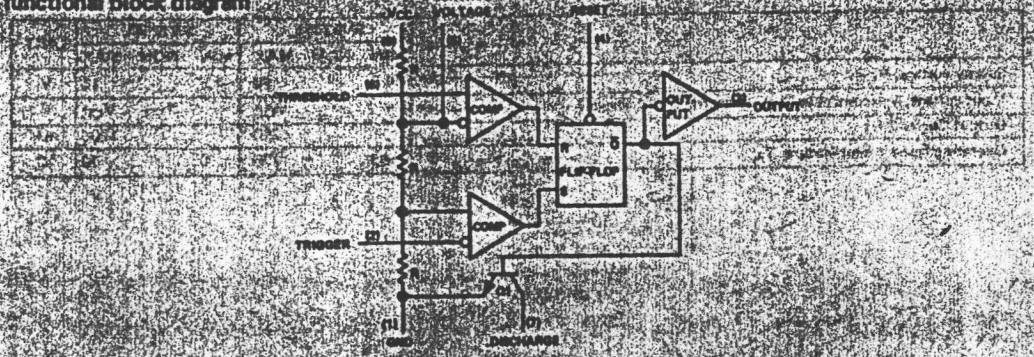
description

The SN52555 and SN72555 are monolithic timing circuits capable of producing accurate time delays or oscillation. In the time-delay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle may be independently controlled with two external resistors and a single external capacitor.

The threshold and trigger levels are normally two-thirds and one-third, respectively, of V_{CC}. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. When the threshold input rises above the threshold level, the flip-flop is reset and the output goes low. The reset input can override all other inputs and can be used to initiate a new timing cycle. When the reset input goes low, the flip-flop is reset and the output goes low. When the output is low, a low-impedance path is provided between the discharge terminal and ground.

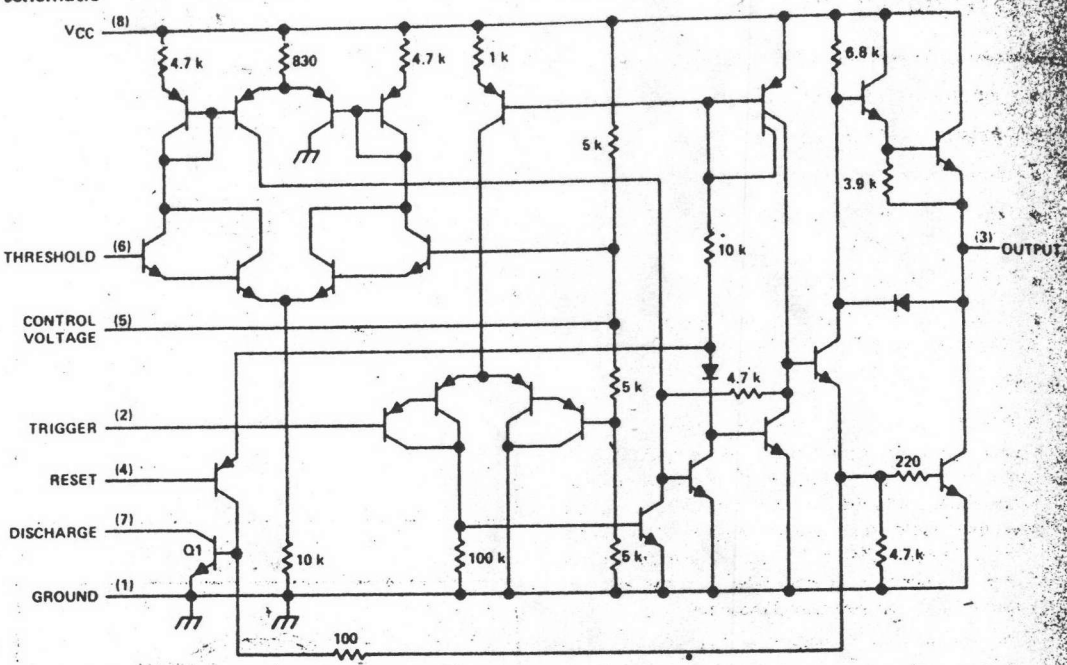
The output circuit is capable of sinking or sourcing current up to 200 milliamperes. Operation is specified for supplies of 5 to 15 volts. With a 5-volt supply, output levels are compatible with TTL inputs.

functional block diagram



3

schematic



Resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	18 V
Input voltage (control voltage, reset, threshold, trigger)	V_{CC}
Output current	±225 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	600 mW
Operating free-air temperature range: SN52555	−55°C to 125°C
SN72555	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: JP or L package	300°C
Lead temperature 1/16 inch from case for 10 seconds: P package	260°C

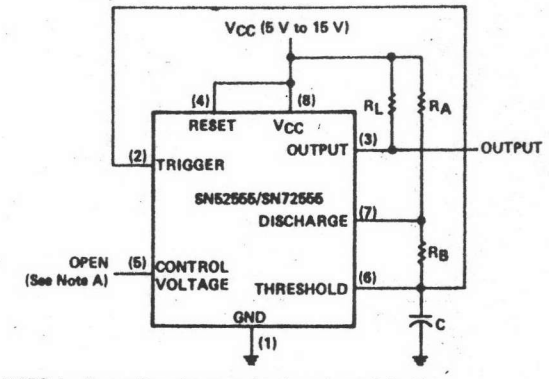
NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curve, Figure 1.

recommended operating conditions

	SN52555			SN72555			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5		18	4.5		16	V
Input voltage, V_I (control voltage, reset, threshold, trigger)			V_{CC}			V_{CC}	V
Output Current, I_O			±200			±200	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

TYPICAL APPLICATION DATA

astable operation



NOTE A: Decoupling the control voltage input (pin 5) to ground with a capacitor may improve operation. This should be evaluated for individual applications.

FIGURE 14—CIRCUIT FOR ASTABLE OPERATION

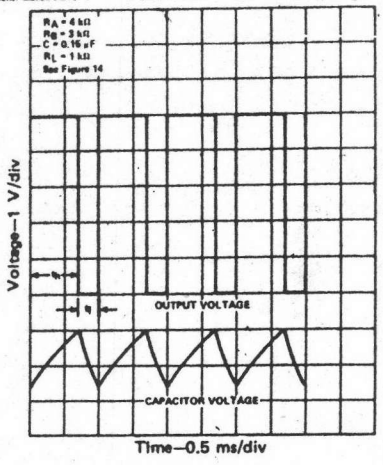


FIGURE 15—TYPICAL ASTABLE WAVEFORMS

Addition of a second resistor, R_B, to the circuit of Figure 11; as shown in Figure 14, and connection of the trigger input to the threshold input will cause the SN52555/SN72555 to self-trigger and run as a multivibrator. The capacitor C will charge through R_A and R_B then discharge through R_B only. The duty cycle may be controlled, therefore, by the values of R_A and R_B.

This astable connection results in capacitor C charging and discharging between the threshold-voltage level ($\approx 0.67 \cdot V_{CC}$) and the trigger-voltage level ($\approx 0.33 \cdot V_{CC}$). As in the monostable circuit, charge and discharge times (and therefore the frequency and duty cycle) are independent of the supply voltage.

Figure 15 shows typical waveforms generated during astable operation. The output high-level duration, t_h, is calculated as:

$$t_h = 0.693\,(R_A + R_B)C,$$

output low-level duration, t_l, as:

$$t_l = 0.693\,(R_B)C.$$

The total period is $T = t_h + t_l$ and frequency is

$$f = \frac{1}{T}, \text{ or } f = \frac{1.44}{(R_A + 2R_B)C}.$$

The frequency of oscillation may be determined by referring to the chart shown in Figure 16, which relates free-running frequency, f, to the external resistors R_A and R_B and the external capacitor C. Duty cycle, D, is determined by the values selected for R_A and R_B and may be calculated as:

$$D = \frac{R_B}{R_A + R_B}.$$

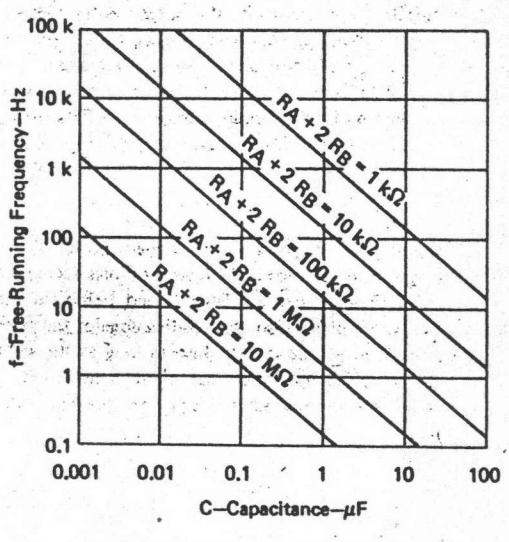


FIGURE 16—FREE-RUNNING FREQUENCY

ภาคผนวก ง

```
0000                START   ORG     0000H   ;START THE PROGRAM
                    ;   CLEAR ALL REGISTER
0000 AF                     XRA     A
0001 47                     MOV     B,A
0002 4F                     MOV     C,A
0003 57                     MOV     D,A
0004 5F                     MOV     E,A
0005 67                     MOV     H,A
0006 6F                     MOV     L,A
0007 31F00F                 LXI     SP,0FF0H        ;SET STACK POINTER
000A 2608                   MVI     H,8
000C 22FC0F                 SHLD    RLOC    ;STORE START POINTER IN READ POINTER
000F 22FE0F                 SHLD    WLOC    ;STORE START POINTER IN WRITE POINTER
0012 32F80F                 STA     CBIT    ;CLEAR MEMORY FOR CHECK BIT
0015 32F90F                 STA     DATA    ;CLEAR MEMORY FOR DATA
0018 32F30F                 STA     CONT    ;CLEAR DELAY POINTER
001B 32F10F                 STA     ELINE   ;CLEAR FLAG OF 1 LINE FROM DATAPOINT
                    ;   SET I/O PORT OF 8255(1)
                    ;   SET PORT A IS AN IN PORT
                    ;   SET PORT B IS AN IN PORT
                    ;   SET PORT C BIT 0 - 3 IS AN OUT PORT
                    ;   SET PORT C BIT 4 - 7 IS AN IN PORT
001E 3E9A                   MVI     A,9AH
0020 D317                   OUT     17H
                    ;   SET I/O PORT OF 8255(2)
                    ;   SET PORT GROUP A IS AN OUT PORT
                    ;   SET PORT GROUP B IS AN IN PORT
0022 3E83                   MVI     A,83H
0024 D30F                   OUT     0FH
0026 AF                     XRA     A       ;CLEAR REGISTER A
0027 D3FF                   OUT     0FFH    ;CLEAR PRINTER
0029 D316                   OUT     16H     ;CLEAR PRINTER
002B 3E02                   MVI     A,2     ;SET INDICATER RECIEVING DATA
002D D30C                   OUT     0CH     ;DATA-POINT TRANSMIT
                    ;   SET MODE OF 8251 IS AN ASYNCHRONOUS MODE
                    ;   SET DATA 7 OR 8 BIT
                    ;   SET BUAD RATE (X16)
                    ;   SET STOP BIT 1 OR 2
002F AF                     XRA     A
0030 D319                   OUT     19H
0032 D319                   OUT     19H
0034 D319                   OUT     19H
0036 3E40                   MVI     A,40H
0038 D319                   OUT     19H
003A DB15                   IN      15H     ;INPUT CONTROL BIT
003C E6FE                   ANI     0FEH    ;SUBPRESS CLOCK INPUT
003E F64E                   ORI     4EH     ;SET MODE FORMAT OF 8251
0040 D319                   OUT     19H     ;CONTROL CHARACTER OF 8251
0042 DB18                   IN      18H     ;CLEAR BUFFER OF 8251
0044 3E05                   MVI     A,5
0046 D319                   OUT     19H     ;SET 8251
0048 DB15                   IN      15H     ;INPUT CONTROL BIT
004A E606                   ANI     06H     ;GET ADDRESS OF DECODER
004C 0F                     RRC
004D F604                   ORI     4       ;SET ADDRESS OF DECODER
004F 57                     MOV     D,A     ;TO ADDRESS OF DECODER
0050 2F                     CMA
0051 0F                     RRC
0052 0F                     RRC
0053 E680                   ANI     80H
0055 32F90F                 STA     ASCII
0058 31F00F     PAPERC      LXI     SP,0FF0H        ;SET STACK POINTER
005B AF                     XRA     A
005C D30E                   OUT     0EH     ;READY INDICATOR
```

```
005E DB16           IN      16H     ;CHECK PAPER
0060 E610           ANI     10H     ;PAPER?
0062 CA6B00         JZ      LDATA1  ;PAPER READY
0065 CD9100         CALL    INDATA  ;INPUT SERIAL DATA
0068 C35800         JMP     PAPERC  ;CHECK PAPER
006B CD7002 LDATA1  CALL    HOLD
006E CD9100 LDATA   CALL    INDATA  ;INPUT DATA
0071 3E10           MVI     A,10H
0073 D30E           OUT     0EH     ;READY INDICATOR
0075 DB16           IN      16H     ;CHECK PAPER
0077 E610           ANI     10H     ;READY?
0079 CC7702         CZ      CPAPR   ;YES
007C 78             MOV     A,B     ;CHECK DATA
007D B1             ORA     C       ;CHECK DATA
007E CA8700         JZ      LCHECK  ;IF NO DATA
0081 CD9900         CALL    RRTN    ;IF THERE IS DATA IN MEMORY TO RRTN
0084 C36E00         JMP     LDATA
0087 DB15 LCHECK    IN      15H     ;INPUT PRINT DEMONSTRATION
0089 E608           ANI     8       ;PRINT?
008B C40C02         CNZ     CHECK   ;IF CHECK
008E C36E00         JMP     LDATA
;   START INPUT DATA FROM 8251 ROUTINE
0091 DB19 INDATA    IN      19H     ;CHRCK STATUS OF 8251
0093 E602           ANI     2       ;RECIVE READY
0095 C47F01         CNZ     WRTN    ;THERE IS DATA TO WRITE ROUTINE
0098 C9             RET
;   END INPUT SERIAL ROUTINE
;
;   START READ ( PRINT ) ROUTINE
0099 2AF10F RRTN    LHLD    RLOC    ;LOAD READ POINTER
009C 5E             MOV     E,M
009D 0B             DCX     B       ;DECREMENT NO. OF DATA IN MEMORY
009E 23             INX     H       ;INCREMENT READ POINTER
009F CD3002         CALL    CMEM    ;CHECK MEMORY FULL
00A2 22F10F         SHLD    RLOC    ;SAVE READ POINTER
;   START LOOK UP TABLE ROUTINE
00A5 1A DECODE      LDAX    D       ;DECODE DATA
00A6 FE01           CPI     1       ;CARRIAGE RETURN?
00A8 CC2701         CZ      CR      ;YES
00AB 1A             LDAX    D
00AC FE01           CPI     1
00AE C8             RZ              ;READY
00AF FE02           CPI     2       ;SPACE?
00B1 CC4401         CZ      SPACE   ;YES
00B4 FE03           CPI     3       ;BACK SPACE?
00B6 CC5F01         CZ      BACK    ;YES
00B9 FE06           CPI     6       ;TAB?
00BB CC5501         CZ      TAB     ;YES
00BE FE17           CPI     17H     ;FORM FEED?
00C0 CA5800         JZ      PAPERC  ;YES
00C3 FE07           CPI     7       ;SPECIAL CHARACTER?
00C5 C8             RZ
;   END LOOK UP TABLE ROUTINE
00C6 CD9100 CLOCK   CALL    INDATA  ;INPUT DATA ROUTINE
00C9 DB15           IN      15H
00CB E601           ANI     1       ;CLOCK?
00CD CAC600         JZ      CLOCK   ;YES
00D0 21F80F         LXI     H,DATA  ;LOAD NO. DATA TO MEMORY POINTER
00D3 34             INR     M       ;INCREMENT NO. OF DATA
00D4 AF PRINT       XRA     A
00D5 32FB0F         STA     CBIT    ;CLEAR NO. OF CHECK BIT
00D8 1A             LDAX    D       ;DECODERED DATA
00D9 0F             RRC             ;CHECK EVEN OR ODD BIT
00DA DCE200         CC      CDBIT
00DD 0F             RRC
00DE DCE200         CC      CDBIT
```

```
00E1 0F                 RRC
00E2 DC7A01             CC      CDBIT
00E5 0F                 RRC
00E6 DC7A01             CC      CDBIT
00E9 0F                 RRC
00EA DC7A01             CC      CDBIT
00ED 0F                 RRC
00EE DC7A01             CC      CDBIT
00F1 21FB0F             LXI     H,CBIT  ;SET MEMORY POINTER
00F4 7E                 MOV     A,M
00F5 2F                 CMA
00F6 0F                 RRC
00F7 E680               ANI     80H     ;ODD BIT?
00F9 77                 MOV     M,A     ;STORE IN CHECK BIT
00FA 1A                 LDAX    D       ;DECODEED DATA
00FB E67F               ANI     7FH     ;DON'T CARE SHIFT BIT
00FD B6                 ORA     M       ;SET DATA TO PRINTER
00FE 32F60F             STA     CHA1    ;DATA TO PRINTER
0101 1A                 LDAX    D       ;INPUT DATA TO PRINTER
0102 E680               ANI     80H     ;MOVE CHARACTER?
0104 C45F01             CNZ     BACK    ;NOT MOVE
0107 3AF60F             LDA     CHA1    ;DATA TO PRINTER
010A E640               ANI     40H     ;SHIFT BIT
010C CA1401             JZ      OUTD    ;TO OUTPUT ROUTINE
010F D3FF               OUT     0FFH    ;OUT SHIFT BIT TO PRINTER
0111 CD6E02             CALL    DELAY4
0114 3AF60F     OUTD    LDA     CHA1    ;DATA TO PRINTER
0117 D3FF               OUT     0FFH    ;DATA TO PRINT
0119 CD4802             CALL    DELAY1  ;DELAY FOR SOLINOID READY
011C AF                 XRA     A       ;CLAER PRINTER
011D D3FF               OUT     0FFH    ;CLEAR
011F 3AF80F             LDA     DATA    ;NO. OF DATA IN 1 LINE
0122 FE64               CPI     100     ;100 CHARACTER
0124 CC3701             CZ      CR      ;YES
0127 78                 MOV     A,B     ;CHECK MEMORY COUNTER
0128 B7                 ORA     A       ;>256?
0129 C0                 RNZ             ;IF HIGHER
012A 79                 MOV     A,C
012B FE05               CPI     5       ;LESS THAN 5?
012D F0                 RP              ;IF HIGHER
012E AF                 XRA     A
012F 32FA0F             STA     FULL    ;MEMORY FULL
0132 3E02               MVI     A,2     ;RECIEVING DATA FROM DATA POINT
0134 D30C               OUT     0CH     ;DATA-POINT TRANSMIT
0136 C9                 RET
                ;   END PRINT ROUTINE
                ;
                ;   START CARRIAGE ROUTINE
0137 3E04       CR      MVI     A,4     ;CARRIAGE RETURN OUTPUT
0139 CD6901             CALL    OUTCON  ;OUTPUT CONTROL ROUTINE
013C AF                 XRA     A       ;CLEAR NO. OF DATA
013D 32F80F             STA     DATA    ;CLEAR
0140 CD5A02             CALL    DELAY2  ;DELAY FOR CARRIAGE RETURN
0143 C9                 RET
                ;   END CARRIAGE RETURN ROUTINE
                ;
                ;   START SPACE ROUTINE
0144 3E02       SPACE   MVI     A,2     ;SPACE OUTPUT
0146 CD6901             CALL    OUTCON  ;OUTPUT CONTROL ROUTINE
0149 21F80F             LXI     H,DATA  ;SET POINTER OF DATA
014C 34                 INR     M
014D 7E                 MOV     A,M     ;CHECK DATA
014F FE64               CPI     100     ;100 CHARACTER?
0150 CC3701             CZ      CR      ;YES
0153 E1                 POP     H       ;RETURN
0154 C9                 RET
```

```
                        ;   END SPACE ROUTINE
                        ;
                        ;   START TAB ROUTINE
0155 3E08       TAB     MVI     A,8     ;TAB OUTPUT
0157 CD6901             CALL    OUTCON  ;OUTPUT CONTROL ROUTINE
015A CD6E02             CALL    DELAY4
015D E1                 POP     H
015E C9                 RET
                        ;   END TAB ROUTINE
                        ;
                        ;   START BACK SPACE ROUTINE
015F 3E01       BACK    MVI     A,1     ;BACK SPACE OUTPUT
0161 CD6901             CALL    OUTCON  ;OUTPUT CONTROL ROUTINE
0164 21F80F             LXI     H,DATA  ;SET POINTER OF DATA
0167 35                 DCR     M       ;DECREMENT NO. OF DATA
0168 C9                 RET
                        ;   END BACK SPACE ROUTINE
                        ;
                        ;   START OUTPUT CONTROL ROUTINE
0169 F5         OUTCON  PUSH    PSW     ;SAVE CONTENT OF A
016A CD4802             CALL    DELAY1  ;DELAY FOR SOLINOID RETURN
016D F1                 POP     PSW     ;LOAD CONTENT OF A
016E D316               OUT     16H     ;TO PRINTER
0170 CD4802             CALL    DELAY1  ;DELAY FOR SOLINOID READY
0173 AF                 XRA     A       ;CLEAR PRINTER
0174 D316               OUT     16H     ;CLEAR
0176 CD4802             CALL    DELAY1  ;DELAY FOR SOLINOID RETURN
0179 C9                 RET
                        ;   END OUTPUT CONTROL ROUTINE
                        ;
                        ;   START NO. OF DATA BIT ROUTINE
017A 21F80F     CDBIT   LXI     H,CBIT  ;SET MEMORY POINTER
017D 34                 INR     M       ;INCREMENT CHECK BIT
017E C9                 RET
                        ;   END NO. OF CHECK BIT ROUTINE
                        ;
                        ;   START WRITE ROUTINE
017F 2AFE0F     WRTN    LHLD    WLOC    ;LOAD WRITE POINTER
0182 DB18               IN      18H     ;INPUT DATA
0184 77                 MOV     M,A     ;STORE DATA IN MEMORY
0185 3AF90F             LDA     ASCII   ;ASCII?
0188 B7                 ORA     A
0189 C29801             JNZ     WMEM    ;NO
018C 7E                 MOV     A,M
018D E67F               ANI     7FH     ;SUBPRESS MSB
018F 77                 MOV     M,A
0190 3AF10F             LDA     ELINE
0193 E601               ANI     1
0195 C2D201             JNZ     WMCK1
0198 FE03       WMEM    CPI     3       ;END OF TEXT?
019A C2A301             JNZ     WMEMCK  ;IF NOT END
019D 21F10F             LXI     H,ELINE ;LOAD POINTER
01A0 3601               MVI     M,1     ;SET FLAG
01A2 C9                 RET
01A3 FE28       WMEMCK  CPI     28H
01A5 C2B001             JNZ     WMCK
01A8 21F10F             LXI     H,ELINE
01AB 3610               MVI     M,10H
01AD C3DC01             JMP     WMEMDT
01B0 3AF10F     WMCK    LDA     ELINE
01B3 B7                 ORA     A
01B4 CADC01             JZ      WMEMDT
01B7 7E                 MOV     A,M
01B8 FE29               CPI     29H
01BA CAC501             JZ      WMCK2
01BD 21F10F             LXI     H,ELINE
```

```
01C0 3600           /       MVI     M,0
01C2 C3DC01                 JMP     WMEMDT
01C5 3E01           WMCK2   MVI     A,1
01C7 32F10F                 STA     ELINE
01CA 2AFE0F                 LHLD    WLOC
01CD 2B                     DCX     H
01CE 22FE0F                 SHLD    WLOC
01D1 C9                     RET
01D2 7E             WMCK1   MOV     A,M     ;CHECK RETURN
01D3 FE0D                   CPI     0DH     ;CARRIAGE RETURN?
01D5 C2E401                 JNZ     WMEMDA  ;DELAY LOOP
01D8 AF                     XRA     A       ;CLEAR REGISTER
01D9 32F10F                 STA     ELINE   ;SET FLAG
01DC 2AFE0F         WMEMDT  LHLD    WLOC
01DF 23                     INX     H       ;INCREMENT WRITE POINTER
01E0 03                     INX     B       ;INCREMENT DATA IN MEMORY
01E1 CD3002                 CALL    CMEM    ;CHECK MEMORY FULL
01E4 22FE0F         WMEMDA  SHLD    WLOC    ;SAVE WRITE POINTER
01E7 3AF30F                 LDA     CONT    ;DELAY LOOP?
01EA B7                     ORA     A
01EB CAFF01                 JZ      NEXT    ;NO
01EE 21F40F                 LXI     H,DEDY  ;LOAD DEDY
01F1 3606                   MVI     M,6     ;DECREMENT 6 DELAY LOOP
01F3 1B             LOOP1   DCX     D       ;DECREMENT DELAY LOOP
01F4 7A                     MOV     A,D
01F5 B3                     ORA     E       ;LOOP?
01F6 CAFF01                 JZ      NEXT    ;NO
01F9 35                     DCR     M       ;DECREMENT LOOP
01FA 7E                     MOV     A,M
01FB B7                     ORA     A       ;LOOP?
01FC C2F301                 JNZ     LOOP1   ;YES
01FF 78             NEXT    MOV     A,B     ;CHECK MEMORY FULL
0200 FE06                   CPI     6
0202 C0                     RNZ
0203 79                     MOV     A,C     ;CHECK MEMORY FULL
0204 FEC0                   CPI     0C0H
0206 C0                     RNZ             ;NOT FULL CONTINUE
0207 3E81                   MVI     A,81H   ;STOP DATA-POINT
0209 D30C                   OUT     0CH     ;STOP DATA-POINT TRANSMIT
020B C9             OWRTN   RET
                    ;   END WRITE ROUTINE
                    ;
                    ;   START CHECK DECODER ROUTINE
020C 3E81           CHECK   MVI     A,81H   ;STOP DATA-POINT TRANSMIT
020E D30C                   OUT     0CH
0210 1605                   MVI     D,5     ;SET ADDRESS OF DECODER
0212 AF                     XRA     A
0213 D316                   OUT     16H     ;STOP PRINTER
0215 21C002                 LXI     H,2C0H  ;SET MEMORY POINTER TO TABLE
0218 22FC0F                 SHLD    RLOC
021B 2AFC0F         NXCHE   LHLD    RLOC    ;POINTER OF MEMORY
021E 5E                     MOV     E,M     ;SET DECODER
021F CDA500                 CALL    DECODE  ;DECODE ROUTINE
0222 2AFC0F                 LHLD    RLOC    ;LOAD POINTER
0225 23                     INX     H       ;NEXT ADDRESS
0226 22FC0F                 SHLD    RLOC    ;SAVE POINTER
0229 7C                     MOV     A,H     ;CHECK ADDRESS
022A EE04                   XRI     4       ;END?
022C C21B02                 JNZ     NXCHE   ;NO
022F C9                     RET
                    ;   END CHECK DECODER ROUTINE
                    ;
                    ;   START CHECK MEMORY ROUTINE
0230 7D             CMEM    MOV     A,L
0231 E6F0                   ANI     0F0H
0233 B4                     ORA     H
```

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0234 FECF               CPI     0CFH
0236 C0                 RNZ
0237 21000B             LXI     H,800H
023A C9                 RET
                ;   END CHECK MEMORY ROUTINE
                ;
                ;   START DELAY ROUTINE
023B CD9100     DELAY   CALL    INDATA  ;INPUT DATA
023E 7A                 MOV     A,D     ;END LOOP?
023F B3                 ORA     E
0240 C8                 RZ
0241 1B                 DCX     D       ;DECREMENT LOOP
0242 7A                 MOV     A,D
0243 B3                 ORA     E
0244 C23B02             JNZ     DELAY   ;NOT END
0247 C9                 RET
                ;
0248 D5         DELAY1  PUSH    D       ;SAVE DECODER ADDRESS
0249 3E01               MVI     A,1
024B 32F30F             STA     CONT    ;SET DELAY LOOP
024E 118403             LXI     D,900   ;DELAY 35 MSEC
0251 CD3B02             CALL    DELAY   ;DELAY
0254 D1                 POP     D       ;SET DECODER ADDRESS
0255 AF                 XRA     A
0256 32F30F             STA     CONT    ;CLEAR POINTER
0259 C9                 RET
                ;
025A 21F50F     DELAY2  LXI     H,DLAY  ;SET COUNTER DELAY
025D 361E               MVI     M,30    ;SET DELAY 1 SEC FOR CARRIAGE RETURN
025F 21F50F     DELAY3  LXI     H,DLAY
0262 35                 DCR     M       ;LOOP
0263 CD4802             CALL    DELAY1  ;DELAY 35 MSEC
0266 3AF50F             LDA     DLAY    ;CHECK COUNTER DELAY
0269 B7                 ORA     A
026A C25F02             JNZ     DELAY3  ;NOT END
026D C9                 RET
                ;
026E 21F50F     DELAY4  LXI     H,DLAY
0271 3602               MVI     M,2     ;SET 70 MSEC FOR SHIFT
0273 CD5F02             CALL    DELAY3
0276 C9                 RET
                ;   END DELAY ROUTINE
                ;
                ;   START CHECK PAPER ROUTINE
0277 CD7D02     CPAPR   CALL    HOLD
027A C35800             JMP     PAPERC
027D CD9100     HOLD    CALL    INDATA  ;INPUT DATA
0280 DB16               IN      16H     ;INPUT READY SW.
0282 E610               ANI     10H     ;READY SW.PRESS
0284 CA7D02             JZ      HOLD
0287 C9                 RET
                ;   END CHECK PAPER ROUTINE
                ;
                ;   END OF JOB ROUTINE
0288 AF         EOJRTN  XRA     A
0289 D3FF               OUT     0FFH
028B C7                 RST     0       ;STOP PROGRAM
OFF1 =          ELINE   EQU     0FF1H   ;LOCATION OF ENDLINE FROM DATAPOINT
OFF2 =          CHA2    EQU     0FF2H   ;LOCATION OF CHECK INPUT
OFF3 =          CONT    EQU     0FF3H   ;LOCATION OF DELAY POINTER
OFF4 =          DEDY    EQU     0FF4H   ;LOCATION OF DELAY LOOP
OFF5 =          DLAY    EQU     0FF5H   ;LOCATION OF COUNTER DELAY
OFF6 =          CHA1    EQU     0FF6H   ;LOCATION OF INPUT DATA
OFF7 =          CONTROL EQU     0FF7H   ;LOCATION OF CONTROL BIT OF PRINTER
OFF8 =          DATA    EQU     0FF8H   ;LOCATION OF NUMBER OF DATA
OFF9 =          ASCII   EQU     0FF9H   ;LOCATION OF ASCII FOR PRINT
OFFA =          FULL    EQU     0FFAH   ;LOCATION OF FLAG FOR MEMORY FULL
OFFB =          CBIT    EQU     0FFBH   ;LOCATION OF CONTENT OF CHECK BIT
OFFC =          RLOC    EQU     0FFCH   ;LOCATION OF READ POINTER IN MEMORY
OFFE =          WLOC    EQU     0FFEH   ;LOCATION OF WRITE POINTER IN MEMORY
028C                    END     START   ;STOP PROGRAM
```

ภาคผนวก จ

MAGNET COIL SPECIFICATIONS

Magnet coils may be found in both 24 and 48 volt operating ranges (Figure 4). The character selection, operational, and lower case shift magnets will operate within 10 milliseconds at their rated voltages. The upper case magnet, red ribbon shift magnet, and keyboard lock solenoid will operate within 12 milliseconds when operated at their rated voltage. The chart below gives the resistance and current ratings of the various magnets. Operation can be maintained at +10% of rated voltage, however, the operating speeds will vary.

NOTE: Magnet and triplink adjustments will affect pick time.

Where Used	Rated†† Voltage	Resistance in Ohms			Max. mA*
		Low	Rated	High	
Keyboard† Lock	48	329	358	397	146
	24	100	105	110	240
Upper Case Shift**	48	221	240	259	217
	24	62	65	68	387
One Magnet† Ribbon Shift	48	345	395	455	139
	24	125	137	150	192
All Others	48	432	475	518	111
	24	122	128	133	197

*Theoretical maximum current (in Milliamperes) at rated voltage – computed as ratio of rated voltage to low resistance.

**Also red magnet of Two Magnet ribbon shift.

†100% Duty Cycle. The Duty Cycle of all other magnets is described as "sufficient to provide continuous machine operation when magnet pulses are gated by the Feedback and Interlock Contacts."

Figure 4 – Magnet Coil Specifications

ประวัติผู้เขียน

นายสมโภชน์ อุไรเวโรจนากร เกิดวันที่ 16 สิงหาคม 2498 ที่จังหวัดกรุงเทพฯ สำเร็จการศึกษาขั้นปริญญาบัณฑิตจากจุฬาลงกรณมหาวิทยาลัย ได้รับปริญญาวิศวกรรมศาสตร์บัณฑิต ในปี พ.ศ. 2521 ปัจจุบันทำงานอยู่ธนาคารกสิกรไทย สีลม