CHAPTER IV

PERFORMANCE MODELING APPLICATIONS

The queueing model presents in chapter III can be useful in the system design stage of a multiple-microprocessor system. It can be helpful in choosing the architecture that best suits a given application. Two applications of the proposed model are presented in this chapter. The first application employs the model to analyze the performance of multiple-microprocessor based communication controller. The second application compares the performance of loosely coupled multiple-microprocessor system with that of the shared-memory system, when each system is considered as a part of a SCADA system. The approach to be presented in this chapter can be used as a guide-line to analyze the performance of other multiple-microprocessor systems.

4.1 Performance Analysis of The Multiple-Microprocessor Based Communication Controller [26].

The proposed model is used to investigate the response time of a multiple-microprocessor system functioned as a communication controller in a data acquisition system. The system of interest is shown in Fig. 4.1 . In order to relieve the load of the host computer in such a system, some data processing tasks are assigned to the communication controller. The external data from remote stations are sent to the host computer through the communication controller. The communication controller consists of two microprocessors, an input unit,and an output unit.

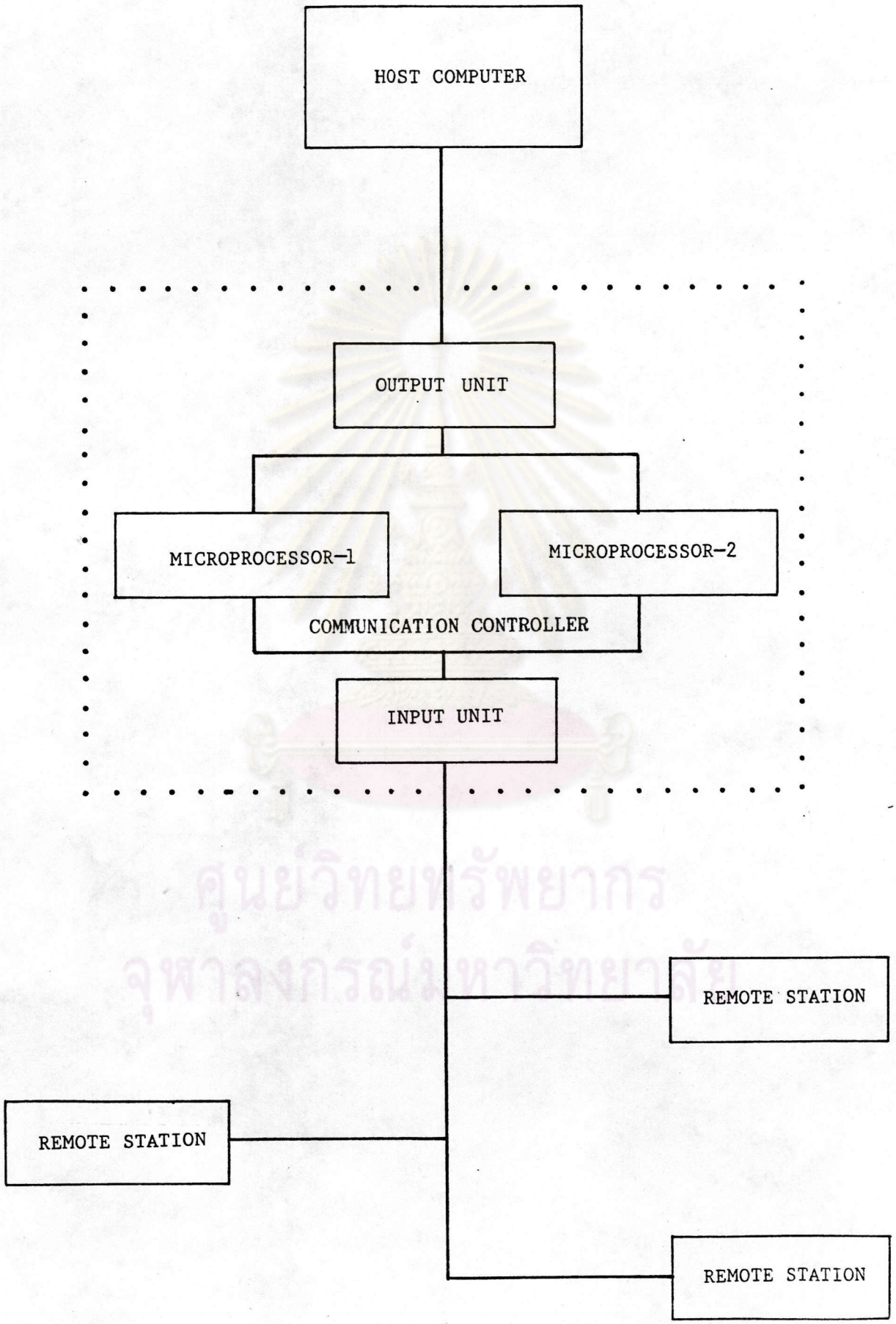

Fig 4.1 A multiple-microprocessor based communication controller in a data acquisition system.

The input transactions from the remote stations are input into the communication controller through the input unit and then sent to the shared memory. The transaction is then processed by either microprocessor-1 or microprocessor-2 depending on which one is available at the time of arrival. The processed transaction is then sent to the host computer through the output unit. The two microprocessors are not identical. The second microprocessor processing rate is a fraction of that of the first microprocessor. This is the situation where the former communication controller has only one microprocessor and there is a requirement to improve the system response time then one additional microprocessor is attached to the system. It is worth investigating the system response time when there are two microprocessors working together before actual implementation.

We can model the communication controller by using our M/M/2 queueing model with unequal service rate. It is assumed that the response time of the shared memory, the input unit, the output unit, and the internal bus are very short compared with the transaction processing time required by the microprocessors. Let the average processing rate of microprocessor-1 is $\mu_1 = 1$ transaction per second and the processing rate of microprocessor-2 is $\mu_2 = M\,\mu_1$ transaction per second.

The response time of the system with various value of M are shown in Fig. 4.2 .

There are two possible cases in our system i.e.

CASE 1 The former microprocessor has higher processing capability than the additional microprocessor.

In this case the former microprocessor will be microprocessor-1 and the additional microprocessor will be microprocessor-2 in our model. The multiple-microprocessor system is

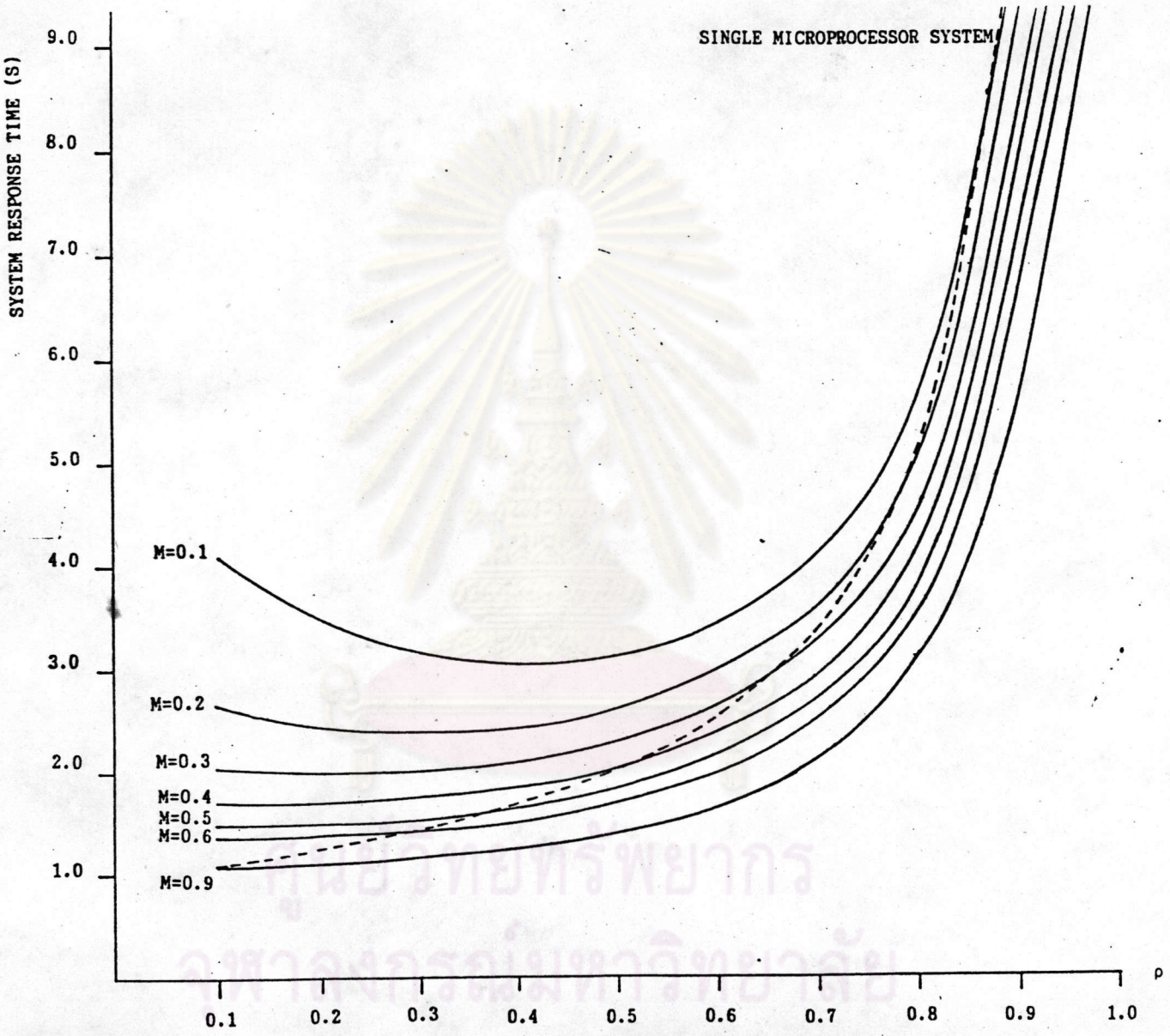

Fig 4.2 Response time of the multiple-microprocessor system in Fig 4.1 when μ_1 = 1 transaction/s and $\mu_2 = M\,\mu_1$, M = 0.1, 0.2, 0.3,...

normally used in a high traffic environment, hence it should be considered only the system with traffic intensity of higher than 50% (ρ=0.5) . The response time of single microprocessor system can be reduced by adding another microprocessor with an appropriate processing capability. It should be remarked that if the additional microprocessor has very low processing capability compared to that of the first one, the response time will increase rather than decrease. This is due to the influence of the small microprocessor, especially at low traffic intensity. For example if there are 2 transactions entering the system simultaneously, the first transaction can be processed within 1 second by the first microprocessor but another transaction requires 10 seconds for processing by the second microprocessor. The system response time then increases when comparing with the single microprocessor system. For all values of M , the multiple-microprocessor system can respond to a higher traffic intensity than the single microprocessor system.

However due to the influence of the small cooporating microprocessor, the full benefit from the multiple-microprocessor system can be achieved only in the system that the traffic intensity is higher than 50% (ρ>0.5) and the additional microprocessor has the processing capability of not less than 40% (M>0.4) of the former microprocessor. It is therefore suggested that the additional microprocessor should have processing capability of not less then 40% of the former microprocessor in the multiple-microprocessor system.

CASE 2 The additional microprocessor has higher processing capability than the former microprocessor.

Since a new generation microprocessor usually has more processing capability than that of the old one, microprocessor-1 in our model will be the additional microprocessor while microprocessor-2 will be the former microprocessor. If the former microprocessor is totally replaced by the new one, the system will become the single

microprocessor system. From the result of our model it is obvious that if the former microprocessor has a processing capability of only 10-30% of the new one,it is not effective to employ the multiple-microprocessor system. The multiple-microprocessor system is effective in the system that the former microprocessor has the processing capability of not less than 40% of the new one. However there should be the external device to by-pass the former microprocessor from the input traffic until the traffic intensity excesses the specific value in order to keep the system response time to minimum for all traffic intensity. For example the former microprocessor with 60% processing capability of the new one will be by-bassed from the input traffic until the traffic intensity is higher than 30%. At the traffic intensity of less than 30%, all input transactions are processed by the additional microprocessor. The system becomes the multiple-microprocessor system after the traffic intensity excesses 30%, the input transactions are processed by both the former and the additional microprocessor. By this way the system response time will always be kept to minimum and the full benefit from the multiple-microprocessor system is achieved.

If the system is implemented by using the multiple-microprocessor system with processor priority as described in section 3.2 , the system response time at various processing rate is shown in Fig. 4.3 . The response time of a single microprocessor system can be reduced by adding another microprocessor with an appropriate processing rate. However ,it should be remarked that if the additional microprocessor has very low processing capability compared with that of the first one,the response time will increase rather than decrease. This results from the influence of the small microprocessor. For example,if there are 2 transactions entering the system simultaneously,the first transaction can be processed within 1 second by the large microprocessor, but another transaction requires 10 seconds for processing by the small microprocessor. The system

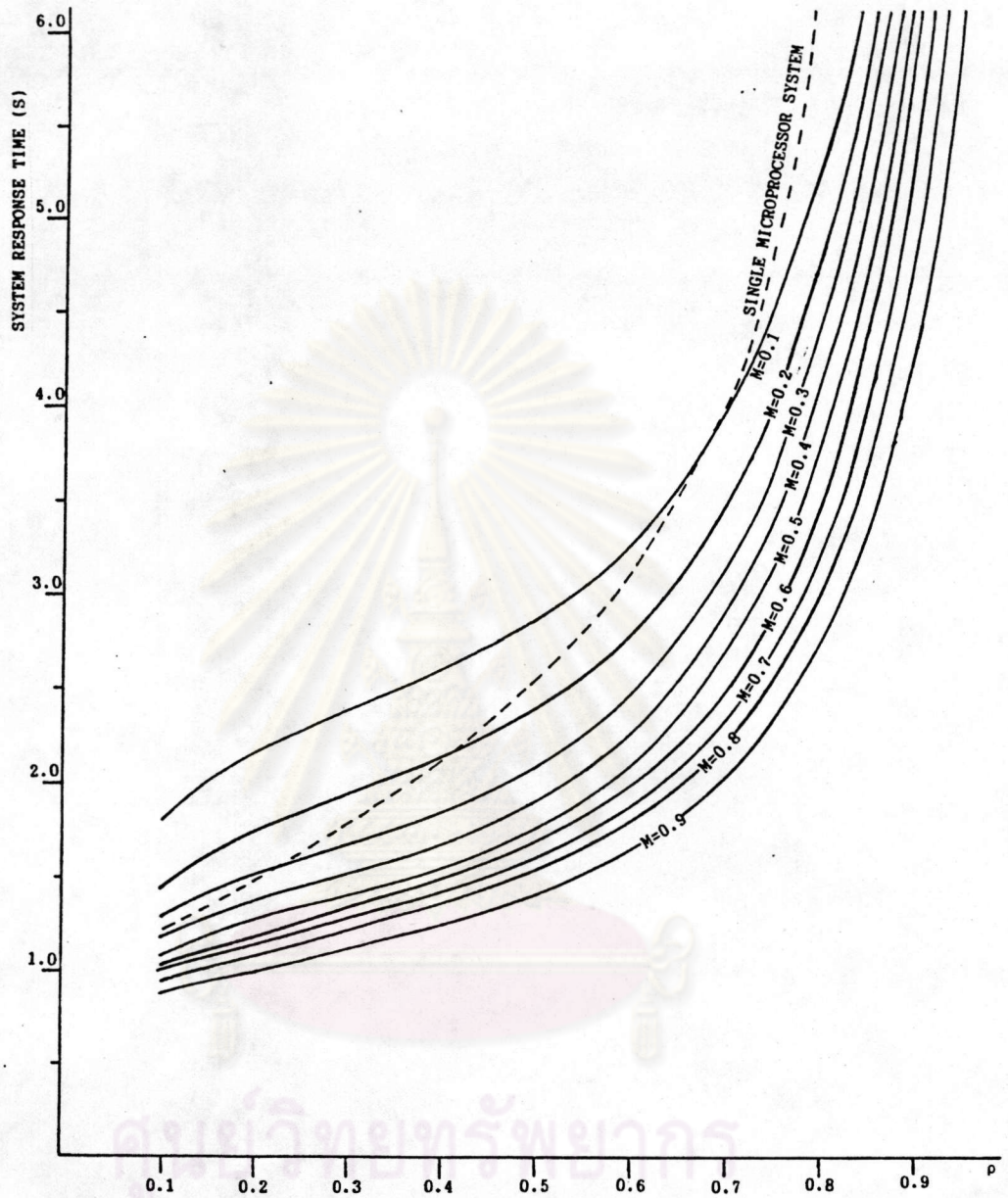

Fig 4.3 Response time of the multiple-microprocessor system in Fig 4.1 when microprocessor-1 has higher priority than microprocessor-2.

response time then increases when compared with the single microprocessor system.

In all cases, the multiple-microprocessor system with processor priority can provide shorter response time than the system with equal priority. This comes from the fact that the incomming transaction is scheduled to be processed by the microprocessor with the highest processing rate first,the transaction will be processed by the other microprocessors only when the former is busy.

In all cases, the multiple-microprocessor system with processor priority can respond to a higher traffic rate than the single microprocessor system. However, due to the influence of the small cooperating microprocessor, it is suggested that the additional microprocessor should has processing capability not less than 40% of the first microprocessor, in order to get full benefit of the multiple-microprocessor system.

4.2 Performance Comparison of the SCADA Systems [30].

Following an increasing demand for more sophisticated information processing from the industries, the functions of data aquisition and control system have become more complex in recent years. Today communication between the host computer and remote stations in most of the Supervisory Control And Data Aquisition (SCADA) is handled by a multiple-microprocessor based communication controller [31]. There are at present two popular multiple-microprocessor systems for real-time applications. They are the shared-memory multiple-microprocessor system and the loosely coupled multiple-microprocessor system. In this section, both of the multiple-microprocessor systems are proposed to function as the SCADA communication controller. The performance of the SCADA systems are compared,based on the response time, by using queueing model.

4.2.1 SCADA System with a Loosely Coupled Multiple-Microprocessor System as a Communication Controller.

In this approach, the SCADA communication controller is implemented by using a loosely coupled multiple microprocessor system. The communication controller consists of four microprocessors; and each microprocessor exchanges data with the others through the communication links as shown in Fig. 4.4. Three microprocessors are assigned as the REMOTE LINK UNIT (RLU) to manage data communication between the communication controller and the SCADA remote stations. Another microprocessor is assigned as the HOST INTERFACE UNIT (HIU) to manage communication between the communication controller and the SCADA host computer. The HIU communicates with the host computer and the RLUs through the high speed serial data transmission links. The remote stations are separated into three groups; each group communicates with the communication controller through the designated RLUs. The RLUs use the roll-call polling method to control remote station accessing [32]. As the name implies, remote stations are interrogated sequentially, one by one, by the RLU, which asks if they have any messages to transmit. The interrogated remote station then transmits data to the RLU. The RLU then sends a polling message to the next remote station on its list, repeating the same process. Once all the remote stations have been given permission to transmit data,the polling cycle is completed and a new one begins. The RLU then transmit all the received data to the host computer, through the HIU, according to the host computer command and a SCADA cycle is completed. The time duration between the issue of command by the host computer and its reception of the requested data is called the response time.

To analyze the system performance using queueing theory, each unit is modeled as a queue/server pair and assumed to be characterized completely by its mean service rate μ and message arrival rate λ. For the communication controller, there are separate communication

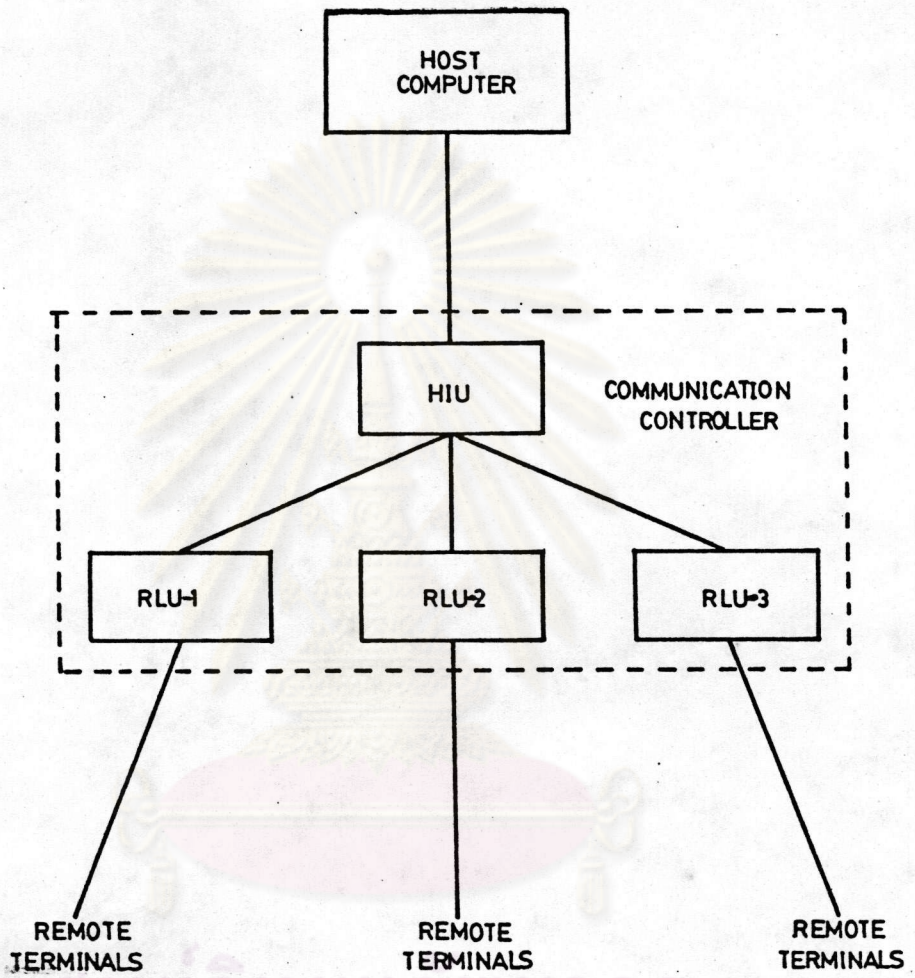

Fig 4.4 The SCADA system with the loosely coupled multiple-microprocessor system as a communication controller.

paths between HIU and the 3 RLUs, then three separate queues occur. It is assumed that the message arrival rate is a random variable with Poisson distribution and all the service time distributions are exponential, The 3 RLUs form a 3 M/M/1 queueing network and the SCADA system is modeled as a tandem of queues as shown in Fig. 4.5.

From Fig. 4.5

λ is the mean message arrival rate,

μ_{ho} is the mean service rate of the host computer,

μ_{hi} is the mean service rate of HIU,

μ_{ri} is the mean service rate of RLUi,

μ_c is the mean service rate of the communication controller.

The total system response time (TT) is the summation of the response time of the host computer and the communication controller [7]:

$$TT = \frac{1}{\mu_{ho}-\lambda} + \frac{1}{\mu_c-\lambda} \qquad (4.1)$$

The messages from the host computer enter the HIU and pass through the RLUs to the remote stations. If data from HIU is sent to the ith RLU with the probability Pi, then the mean response time, Ti; for each RLU is

$$Ti = \frac{1}{\mu_{ri} - \lambda_{Pi}} \quad i = 1, 2, 3 \qquad (4.2)$$

The overall response time of the 3 polling RLUs is

$$Tp = \sum_{i=1}^{3} P_i \frac{1}{\mu_{ri} - \lambda_{Pi}} \quad i = 1, 2, 3 \qquad (4.3)$$

Express Pi in term of μ_{ri}

$$Pi = \frac{\mu_{ri}}{\sum_{j=1}^{3} \mu_{rj}} \quad i = 1, 2, 3 \qquad (4.4)$$

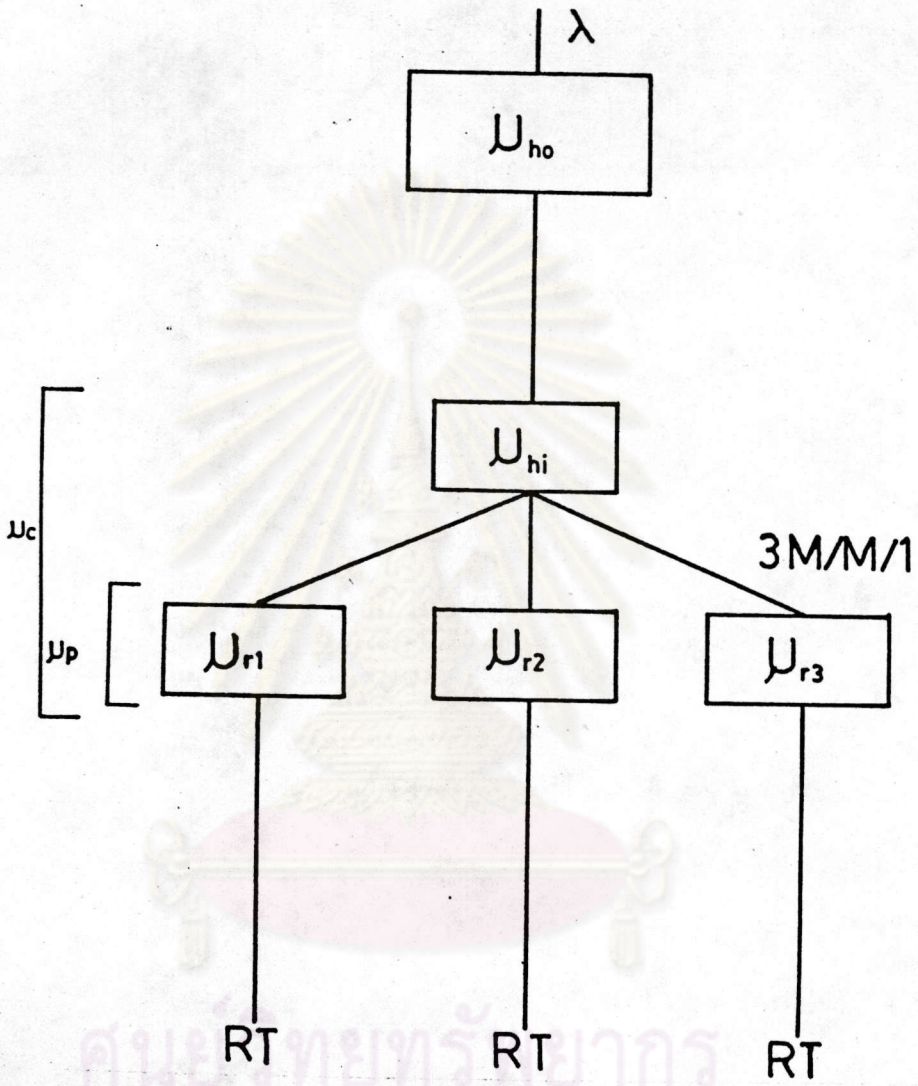

Fig 4.5 Queueing model of the SCADA system in Fig. 4.4

Substitution of Pi from eq. (4.4) into eq.(4.3) gives the overall response time of the 3 RLU's :

$$Tp = \sum_{i=1}^{3} \frac{1}{\mu_{ri} - \lambda\mu_{ri} \frac{\mu_{ri}}{\sum_{j=1}^{3} \mu_{rj}}}$$

$$= \frac{3}{\sum_{i=1}^{3} \mu_{ri} - \lambda}$$

Hence, the overall service rate of the 3 RLU's μ_p is

$$\mu_p = \frac{\sum_{i=1}^{3} \mu_{ri} - \lambda}{3} \qquad (4.5)$$

From Fig.4.5, the HIU and the 3 RLUs form a tandem queue; and the the total response time of the communication controller, TTc, is

$$TTc = \frac{1}{\mu_c - \lambda} = \frac{1}{\mu_{hi} - \lambda} + \frac{1}{\mu_p - \lambda}$$

$$= \frac{1}{\mu_c - \lambda} = \frac{1}{\mu_{hi} - \lambda} + \frac{3}{\sum_{i=1}^{3} \mu_{ri} - 4\lambda} \qquad (4.6)$$

The RLU service rate μ_{ri} can be calculated from the polling cycle time, derived by Yang [7].

If Tt is the message transmitted time in polling,

Ni is the number of remote terminal attached to RLUi,

C is the mean length of the message reply time interval,

then the RLU service time μ_{ri} is

$$\mu_{ri} = \frac{1}{Tt + N_i C} \qquad i = 1, 2, 3 \qquad (4.7)$$

To give a numerical example of this SCADA system, the SCADA parameters are given as follows :

$N_1 = N_2 = N_3$ = number of remote stations attached to RLUi
= 10 stations

C = message reply time interval = 1 timeslot

Tt = message transmitted time = 3 timeslots

polling message length = 40 bits

message transmitted rate = 1200 bits/s

The time taken for 1 timeslot = 40 bits/(1200 bits/s) = 33.33 ms
Substition of these numerical data in eq. (4.7), gives for this SCADA

$$\mu_{ri} = \frac{1}{(3 \times 33.33ms) + 10\ (1 \times 33.33ms)}$$

$$= 2.3 \text{ messages/s.}$$

If the message arrival rate $\lambda = 0.05$ message/s, the service rate of the host computer and HIU, $\mu_{ho} = \mu_{hi} = 3$ messages/s, then the total response time of the communication controller, from eq. (4.6), is

$$TTc = \frac{1}{\mu_c - \lambda} = \frac{1}{3 - 0.5} + \frac{3}{3(2.3) - 4(0.5)}$$

$$= 1.01 \text{ s.}$$

The SCADA system response time, TT, of the loosely coupled multiple microprocessor based SCADA can be calculated from eq (4.1).

$$TT = \frac{1}{3 - 0.5} + 1.01 = 1.41 \text{ s.}$$

4.2.2 SCADA System with the Shared-Memory Multiple-Microprocessor System as a Communication Controller.

The SCADA communication controller in the previous system is replaced by the proposed shared memory multiple microprocessor system. The communication controller has the same configuration as the previous system but only replaces the serial communication links

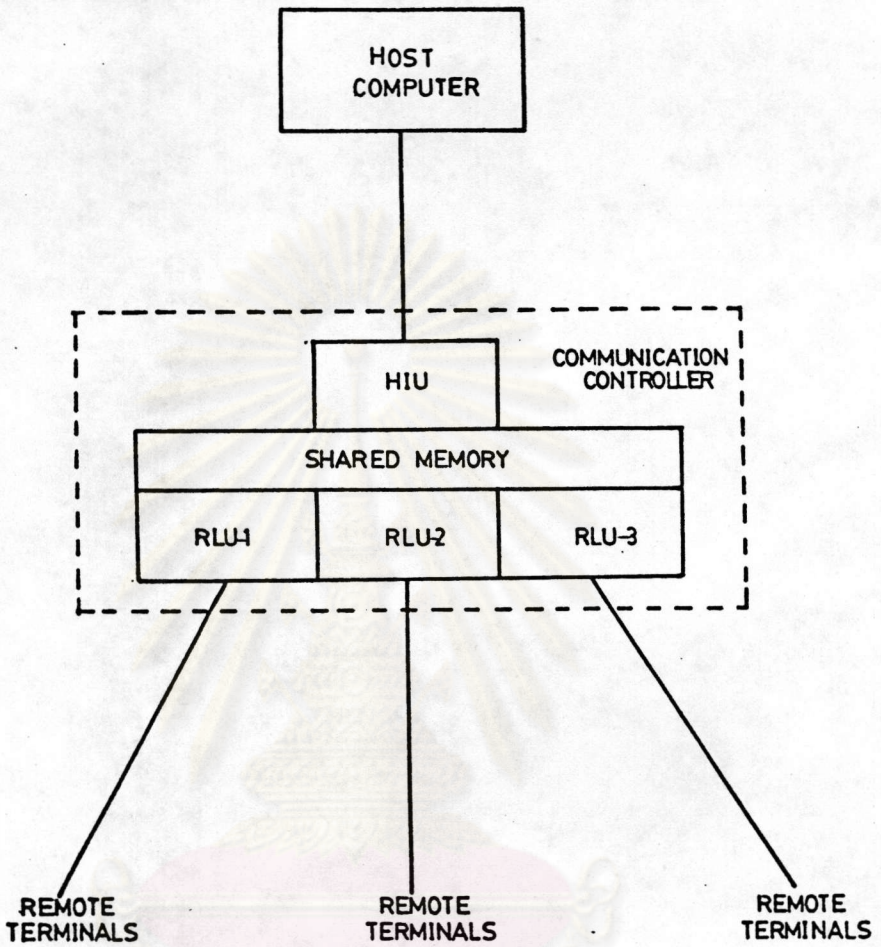

Fig 4.6 The SCADA system with the shared-memory multiple-microprocessor system as a communication controller.

between HIU and RLUs with the common shared memory, as shown in Fig. 4.6. The HIU and RLUs use the common shared memory to exchange data, both from the host computer and the remote terminals. Using shared memory technique, each microprocessor in the system will see the shared memory as logical extension of its local memory. In the simplest scheme, each microprocessor using the shared memory will be assigned a specific area to write data, but allowed to read data from any area in the shared memory. With this configuration, the data transfer rate through the shared memory is very high when compared with that of the communication link; this implies that HIU can send or receive data from any RLUs at any given time. It is equivalent to a queueing network with 3 identical servers (RLU) service to the single queue (from HIU) i.e. the 3 RLUs from the M/M/3 queueing model, as shown in Fig. 4.7 .

The queueing model in section 4.1 can applied to this system. It is assumed that $\mu_{r1} = \mu_{r2} = \mu_{r3} = \mu_{ri}$ and the mean response time for the 3 polling RLUs can be calculated from eq. (3.5) .

$$Tp = \frac{\frac{\lambda^3}{6\mu_{ri}^3}}{3\mu_{ri}\left(1-\frac{\lambda}{3\mu_{ri}}\right)\left[\frac{\lambda^3}{6\mu_{ri}^3} + \left(1-\frac{\lambda}{3\mu_{ri}}\right)\left(1+\frac{\lambda}{\mu_{ri}} + \frac{\lambda^2}{2\mu_{ri}^2}\right)\right]} + \frac{1}{\mu_{ri}} \qquad (4.8)$$

Now the service rate μ_p of the 3 polling RLUs can be calculated as follows:

$$\mu_p = \frac{1}{Tp} = \frac{3\mu_{ri}^2\left(1-\frac{\lambda}{3\mu_{ri}}\right)\left[\frac{\lambda^3}{6\mu_{ri}^3} + \left(1-\frac{\lambda}{3\mu_{ri}} + \frac{\lambda^2}{2\mu_{ri}^2}\right)\right]}{\frac{\lambda^3}{6\mu_{ri}^2} + 3\mu_{ri}\left(1-\frac{\lambda}{3\mu_{ri}}\right)\left[\frac{\lambda^3}{6\mu_{ri}^3} + \left(1-\frac{\lambda}{3\mu_{ri}} + \frac{\lambda^2}{2\mu_{ri}^2}\right)\right]} \qquad (4.9)$$

From Fig. 4.7 HIU and the 3 RLUs form a tandem queue; hence, the response time of the communication controller, TTc is

$$TTc = \frac{1}{\mu_c - \lambda} = \frac{1}{\mu_{hi} - \lambda} + \frac{1}{\mu_p - \lambda} \qquad (4.10)$$

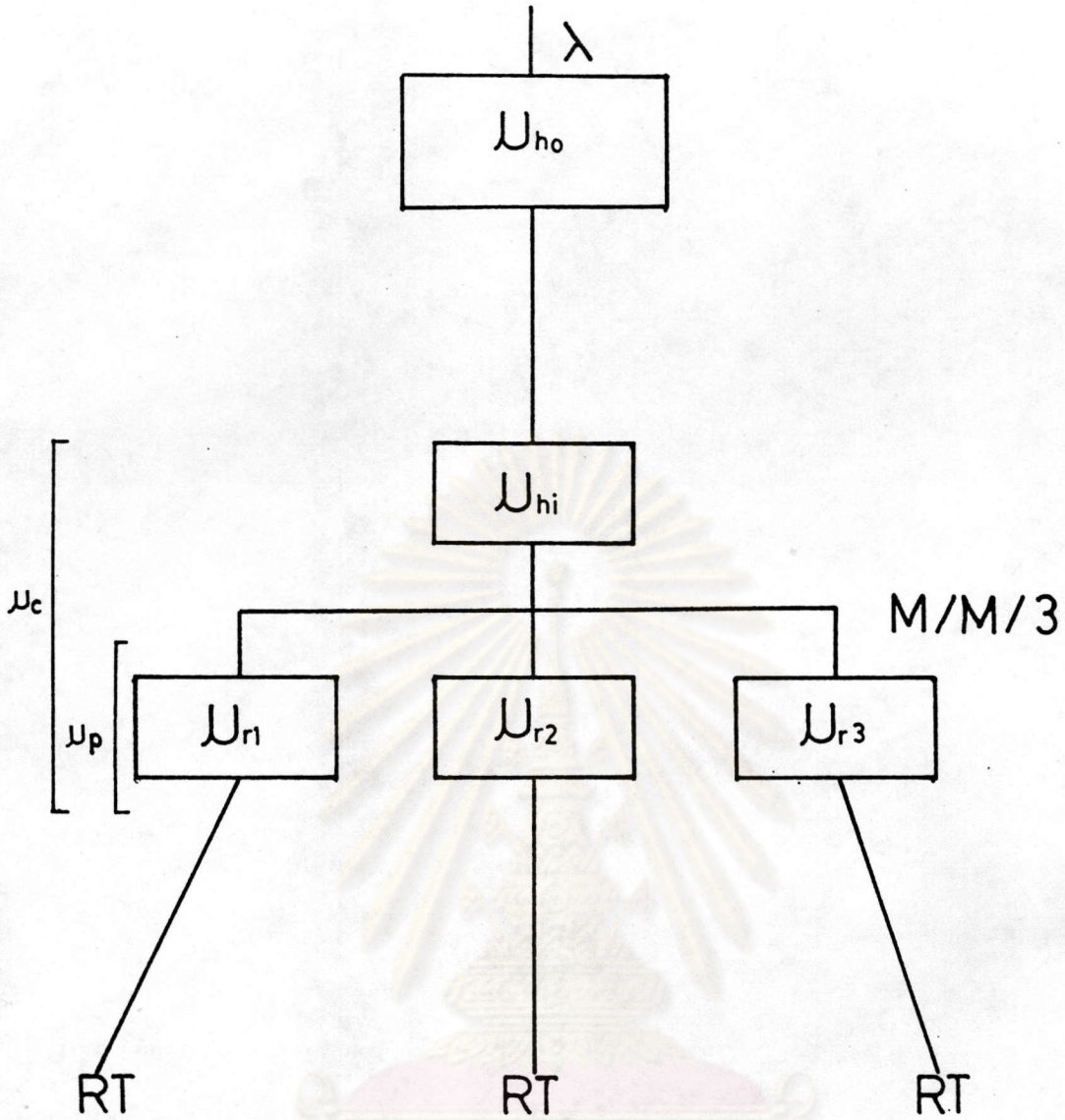

Fig 4.7 Queueing model of the SCADA system in Fig. 4.6

Based on the same calculation as in section 4.2.1, μ_{ri} for this system is the same as the previous system ,i.e.,

$$\mu_{ri} = \frac{1}{Ti + N_iC} \qquad i = 1, 2, 3 \qquad (4.11)$$

If the same numerical values for the SCADA parameters are assigned as in section 4.2.1 then μ_{ri} = 2.3 messages/s. If the mean message arrival rate is assumed to be 0.5 message/s, and the host computer and HIU service rate are both equal to 3 messages/s. The service rate of the 3 RLUs, μ_p can be calcutated by substituting μ_{ri} and λ in eq. (4.9) and the μ_p is 2.30 messages/s.

Substition of μ_p , μ_{hi} and λ in eq.(4.10) yields the response time of the communication controller TTc :

$$TTc = \frac{1}{\mu_c - \lambda} = \frac{1}{3 - 0.5} + \frac{1}{2.3 - 0.5} = 0.93 \text{ s.}$$

Using eq. (4.1), the total SCADA system response time, TT, of the shared memory based SCADA system is then calculated .

$$TT = \frac{1}{3 - 0.5} + 0.93 = 1.33 \text{ s.}$$

From the analysis results of the queueing model of both proposed systems, it is found that the response time of the SCADA with the shared-memory multiple-microprocessor system is 1.33 seconds while that of the SCADA with the loosely coupled multiple-microprocessor system is 1.41 seconds, at a message arrival rate of 0.5 message/s, based on the same SCADA parameters. The former system response time is about 5% faster than the latter. The system response time at various mean arrival rates, based on the same SCADA parameters are calculated and the results for both systems are shown in Fig.4.8. It is obvious that the higher the message arrival rate is, the better the response

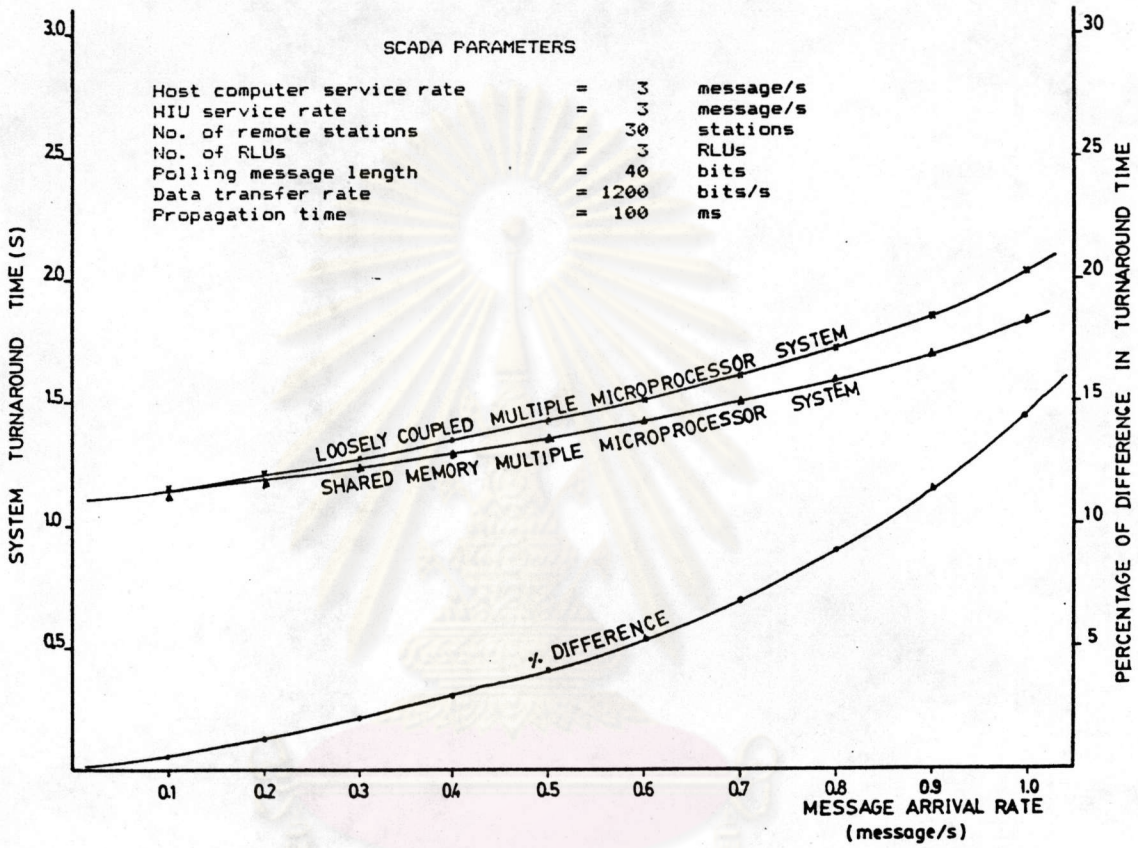

Fig 4.8 Performance comparison between the two SCADA systems.

time of the SCADA with the shared-memory multiple-microprocessor sytems becomes, compared with that of the SCADA with the loosely coupled multiple-microprocessor system. Hence, it can be concluded that the SCADA with the loosely coupled multiple-microprocessor system is appropriate for the system with low message arrival rate while the shared-memory multiple-microprocessor system is appropriate for implementing a communication controller for SCADA system with high message arrival rate.