Chapter 6

Building the pulse shaping unit

The pulse shaping unit consists of the GPIB interface and the main circuit of the pulse shaping unit. The GPIB interface of the pulse shaping unit is the same as one of the pulse programmer, so this section will not be referred.

The main circuit of the pulse shaping unit

The structure of the pulse shaping unit has been described in chapter 4. In this chapter will describe the details of the pulse shaping unit. The main circuit of the pulse shaping unit is shown in Fig.6-1. On the left of this circuit, it is connected with the GPIB interface. A 8 bit latch (IC1) is active during the information-store time.

The information storing of the pulse shaping unit

When the pulse shaping unit is turned on, the GPIB interface and the other parts of the pulse shaping unit will be initialized. The 8 bit latch will be active - $\overline{LE}$ and $\overline{OE1}$ are low. A memory (IC7), that is 62256 for 32K RAM or 6264 for 8K RAM, is in the write state - $R/\overline{W}$ is low and $OE2$ is high. The manual trigger switch (SW1) or external trigger is disabled - EN is low and START is normally high. The address generator consists of binary counter (down), binary counter (up), 11 bit latch, AND gates (IC11A, IC11B, IC11C) and inverter (IC9C). It is reset address to zero by taking $\overline{RES}$ to low for a moment when INC and EOD are high. In the information-store time, OC is low to control the output of the pulse shaping unit to zero voltage and $\overline{WREN}$ is low for the write state.

When the informations are sent to the pulse shaping unit, IC1 will be controlled to latch data on Q0 - Q7 by the GPIB interface before increment one address - taking positive pulse on INC pin. Each byte of

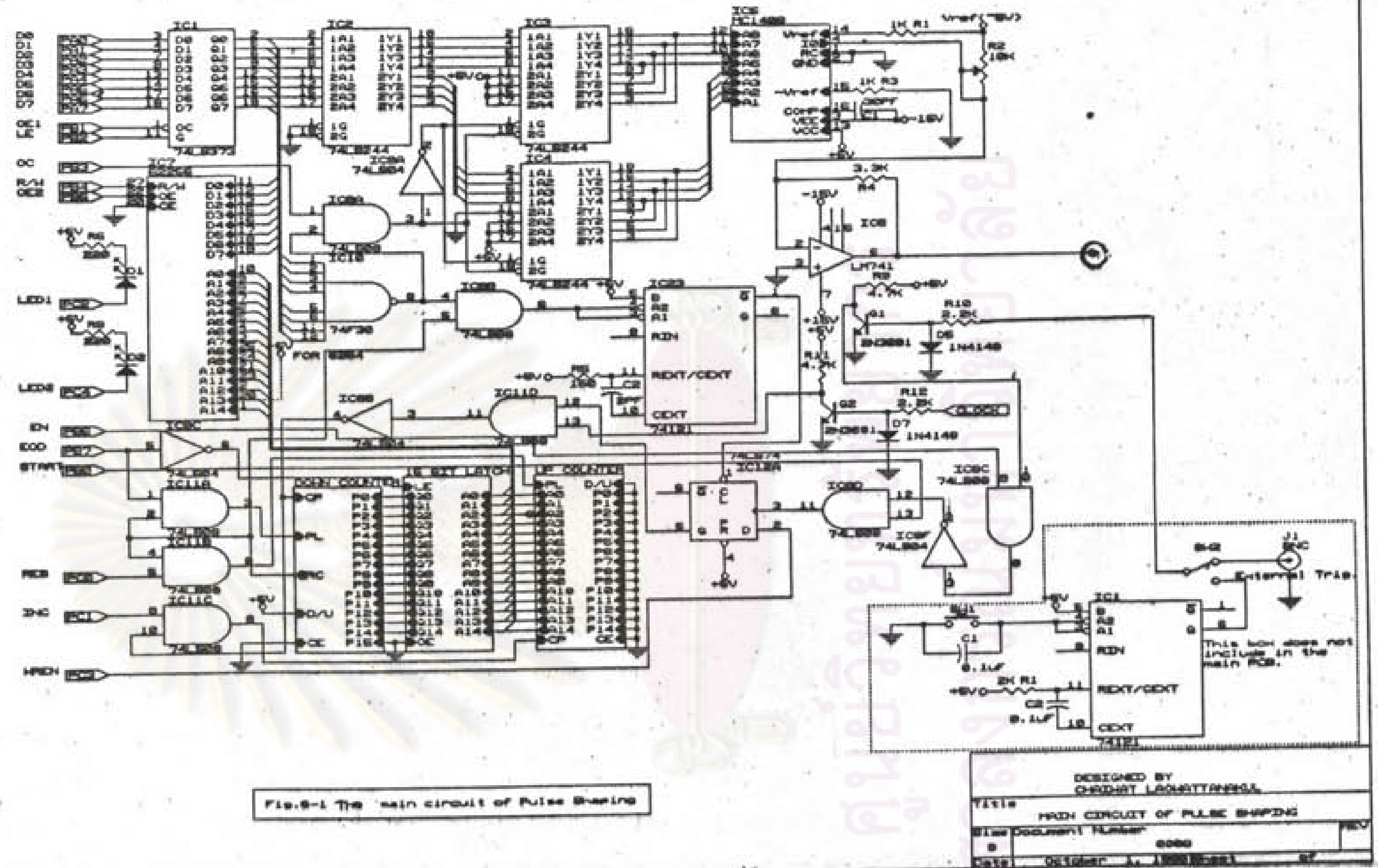

Fig.9-1 The main circuit of Pulse Shaping

the information will store on 62256 RAM (IC7). It will repeat until end of data, two bytes of 255 value. These values will not store in the pulse shaping unit. Then the GPIB interface will control IC1 to disable - $\overline{IE}$ and $\overline{OE1}$ are high - and control 62256 RAM (IC7) to the read state - $R/\overline{W}$ is high and $\overline{OE2}$ is low after latching the last address on the address bus into the 15 bit latch, resetting the up counter to zero and loading the down counter with the last address from the 15 bit latch. D2 (Data ready) is also lighted by the GPIB interface taking LED2 to be low and then $\overline{WREN}$ and OC are controlled to be high also. At this time the GPIB interface is waiting the GPIB commands - such as gpsclr, gpaclr, gpsloc,..., etc. (see the GPIB commands in appendix A). If the GPIB command is the trigger command (gptrg), the GPIB interface will generate the negative pulse on 'START' pin. The leading edge of this signal will execute the pulse shaping unit.

The executing process of the pulse shaping unit

The negative pulse on 'START' pin is ANDed with the inverted signal from IC9F and IC8C, the trigger-enable switch. The leading edge of this negative pulse will control IC12A and IC11D, the clock switch, to turn on. Consequently, the clock can pass to the address generator, then the address on the address bus is increased with rate 1 address per clock-period. While the address is changed, the stored data on IC7 is released on the data bus and is sent to the D/A (IC5) by passing IC2, IC3 and IC4. Analog signal on the output of the D/A (IC5) is amplified by a operational amplifier (IC6). This analog signal will not be zero voltage when the new data on the data bus will not be 127 or the stop code (255). If the new data on the data bus is the stop code (255), the output signal of the stop code checker (IC10) will change from high to low. It will send to two parts. This first part is the bus switch consists of IC3 and IC4. This signal will control IC3 and IC4 to send value (127) to the D/A (IC6), so the voltages of the analog output of IC6 is zero. The second part is the start/stop control consists of IC8B and IC23. This signal will control IC8B and IC23 to generate the negative pulse for

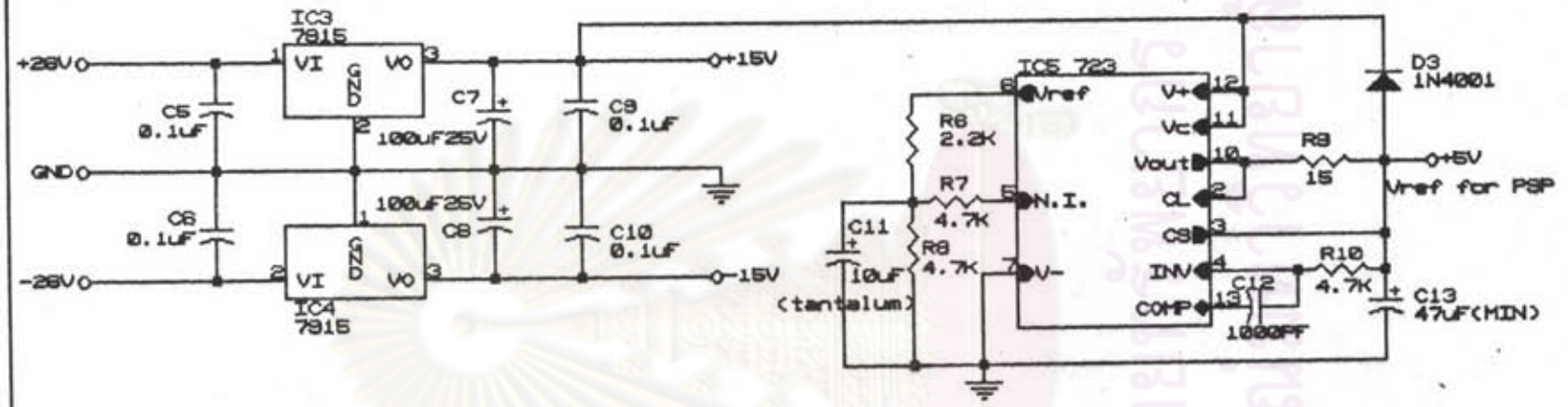

Fig.6-2 The circuit of resulator for A/D of PSP

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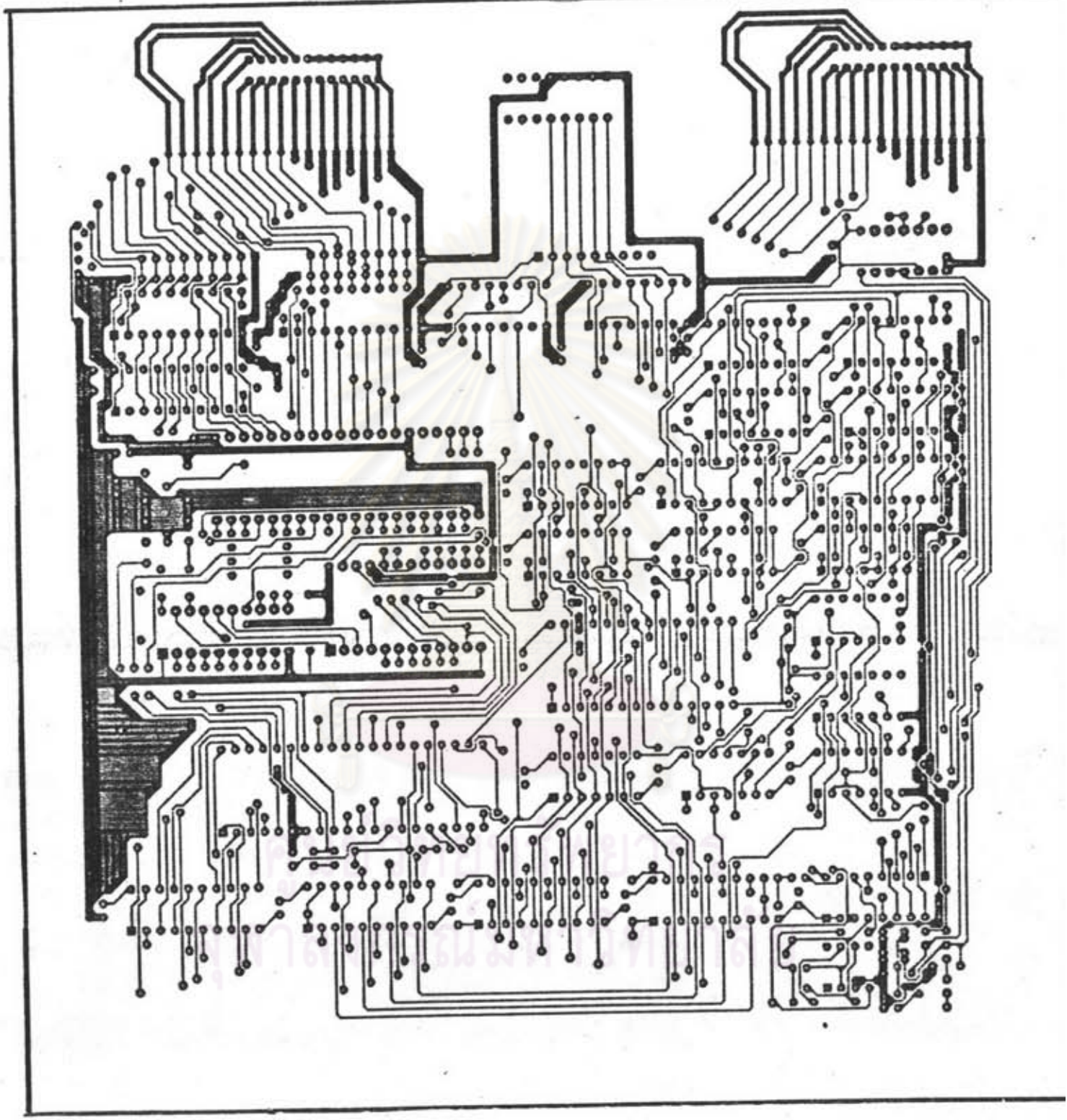

Fig.6-3 The mirror of the solder side of the printed circuit board for PSP.

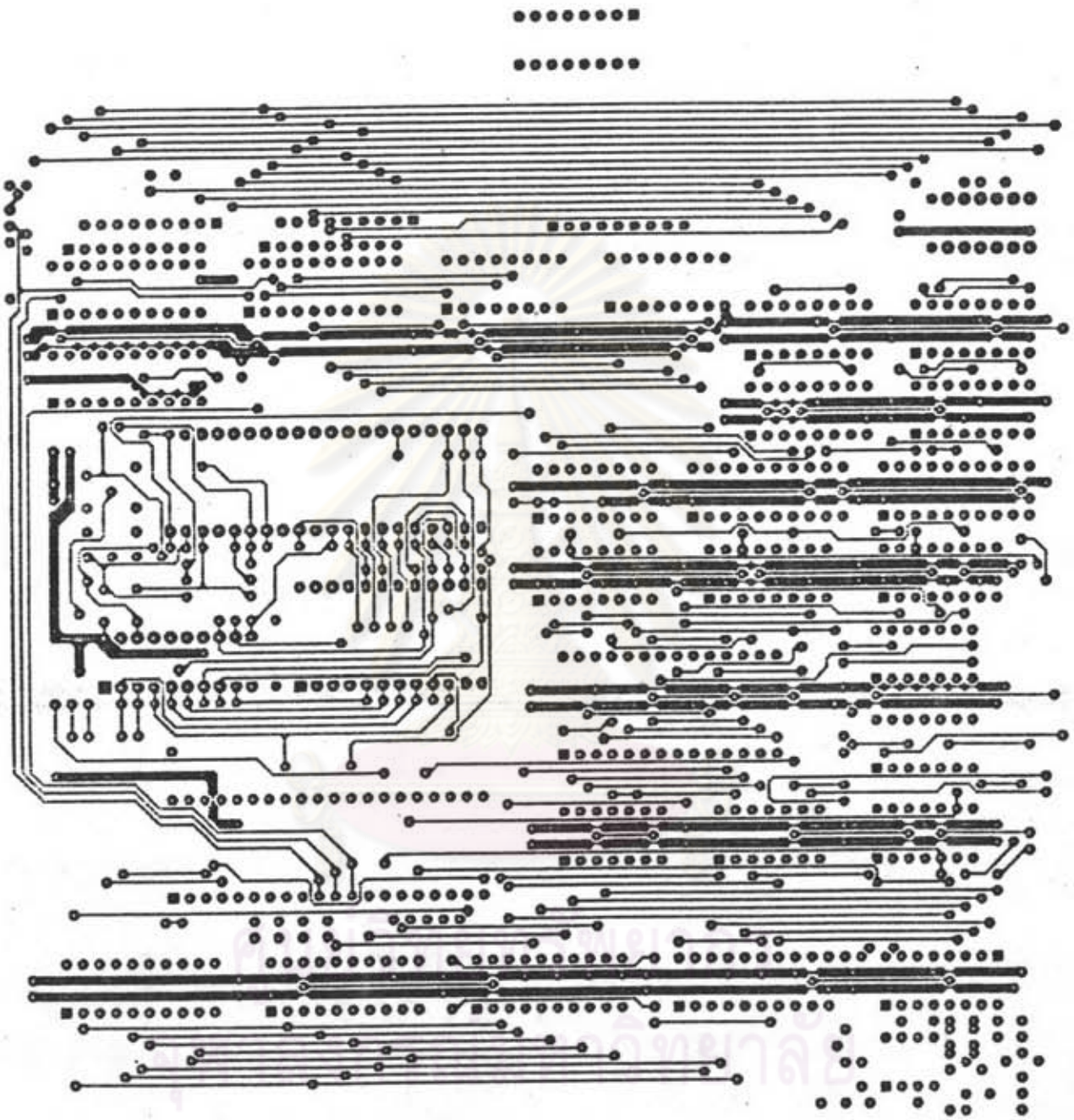

Fig.6-4 The component side of the printed circuit board for PSP.

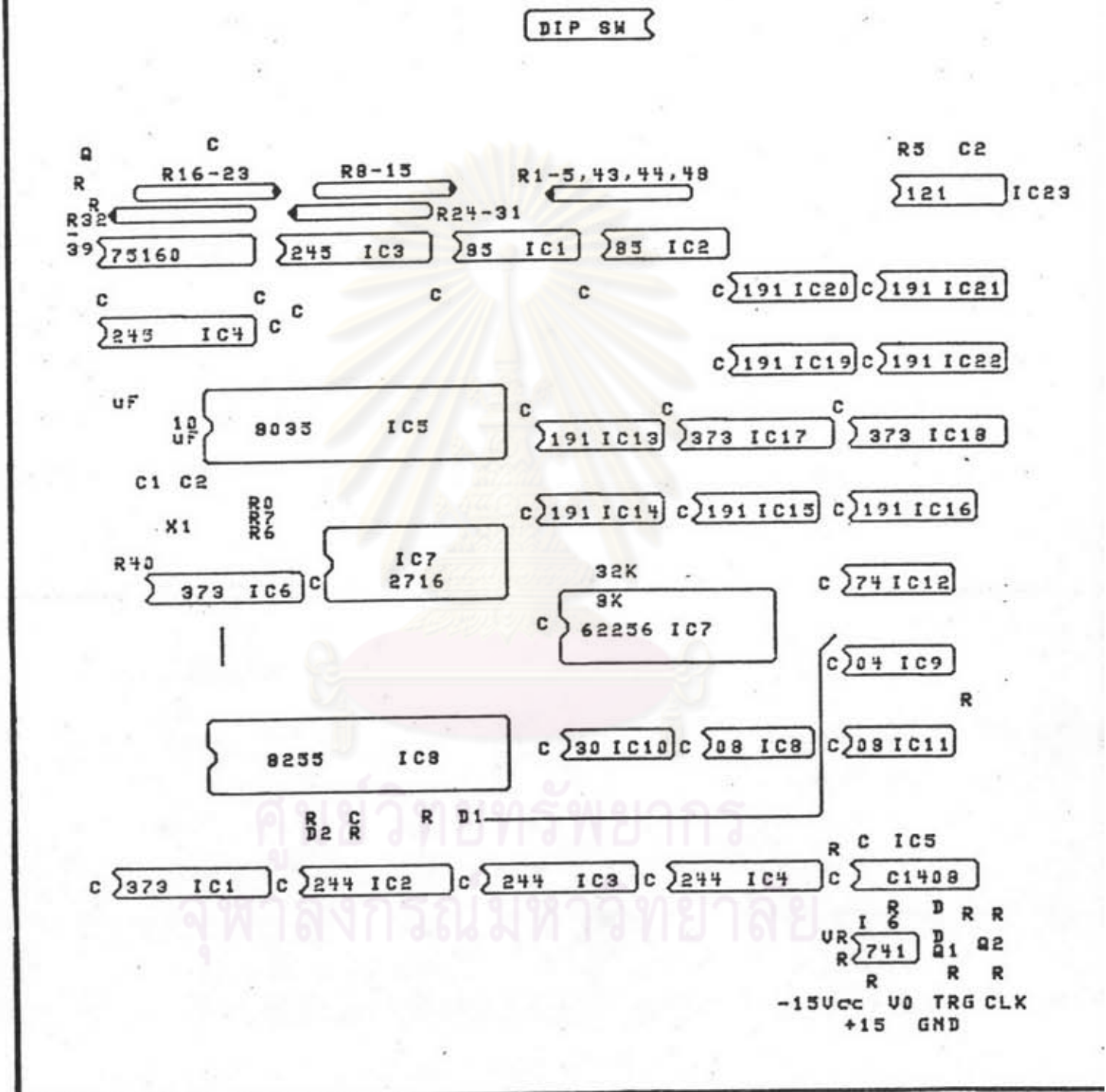

Fig.6-5 The component layout for PSP.

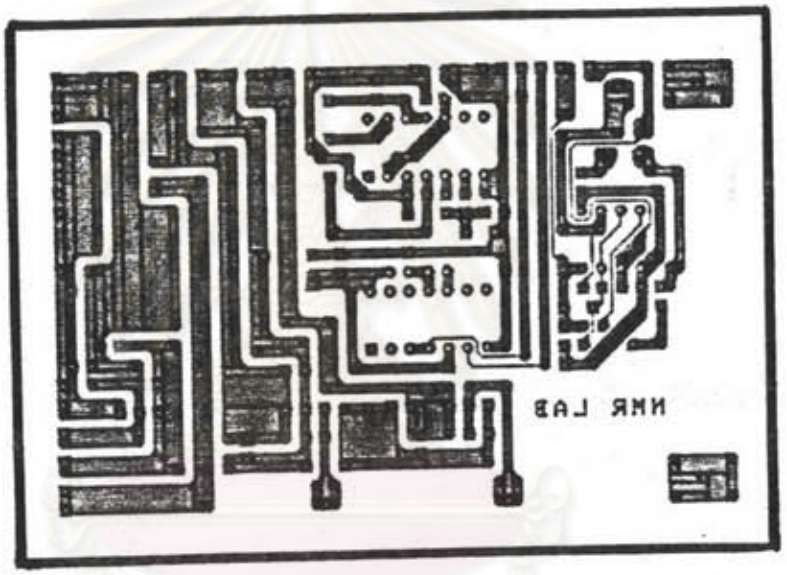

Fig.6-6 The mirror of the solder side of the printed circuit board of the power supply and the internal clock for PSP.

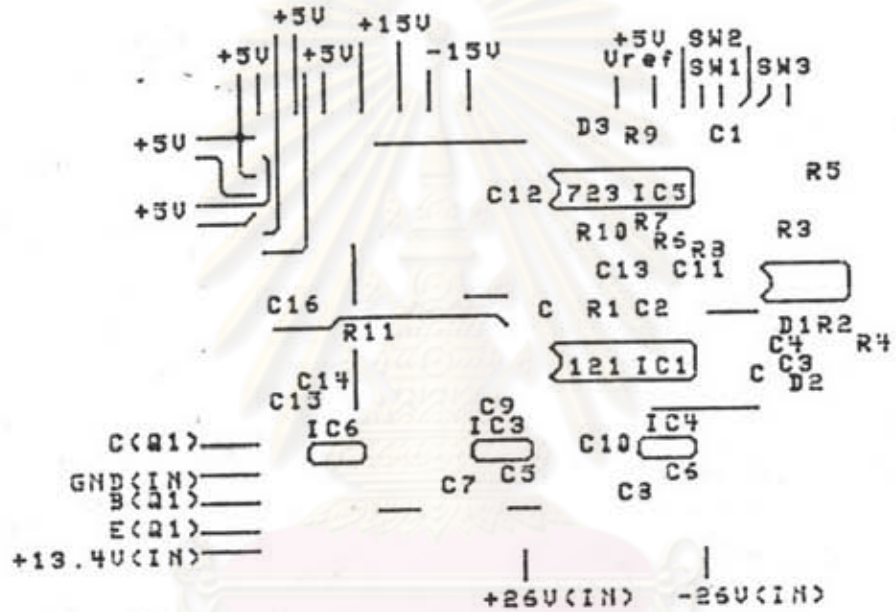

Fig.6-7 The component layput of the printed circuit board of the power supply and the internal clock for PSP.

turning the clock switch off. Then the address generator will stop at the address storing the stop code and it is waiting to receive the trigger signal from the 'START' pin or external trigger or manual trigger button (SW1) on the front panel key operation. This manual trigger button (SW1) can enable by the GPIB local commands (gpsloc or gpaloc) - the GPIB interface will control 'EN' pin to be high. In NMR imaging, the trigger signal is received from the external trigger that is connected with the some channels of the pulse programmer.

Power Supply for the pulse shaping unit

Since the pulse shaping unit is build with ICs TTL and linear ICs, so power supplies of the pulse shaping unit are +15V, +5V, -15V and +7.1V for reference voltage of the D/A. The circuit of the pulse shaping unit requires current at least 0.7A for IC TTL (+5V). This circuit is the same as one in Fig.5-7. It contains only the regulator, without transformer and rectifier. The another power supplies are shown in Fig.6-2.