CHAPTER 3

DEVELOPMENT OF TWO CHANNEL ANALYZER

Two channel analyzer is developed for analysing two toxic elements, lead and sulfur in fuel oils. The basic function of this equipment bases on a pulse height analysis technique in single channel analyzer(SCA). The SCA produces an accumulating data to the counter when the pulse height falls within the energy window which is set by the E and Δ E controls. Thus a particular spectral line of photon energy by the proportional detector can be selected and counted alone in the presence of other spectral lines.

3.1 The Function of Two Channel Analyzer[6]

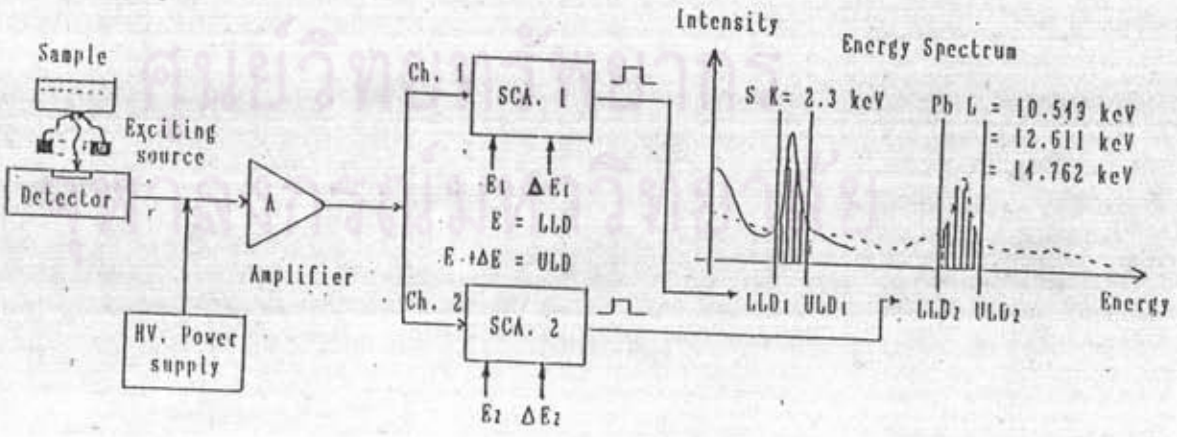

Fig. 3.1 Simplified diagram of two channel analyzer.

In diagram of Fig. 3.1, the primary X-ray from exciting source induces the sample to emit the fluorescent X-ray. When the characteristic X-ray of each element incidents on a proportional detector, the inert gas in the detector will be ionized and created the ion-pairs, under the influence of the electric field between anode and cathode. The amount of ion-pairs correspond to the photon energy. The collected charges on the anode of detector are integrated by charge sensitive amplifier and the amplifier changed these signal into voltage pulses. All pulses are gained the amplitude to suitable range by amplifier and provide the output pulse in Guassian shape. Pulse height of amplifier output are selected by the two sets of the energy window, the first channel for E_1 (range from 1.978 keV - 2.638 keV) and the second channel for E_2 (range from 9.748 keV - 15.458 keV), as shown in Fig. 3.1. Two spectral lines of sulfur K X-ray and lead L X-ray are obtained in each channel of SCA

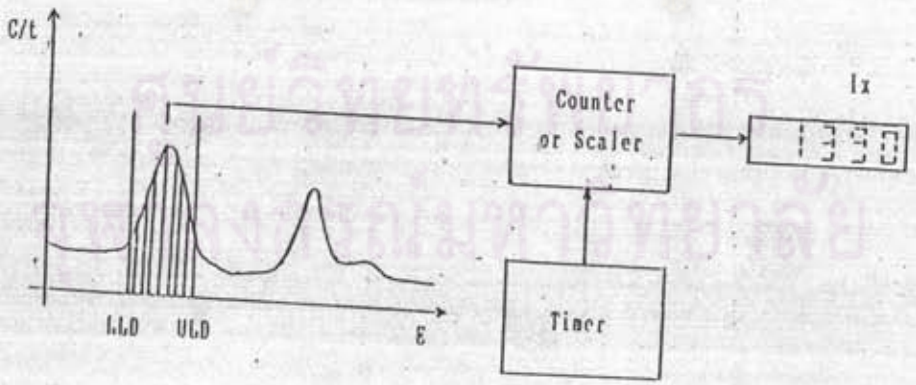

Fig. 3.2 Accumulating data of area under peak.

The selected pulse height from SCA are accumulated by the counter, as a data of intensity equivalents to the area under peak of fluorescent X-ray of the element in the sample. By these data, the concentration of known element can be calculated by comparing to standard sample.

3.2 Block Diagram Description

This equipment is designed to facilitate the inspection of some elements in known sample by using X-ray fluorescence technique. The configuration of two channel analyzer are comprised of four main parts; detector chamber, amplifier, pulse height analyzer and data display unit, as shown in Fig. 3.3

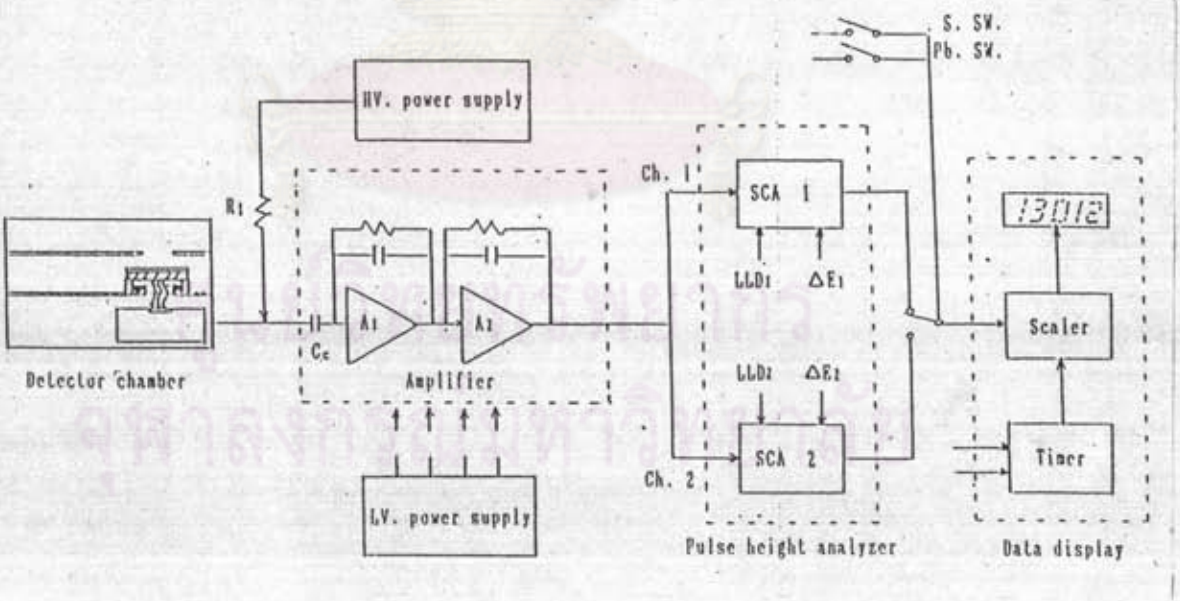

Fig. 3.3 Block diagram of two channel analyzer.

The detector chamber consists of a proportional X-ray detector with xenon gas filled, a high voltage power supply in range of 0-2500 volts to provide the operating bias for detector and a chamber set which designs in two purposes, one for the quick changing of two exciting sources (Fe-55 and Cd-109), to obtain the suitable absorption energy and sample loading, the other for the purpose of radiation protection. The construction of detector chamber is shown in Fig. 3.4

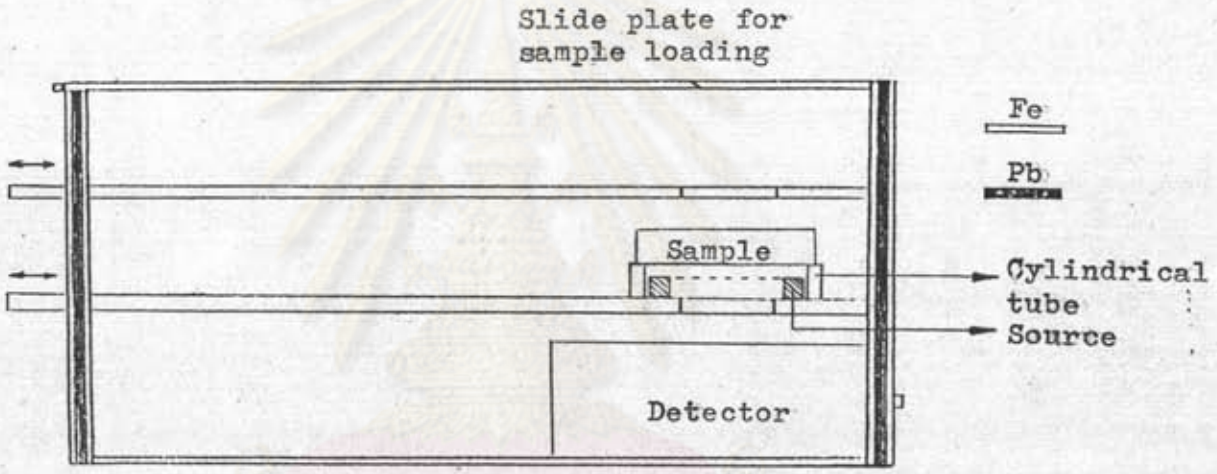

Fig. 3.4 The construction of detector chamber

An amplifier circuit is provided in two partial circuits. One is preamplifier, the other is a main amplifier. The charge sensitive type preamplifier converts the ionized-charge which is developed in the detector during each absorbed photon event into a step pulse output which the amplitude is proportional to the total accumalated-charges in the event. The main amplifier stage

functions as a selectable gain and serves to shape the pulse. The filter shaping network is used to refine and make the pulse symmetry, minimize the variation of output amplitude in detector rise time and maximize signal to noise ratio. Unipolar shaping is achieved by a differentiator and two integrators. Fig. 3.5 shows the pulse waveforms of amplifier.

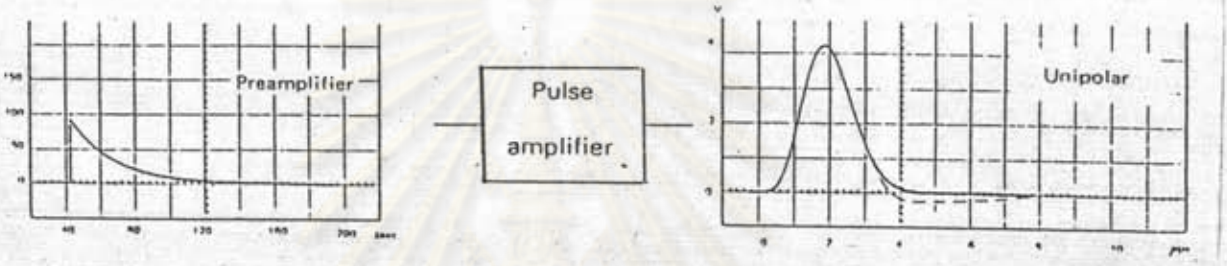

Fig. 3.5 Pulse waveform of amplifier.

The pulse height analyzer consists of two units of single channel analyzer. The first channel and the second one provide the energy window of sulfur X-ray spectral line and lead X-ray spectral line, respectively. Each unit of SCA analyses the peak amplitude of energy pulses from the pulse amplifier independently and generates its primary logic output from input analog pulses between the levels referenced by the lower level (E) and window (ΔE) ten-turn potentiometer controls. The reference levels for the comparison of coming pulses are called lower level and upper level discriminators, respectively. The function of single channel analyzer is shown in Fig. 3.6

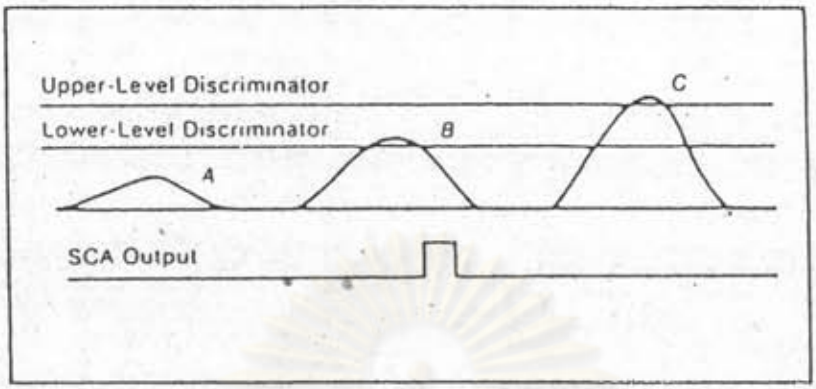

Fig. 3.6 Single channel analyzer function

Data display unit is the last stage of two channel analyzer, it contains of 5-digit counter and timer with preset controls. The counter simply counts the number of SCA output pulse during counting period while the timer establishes the duration time of the counting period. The data display is accumulated in counts per unit of time.

3.3 Circuit Operation of Two Channel Analyzer.

Two channel analyzer circuit is shown in Fig. 3.1 and 3.2, which can be devided into five partial circuits, as follows:

a) Preamplifier and amplifier.

b) Single channel analyzer.

c) Counter and timer.

d) High voltage power supply.

e) Low voltage power supply.

All circuits are shown from Fig. A.1 to A.8 in Appendix A.

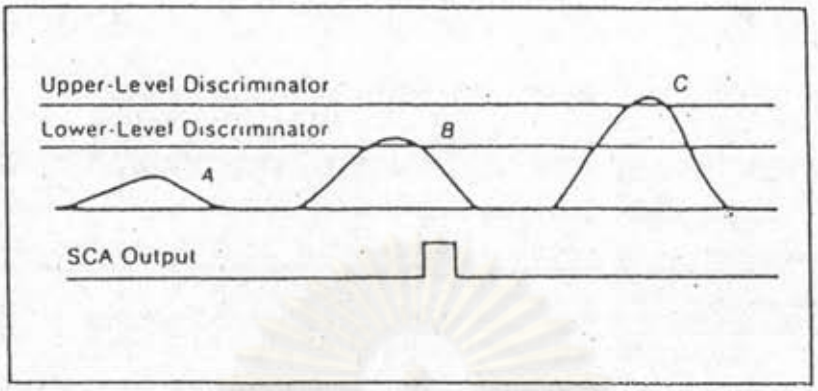

Fig. 3.6 Single channel analyzer function

Data display unit is the last stage of two channel analyzer, it contains of 5-digit counter and timer with preset controls. The counter simply counts the number of SCA output pulse during counting period while the timer establishes the duration time of the counting period. The data display is accumulated in counts per unit of time.

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3.3.1. Preamplifier and Amplifier[6]

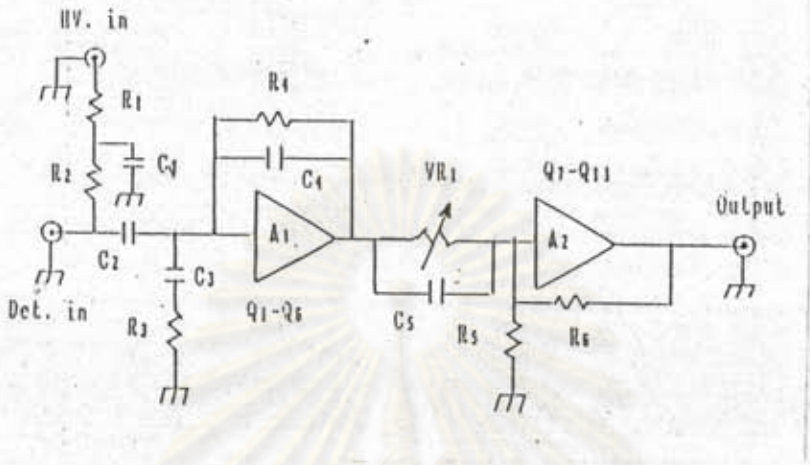

Fig. 3.7 Functional schematic of preamplifier

The circuit diagram of preamplifier can be written into functional diagram as shown in Fig. 3.7. The first stage functions as a charge to voltage converter. R_1, R_2 and C_3 form as decoupling network for supply detector bias voltage. Q_1 through Q_6 are provided a large voltage gain, as an operational amplifier. C_4 closes the loop as the feedback and C_3 acts as the source impedance. The voltage gain can be calculated by,

$$A_v = \frac{-C_3}{C_4}$$

and

$$V_o = \frac{-Qe^{-t/R_4C_4}}{C_4}$$

The resistor R_4 is required for discharge the accumulated charge at each photon event in C_4 in order to prevent the saturation output of preamplifier. The second stage, pole/zero stage, is used to compensate the storage charge in coupling network for optimum baseline operation. VR_1, C_5 and R_5 are formed as the differentiator circuit with a pole/zero adjustment. R_5 and C_5 are responsible for adding the nominal 50 μs tail pulse. The last stage, buffer stage, consists of Q_7 through Q_{11}. It is configured the operational amplifier approach. The loop is closed by both R_6 and R_5 as a non-inverting amplifier. The gain can be determined by

$$A_v = \frac{R_5 + R_6}{R_5}$$

In preamplifier, the charge signal from detector enters at C_2 and converts to voltage pulse. The pulse is amplified and shaping at A_1, A_2 and shaped at C_5, R_5

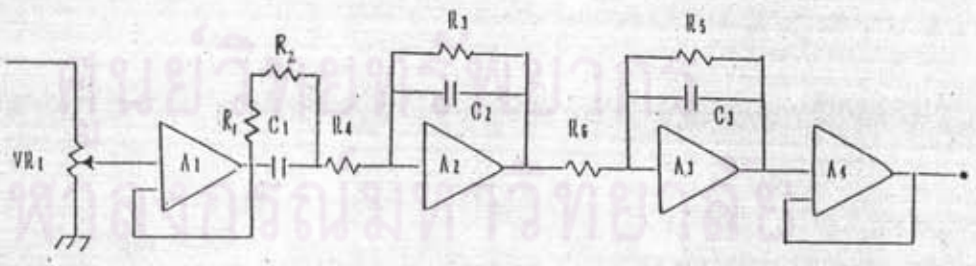

Fig. 3.8 Functional schematic of amplifier.

The pulse signal from preamplifier with long decay time constant, comes to the first stage. Being buffer for the gain control (VR_1), A_1 provides unity gain. The pulse from A_1 stage are differentiated between A_1, A_2. Pole/zero compensation (R_1, C_1, R_2) is also performed in the coupling. A_2 is operated as an inverting loop with the voltage gain of $\frac{R_3}{R_4} \approx 10$. A_3 is the second gain stage of amplifier, its inverting loop has the voltage gain of $\frac{R_5}{R_6} \approx 10$. The total gain of amplifier is about $A_1 x A_2 \approx 100$. The two loop gains of A_2 and A_3 have C_2 and C_3 across feedback resistors for pulse integration. However, the combination between the first stage differentiator and pulse integrator are provided the unipolar pulse nearly Gaussian with the pulse width about 2 μs. The linear range of pulse height amplitude (energy pulse) 0-10 volts is seperated in 2 ways: CH.1 of SCA, and CH.2 of SCA.

3.3.2 Single Channel Analyzer

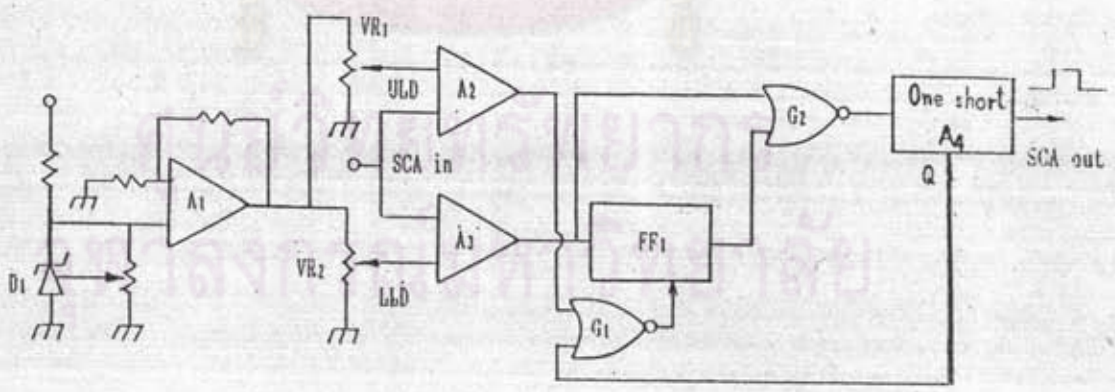

Fig. 3.9 Functional schematic of single channel analyzer.

The energy pulses from amplifier can be analysed by comparing the peak voltage level of those input pulses to the stable DC. reference voltage which provides by zener diode D_1 and A_1 at 10 volts. The comparisons are made for low level discriminator (LLD) and upper level discriminator (ULD), by setting of VR_2 and VR_1, respectively. The pulse discrimination takes place in the precision dual comparator A_2, A_3. In case of the pulse height exceeds the LLD reference level only, the LLD output on A_2 is generated and triggered the clock FF_1 and G_2. The tailing edge of LLD signal on G_2 is used to initiate one short A_4. This one short is set at 0.5 μs. nominal for SCA output. At the same time, Q output from one short goes to G_1 to reset FF_1 for the initial start of new pulse. If the pulse height exceeds both LLD and ULD reference level, the ULD output on A_2 is generated and reset FF_1 before generating the SCA out. The SCA of two channel analyzer is operated in normal mode, using LLD and ULD to set the energy window.

3.3.3 Scaler and Timer.

The scaler stage consists of a real time 5-decade counter, decoder, display, leading zero suppress and control gate, as shown in Fig. 3.12. A real time 5-decade counter is LSI chip MC 14534B. It is a complementary MOS circuit which is composed of five decade ripple counters that have their respective output times multiplexed using an internal scanner. BCD output

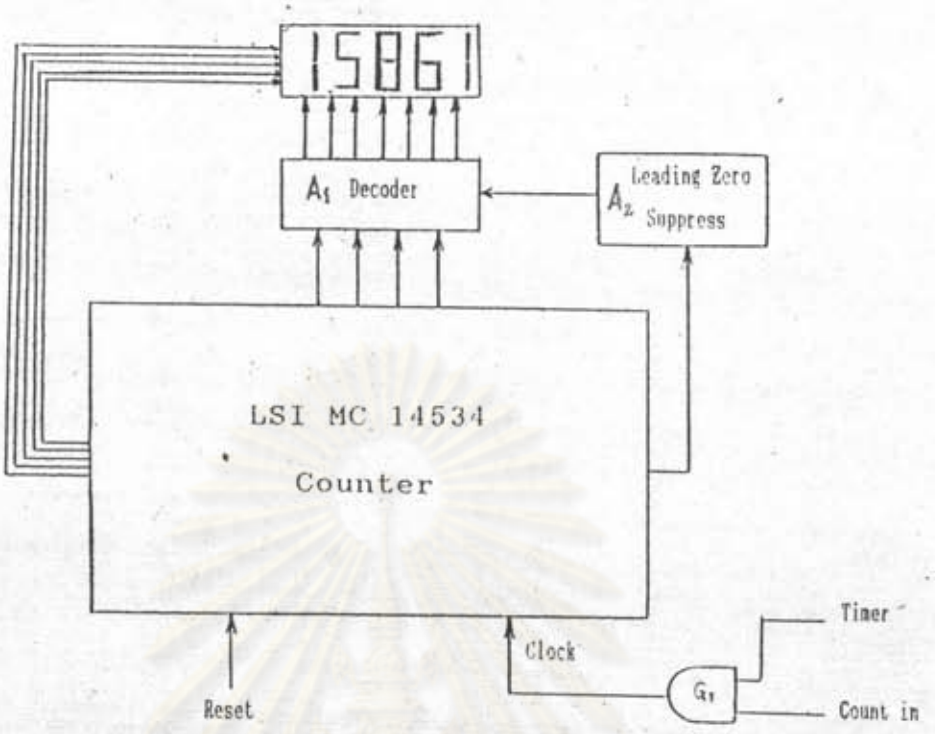

Fig. 3.10 Functional schematic of scaler.

of each counter is fed to decoder A_1, and converts into seven segment readout code. The readout lines of 7-segment code is connected to the common cathode LED 5 digit display. The digit select is controlled by digit scanner. G_1 acts as control gate, one of input gate receives the SCA output and the other one controls counting period by the timer. In order to reduce the power consumption on display, the leading zero is blanked by leading zero suppressed circuit.

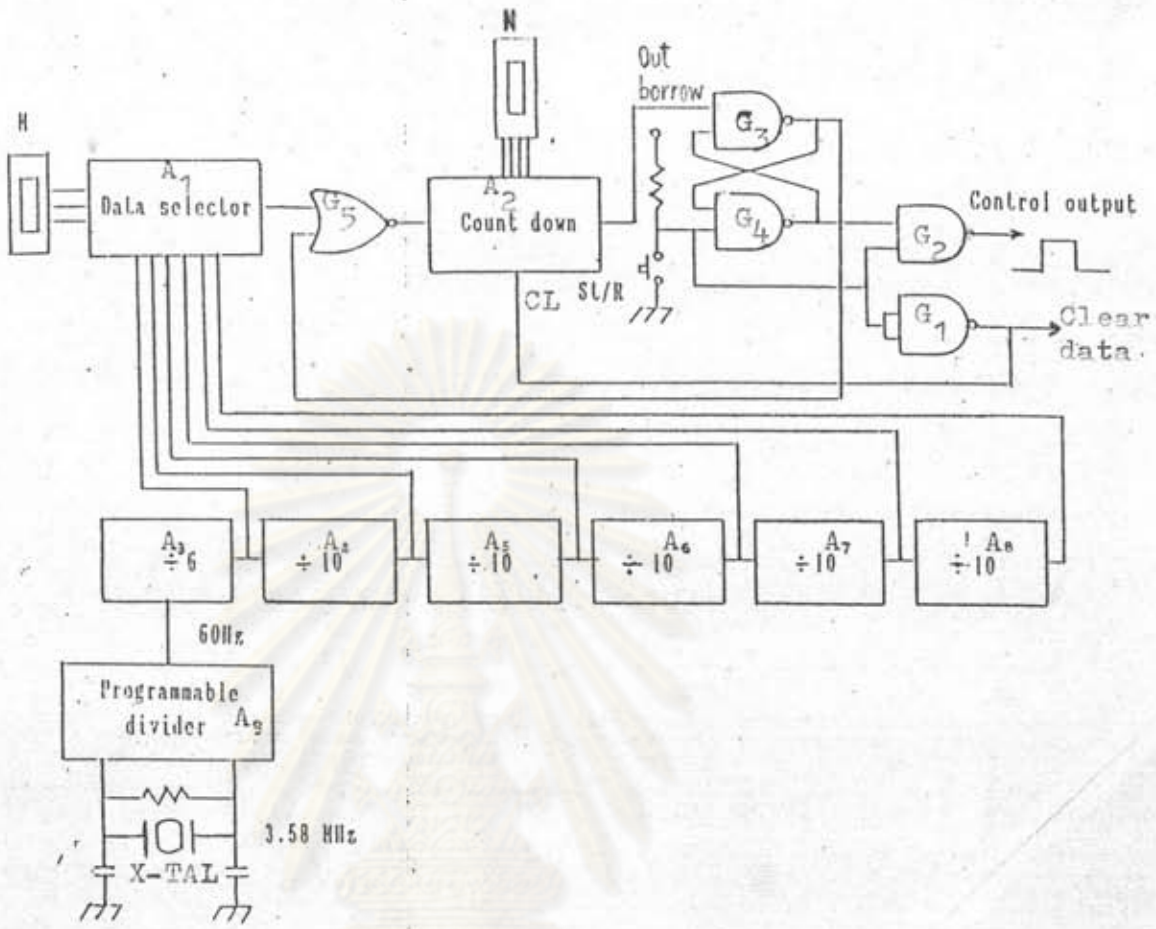

Fig. 3.11 Functional schematic of timer

Functional schematic of timer in Fig. 3.13 consists of time base and preset timer section. The precision timebase is provided by the quartz crystal control oscillator (3.58 MHz) with a programmable divider which generates the frequency of 60 Hz. To obtain the selectable step of interval time, the output frequency of time base section is divided in step of divided by 6, and 5 stages of divided by 10.

The preset time can be selected by BCD-thumbwheel switch ($Nx10^M$) in range of $1\text{-}9x10^4$ seconds. With a series of decade divider, each output will present 10^0, 10^1, 10^2, 10^3 and 10^4 period of time. These periods are used for controlling the index of 10^M by BCD-thumbwheel at data selector (A_1). The selected data output are fed to the presettable countdown (A_2) and set by BCD-thumbwheel switch (N) at input gate. The borrow output, when the countdown goes to zero, is used to reset R-S latch. The interval time which generates during start and stop mode, is a counting period.

3.3.4. High Voltage Power Supply

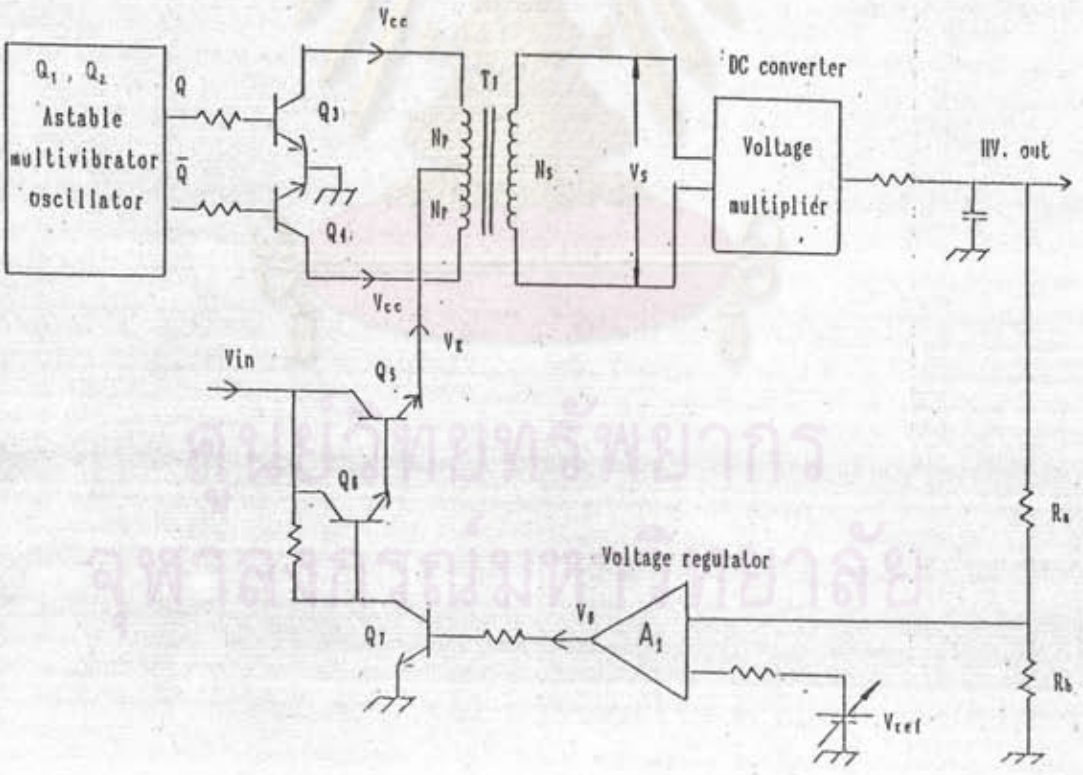

Fig. 3.12 Functional schematic of high voltage power supply

The detector bias supply or high voltage power supply can be divided in 2 main parts, as shows in Fig.3.14, DC.to DC. converter and voltage regulator. In the first part, DC to DC converter, Q_1 and Q_2 acts as astable multivibrator which converts DC. voltage supply to AC. square wave with the frequency of 7 kHz. The output of Q_1 and Q_2 is alternated drive the base of Q_3 and Q_4, operates in switching mode, supply current in the primary winding of T_1 alternately. The ferrite core transformer will induce the secondary winding (turn ratio 1:100) and generate induced voltage Vs which can be express in term of: $V_s = \frac{N_s(V_E - V_{CE_{sat}})}{N_P}$

Because of the limitation of breakdown voltage of insulation in core, the induced voltage Vs is limited. So, the higher voltage can be achieved by voltage multiplier. the set of D_1C_1 through D_2C_2 form as the quadrupler voltage multiplier gives 4 Vs direct current.

The voltage regulator consists of voltage comparator A_1, series transistor Q_5, Q_6 and reference voltage network. To keep the stability of high voltage output, the sampling voltage from divider network of R_a, R_b is fed to voltage comparator A_1. The comparing output of A_1 between sampling voltage and reference voltage is fed to control Q_5 and Q_6 to compensate V_E. The high voltage output is varied by varying the voltage reference, V_{ref}.

3.3.5. Low Voltage Power Supply

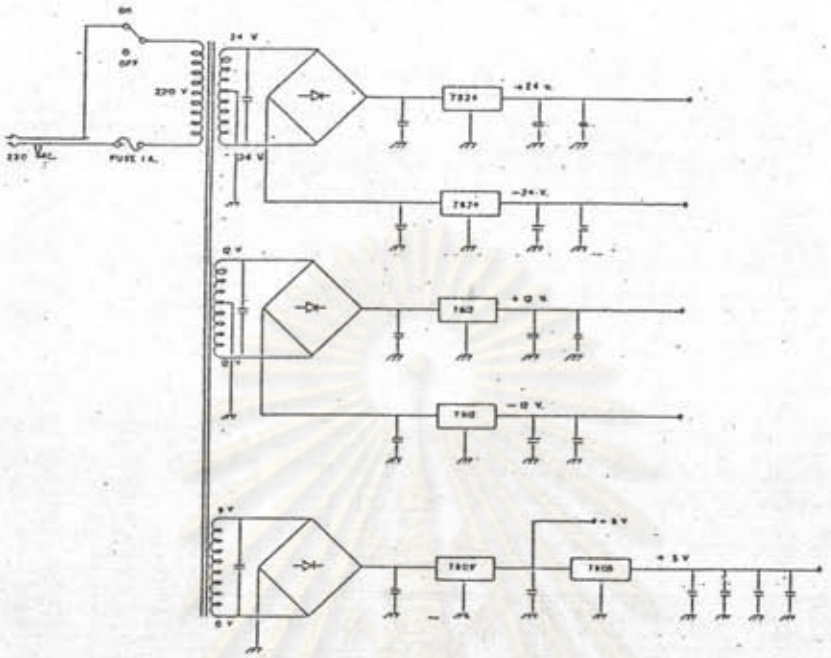

Fig. 3.13 Functional schematic of LV. power supply.

The low voltage power supply is an importance part for energizing all circuits of two channel analyzer. The LV. power supply consists of step down tranformer, line filter, rectifier diode, filter capacitor and voltage regulator, as shown in Fig. 3.15. It is generated the 4 sets of regulated output; ±24.V, ±12V., +9, and +5V., using the three terminals regulator.