เอกสารอ้างอิง

[1] Rectifier and thyrister data book, Toshiba corporation semiconductor group, Tokyo, Japan, 1983

[2] วิชัย ตังขจันทรานนท์, การควบคุมเครื่องกลไฟฟ้าด้วยอิเล็กทรอนิกส์กำลัง 1, สมาคมส่งเสริมเทคโนโลยี (ไทย-ญี่ปุ่น), กทม., 2528

[3] Dewan, S.B., and A. Straughen, Power semiconductor circuits, John Wiley & Sons, N.Y.,1975

[4] Pelly B.R., Thyrister phase controlled converters and cycloconverters, John Wiley & Sons, N.Y., 1971

[5] มงคล เดชนครินทร์, วิชัย ตังขจันทรานนท์ และ วิจิตรวรรณ ประกอบสันติสุข, การออกแบบและสร้างเครื่องต้นแบบของไซโคลคอนเวอร์เตอร์แบบเฟสเดียว, รายงานวิจัยในโครงการวิจัยเพื่อเพิ่มพูนและพัฒนาประสิทธิภาพทางวิชาการ ฝ่ายวิจัยจุฬาลงกรณ์มหาวิทยาลัย, กันยายน 2530

[6] Chen, H. H., A microprocessor control of a three-pulse cycloconverter, IEEE Trans. Indus. Electron. Control instrum., Vol. IECI-24, No. 3, August 1977.

[7] Matouka, M. F., Read-only memory (ROM) trigger generator for phase-controlled cycloconverters, IEEE Trans. Indus. Electron. Control Instrum., Vol. IECI-25, No. 2, May 1978

[8] Singh, D., and R. G. Hoft, Microcomputer-controlled single-phase cycloconverter, IEEE Trans. Indus. Electron. Control Instrum., Vol. IECI-25, No. 3, August 1978

[9] Akagi, H., Fujita, M., Fukao, T., and Miyairi, S., Application of microcomputer to current-controlled cycloconvertor system, Electr. Eng. Jpn., 1980

[10] Kurosawa, R., Shimamura, T., Uchino H., and Sugi, K., Microcomputer-based high power cycloconvertor-fed induction motor drive, IEEE-IAS Annual Meeting, 1982

[11] Ali Mirbod and Ahmed El-amawy, Performance analysis of a novel microprocessor-based controller for a phase-controlled rectifier connected to a weak AC system, IEEE Trans Ind. Appl., Vol. IA-23, 1987

[12] S. B. Dewan and W. G. Dunford, A microprocessor-based controller for a three phase controlled rectifier bridge, IEEE Trans Ind. Appl., Vol IA-19, 1983

[13] วิชัย ตังขจันทรานนท์, การควบคุมเครื่องกลไฟฟ้าด้วยอิเล็กทรอนิกส์กำลัง 2, สมาคมส่งเสริมเทคโนโลยี (ไทย-ญี่ปุ่น), กทม., 2528

[14] โคทม อารียา, วงจรอินเวอร์เตอร์, เอกสารประกอบการฝึกอบรมทางวิชาการ เรื่อง Power Electronics & Applications, สมาคมส่งเสริมเทคโนโลยี (ไทย-ญี่ปุ่น), กทม., 1 - 3 มิถุนายน 2530

[15] G.P. Hunter, V.S. Ramsden, New improved modulation method for a cycloconvertor driving an induction motor, IEE PROCEEDING, Vol. 135, NOVEMBER 1988

[16] Allan, J. A., W. A. Wyeth, G. W. Herzog, and J. A. I. Young, Electrical aspects of the 8750 Hp gearless ball-mill drive at St. Lawrence Cement Company, IEEE Trans. Ind. Appl., Vol. IA-11, Nov./Dec. 1975

[17] Rice, J. B., Design of snubber circuits for thyristor converters, Power Semiconductor Applitions, Vol. I: General Considerations, edited by J. D. Harnden, Jr., and F. B. Golden, IEEE Press, N.Y.,1972,

[18] Locher, R. E., and M. W. Smith(editors), Thyristors-rectifiers, Semiconductor Products Department, General Electric Co., N.Y., 1982

[19] Millman, J., and H. Taub, Pulse, Digital, and Switching Waveforms, McGraw-Hill, N.Y., 1965

[20] Microprofessor MPF-IP User's Manual, Multitech industrial Corp., Taipei, Taiwan, 1983

[21] ไอซี TTL, ซีเอ็ดยูเคชั่น, กทม., 2526

[22] Linear Databook, National Semiconductor Corp., Santa Clara, California, 1982

[23] กฤษดา วิศวธีรานนท์ และ ยืน ภู่วรวรรณ (บรรณาธิการ), ไมโครโปรเซสเซอร์, สมาคมส่งเสริมเทคโนโลยี(ไทย-ญี่ปุ่น), กทม., 2524

[24] ยืน ภู่วรวรรณ และ วัฒนา เชียงกูล, ไมโครโปรเซสเซอร์ ไมโครคอมพิวเตอร์, ซีเอ็ดยูเคชั่น, กทม., 2525

ข้อมูลเกี่ยวกับไอซีเบอร์ 7400

5400/7400 Quadruple 2-Input Positive-NAND Gate

	Schottky TTL					High-Speed TTL					Low-Power Schottky TTL					Standard TTL					Low-Power TTL				
	Device Type	Package C	P	M	CF	Device Type	Package C	P	M	CF	Device Type	Package C	P	M	CF	Device Type	Package C	P	M	CF	Device Type	Package C	P	M	CF
T.I.	SN54S00	J①	N①		W①	SN54H00	J①			W①	SN54LS00	J①			W①	SN5400	J①			W②	SN54L00	J①	N①	T②	
	SN74S00	J①	N①			SN74H00	J①	N①			SN74LS00	J①	N①			SN7400	J①	N①			SN74L00	J①	N①	T②	
FAIRCHILD	FM54S00/FM9S00	D①				FM54H00/FM9H00	D①			F②	FM54LS00/FM9LS00	D①			F①	FM 5400/FM9N00	D①			F②					
	FC74S00/FC9S00	D①	P①			FC74H00/FC9H00	D①	P①			FC74LS00/FC9LS00	D①	P①		F①	FC7400/FC9N00	D①	P①							
MOTOROLA						MC3100	L①			F②						MC5400	L①			F②					
						MC3000	L①	P①		F②	SN74LS00		P①			MC7400	L①	P①		F②					
N.S.C.						DM54H00	J①	N①			DM54LS00					DM5400	J①	N①		W②	DM54L00	J①	N①		F②
	DM74S00		N①			DM74H00	J①	N①			DM74LS00					DM7400	J①	N①			DM74L00	J①	N①		F②
PHILIPS	N74S03		①			GJH131/74H00		①			N74LS00		①			FJH131/7400		①							
SIGNETICS	N54S00	F①	A①		W①	S54H00	F①	A①		W②						S5400	F①	A①		W②					
	N74S00	F①	A①			N74H00	F①	A①			N74LS00		A①			N7400	F①	A①							
SIEMENS																									
																FLH101		①							
FUJITSU																									
						MB601		①	M①		74LS00		M①			MB400		①	M①						
HITACHI																									
	HD74S00		①	P①							HD74LS00		P①			HD7400/HD2503		①	P①						
MITSUBISHI																									
	M5S000			P①							M74LS00		P①			M53200			P①						
NEC																									
	μPB2S00	D①									74LS00		C①			μPB201	D①		C①						
TOSHIBA																									
																TD3400A			P①						

Electrical Characteristics SN54LS00/SN74LS00

absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC}	7V	Operating free-air temperature range	SN54LS	−55°C to 125°C
Input voltage	7V		SN74LS	0°C to 70°C
Interemitter voltage	5.5V	Storage temperature range		−65°C to 150°C

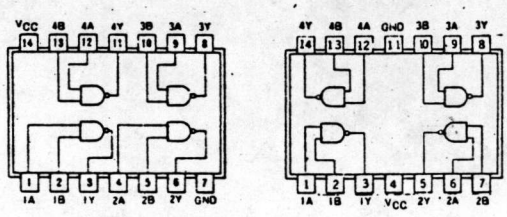
recommended operating conditions

	SN54LS00 MIN	NOM	MAX	SN74LS00 MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range

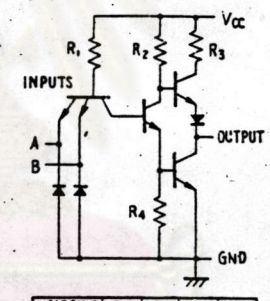
PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC}=MIN, I_I=−18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC}=MIN, V_{IL}=V_{IL} max, I_{OH}=MAX		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC}=MIN, V_{IH}=2V, I_{OL}=4mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC}=MAX, V_I=7V				0.1	mA
I_{IH}	High-level input current	V_{CC}=MAX, V_{IH}=2.7V				20	μA
I_{IL}	Low-level input current	V_{CC}=MAX, V_{IL}=0.4V				−0.4	mA
I_{OS}	Short-circuit output current●	V_{CC}=MAX	54LS Family	−20		−100	mA
			74LS Family	−18		−100	
I_{CCH}	Supply current	V_{CC}=MAX	Total, outputs high		4	8	mA
I_{CCL}	Supply current		Total, outputs low		12	22	mA
I_{CC}	Supply current	V_{CC}=5V	Average per gate (50% duty cycle)		0.4		mA
t_{PLH}	Propagation delay time, low-to-high-level output	V_{CC}=5V, C_L=15pF,	T_A=25°C, R_L=2kΩ		9	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output				10	15	ns

Pin Assignments (Top View)



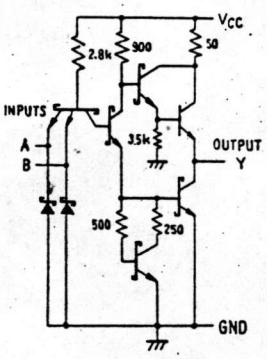
positive logic:
$Y = \overline{AB}$

Schematics (each gate)

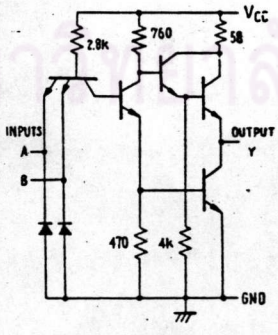


CIRCUIT	R_1	R_2	R_3	R_4
'00	4k	1.4k	130	1k
'L00	40k	20k	500	12k

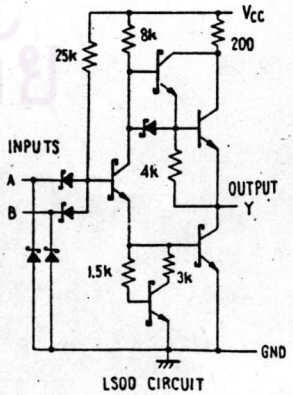
Input clamp diodes not on SN54L'/SN74L' circuits.
'00, 'L00 CIRCUITS



'S00 CIRCUIT



'H00 CIRCUIT



LS00 CIRCUIT

Resistor values shown are nominal and in ohms.

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC}=5V, T_A=25°C.
● Not more than one output should be shorted at a time, and for SN54H'/SN74H' and SN54S'/SN74S', duration of short-circuit should not exceed 1 second.

ภาคผนวก 2
ข้อมูลเกี่ยวกับไอซีเบอร์ LM339

National Semiconductor

Voltage Comparators

LM139/239/339, LM139A/239A/339A, LM2901,LM3302 Low Power Low Offset Voltage Quad Comparators

General Description

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic– where the low power drain of the LM339 is a distinct advantage over standard comparators.

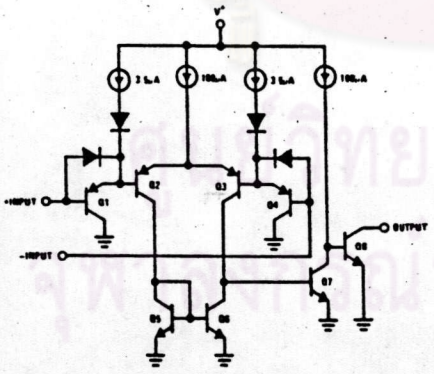
Advantages

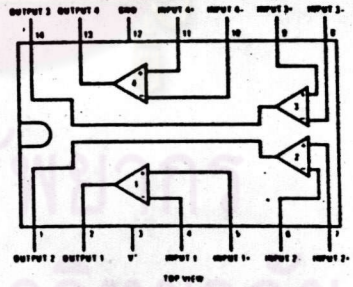
- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near gnd
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Wide single supply voltage range or dual supplies
  LM139 series, 2 V_{DC} to 36 V_{DC} or
  LM139A series, LM2901 ±1 V_{DC} to ±18 V_{DC}
  LM3302 2 V_{DC} to 28 V_{DC} or ±1 V_{DC} to ±14 V_{DC}
- Very low supply current drain (0.8 mA) — independent of supply voltage (2 mW/comparator at +5 V_{DC})
- Low input biasing current 25 nA
- Low input offset current ±5 nA
  and offset voltage ±3 mV
- Input common-mode voltage range includes gnd
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

Schematic and Connection Diagrams



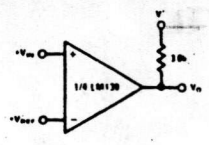


Dual-In-Line and Flat Package

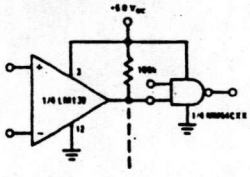
Order Number LM139J, LM139AJ, LM239J, LM239AJ, LM339J, LM339AJ, LM2901J or LM3302J
See NS Package J14A

Order Number LM339N, LM339AN, LM2901N or LM3302N
See NS Package N14A

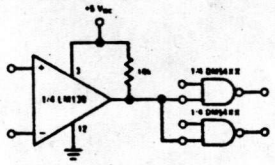
Typical Applications (V^+ = 5.0 V_{DC})



Basic Comparator



Driving CMOS



Driving TTL

Absolute Maximum Ratings

	LM139/LM239/LM339 LM139A/LM239A/LM339A LM2901	LM3302
Supply Voltage, V^+	36 V_{DC} or ±18 V_{DC}	28 V_{DC} or ±14 V_{DC}
Differential Input Voltage	36 V_{DC}	28 V_{DC}
Input Voltage	−0.3 V_{DC} to +36 V_{DC}	−0.3 V_{DC} to +28 V_{DC}
Power Dissipation (Note 1)		
Molded DIP	570 mW	570 mW
Cavity DIP	900 mW	
Flat Pack	800 mW	
Output Short-Circuit to GND, (Note 2)	Continuous	Continuous
Input Current (V_{IN} < −0.3 V_{DC}), (Note 3)	50 mA	50 mA
Operating Temperature Range		
LM339A	0°C to +70°C	−40°C to +85°C
LM239A	−25°C to +85°C	
LM2901	−40°C to +85°C	
LM139A	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

Electrical Characteristics (V^+ = 5 V_{DC}, Note 4)

PARAMETER	CONDITIONS	LM139A			LM239A, LM339A			LM139			LM239, LM339			LM2901			LM3302			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	T_A = 25°C, (Note 9)		±1.0	±2.0		±1.0	±2.0		±2.0	±5.0		±2.0	±5.0		±2.0	±7.0		±3	±20	mV_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, T_A = 25°C, (Note 5)		25	100		25	250		25	100		25	250		25	250		25	500	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, T_A = 25°C		±3.0	±25		±5.0	±50		±3.0	±25		±5.0	±50		±5	±50		±3	±100	nA_{DC}
Input Common-Mode Voltage Range	T_A = 25°C, (Note 8)	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	V_{DC}
Supply Current	R_L = ∞ on all Comparators, T_A = 25°C		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2	mA_{DC}
	R_L = ∞, V^+ = 30V, T_A = 25°C														1	2.5				mA_{DC}
Voltage Gain	$R_L \geq 15\ k\Omega$, V^+ = 15 V_{DC} (To Support Large V_O Swing), T_A = 25°C	50	200		50	200			200			200		25	100		2	30		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = 1.4 V_{DC}, V_{RL} = 5 V_{DC}, R_L = 5.1 kΩ, T_A = 25°C		300			300			300			300			300			300		ns
Response Time	V_{RL} = 5 V_{DC}, R_L = 5.1 kΩ, T_A = 25°C, (Note 7)		1.3			1.3			1.3			1.3			1.3			1.3		µs
Output Sink Current	$V_{IN(-)} \geq 1\ V_{DC}$, $V_{IN(+)}$ = 0, $V_O \leq 1.5\ V_{DC}$, T_A = 25°C	6.0	16		6.0	16		6.0	16		6.0	16		6.0	16		6.0	16		mA_{DC}
Saturation Voltage	$V_{IN(-)} \geq 1\ V_{DC}$, $V_{IN(+)}$ = 0, $I_{SINK} \leq 4$ mA, T_A = 25°C		250	400		250	400		250	400		250	400			400		250	500	mV_{DC}
Output Leakage Current	$V_{IN(+)} \geq 1\ V_{DC}$, $V_{IN(-)}$ = 0, V_O = 5 V_{DC}, T_A = 25°C		0.1			0.1			0.1			0.1			0.1			0.1		nA_{DC}

Electrical Characteristics (Continued)

PARAMETER	CONDITIONS	LM139A			LM239A, LM339A			LM139			LM239, LM339			LM2901			LM3302			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	(Note 9)			4.0			4.0			9.0			9.0		9	15			40	mV_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			±100			±150			±100			±150		50	200			300	nA_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range			300			400			300			400		200	500			1000	nA_{DC}
Input Common-Mode Voltage Range		0		$V^+-2.0$	0		$V^+-2.0$	0		$V^+-2.0$	0		$V^+-2.0$	0		$V^+-2.0$	0		$V^+-2.0$	V_{DC}
Saturation Voltage	$V_{IN(-)} \geq 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4\ mA$			700			700			700			700		400	700			700	mV_{DC}
Output Leakage Current	$V_{IN(+)} \geq 1\ V_{DC}$, $V_{IN(-)} = 0$, $V_O = 30\ V_{DC}$			1.0			1.0			1.0			1.0			1.0			1.0	μA_{DC}
Differential Input Voltage	Keep all V_{IN}'s $\geq 0\ V_{DC}$ (or V^-, if used), (Note 8)			36			36			36			36	0		36			28	V_{DC}

Note 1: For operating at high temperatures, the LM339/LM339A, LM2901, LM3302 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM239 and LM139 must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100\ mW$), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3\ V_{DC}$ (at 25°C).

Note 4: These specifications apply for $V^+ = 5\ V_{DC}$ and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. With the LM239/LM239A, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the LM339/LM339A temperature specifications are limited to $0°C \leq T_A \leq +70°C$, and the LM2901, LM3302 temperature range is $-40°C \leq T_A \leq +85°C$.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$, but either or both inputs can go to $+30\ V_{DC}$ without damage (25V for LM3302).

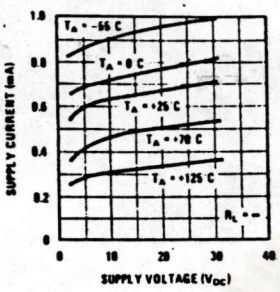
Note 7: The response time specified is a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3\ V_{DC}$ (or $0.3\ V_{DC}$ below the magnitude of the negative power supply, if used) (at 25°C).

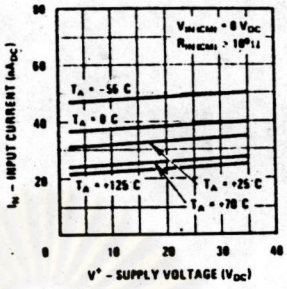
Note 9: At output switch point, $V_O \cong 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from $5\ V_{DC}$; and over the full input common-mode range ($0\ V_{DC}$ to $V^+ - 1.5\ V_{DC}$).

Typical Performance Characteristics LM139/LM239/LM339, LM139A/LM239A/LM339A, LM3302

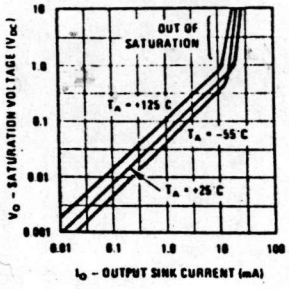
Supply Current



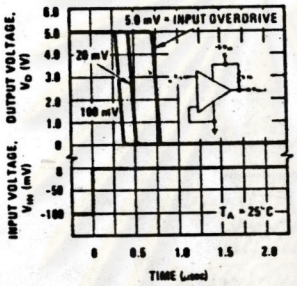
Input Current



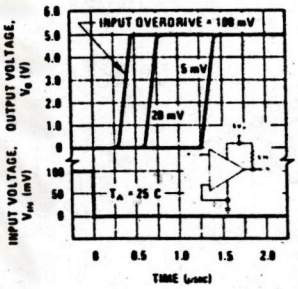
Output Saturation Voltage



Response Time for Various Input Overdrives – Negative Transition

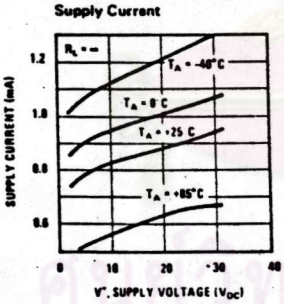


Response Time for Various Input Overdrives – Positive Transition

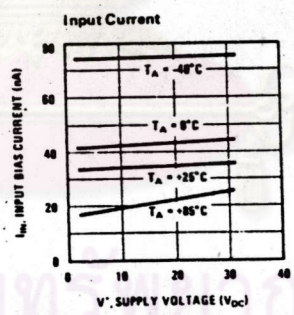


Typical Performance Characteristics LM2901

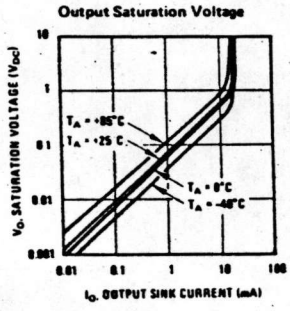
Supply Current



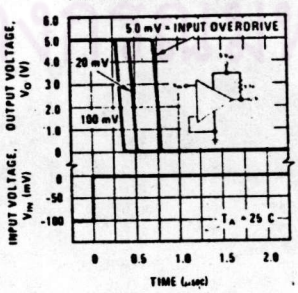
Input Current



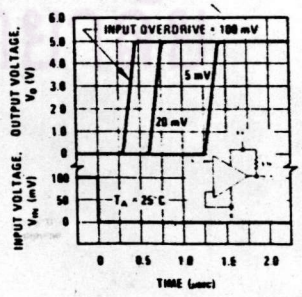
Output Saturation Voltage



Response Time for Various Input Overdrives–Negative Transition



Response Time for Various Input Overdrives–Positive Transition



ภาคผนวก 3

ข้อมูลเกี่ยวกับไอซีเบอร์ 74121

54121/74121 Monostable Multivibrator with Schmitt-Trigger Input

	Schottky TTL					High-Speed TTL					Low-Power Schottky TTL					Standard TTL					Low-Power TTL				
	Device Type	C	P	M	CF	Device Type	C	P	M	CF	Device Type	C	P	M	CF	Device Type	C	P	M	CF	Dexice Type	C	P	M	CF
TI																SN54121	J1			W1	SN54L121	J1	N1	T1	
																SN74121	J1	N1			SN74L121	J1	N1	T1	
FAIRCHILD																FM54121·FM9603	D1			F1					
																FC74121 FC9603	D1	P1							
MOTOROLA																MC54121	L1			F1					
																MC74121	L1	P1		F1					
N.S.C.																DM54121	J1	N1		W1					
																DM74121	J1	N1							
PHILIPS																									
																FJK101/74121		①							
SIGNETICS																S54121	F1	A1		W1					
																N74121	F①	A①		W1					
SIEMENS																									
																FLK101		①							
FUJITSU																									
HITACHI																									
																HD74121/HD2543	①	P1							
MITSUBISHI																									
																M53321		P①							
NEC																									
TOSHIBA																									
																TD34121A		P1							

Electrical Characteristics SN54S121 SN74S121

absolute maximum ratings over operating free-air temperature range

Supply voltage VCC	7V	Operating free-air temperature range	SN54S	-55°C to 125°C
Input voltage	5.5V		SN74S	0°C to 70°C
		Storage temperature range		-65°C to 150°C

recomended operating conditions

		SN54S121			SN74S121			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage VCC		4.5	5	5.5	4.75	5	5.25	V
High-level output current IOH							[illegible]	[illegible]
LOW-level output current IOL							16	mA
Rate of rise or fall of input pulse, dv/dt	Schmitt input B	1			1			V/s
	Logic inputs A1, A2	1			1			V/μs
Input pulse width tw(in)		50			50			ns
External timing resistance Rext		1.4		30	1.4		[illegible]	kΩ
External timing capacitance Cext		0		[illegible]	0		1000	μF
Duty cycle	RT = 2kΩ			[illegible]			67	%
	RT = MAX Rext			90			90	
Operating free-air temperature, TA		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range

	PARAMETER	TEST CONDITIONS †			MIN	TYP ‡	MAX	UNIT
V_{T+}	Positive-going threshold voltage	V_{CC} = MIN		A input		1.4	2	V
V_{T-}	Negative-going threshold voltage	V_{CC} = MIN		A input	0.8	1.4		V
V_{T+}	Positive-going threshold voltage	V_{CC} = MIN		B input		1.55	2	V
V_{T-}	Negative-going threshold voltage	V_{CC} = MIN		B input	0.8	1.35		V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = -12mA				-1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN,	I_{OH} = MAX		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN,	I_{OL} = MAX			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4V		A1 or A2			40	μA
	High-level input current			B			80	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V		A1 or A2			-1.6	mA
				B			-3.2	mA
I_{OS}	Short-circuit output current •	V_{CC} = MAX		54 Family	-20		-55	mA
				74 Family	-18		-55	
I_{CC}	Supply current	V_{CC} = MAX		Quiescent		13	25	mA
				Triggered		23	40	
t_{PLH}	Propagation delay telme, low-to-high-level Q output from either A input	V_{CC} = 5 V, T_A = 25°C, C_L = 15pF, R_L = 400Ω		C_T = 80 pF, Rint to V_{CC}		45	70	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output from B input					35	55	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from either A input					50	80	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from B input					40	65	ns
$t_{w(out)}$	Pulse width obtained using internal timing resistor	V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 400Ω		C_T = 80nF, Rint to V_{CC}	70	110	150	ns
$t_{w(out)}$	Pulse width obtained with zero timing capacitance			C_T = 0, Rint to V_{CC}		30	50	ns
$t_{w(out)}$	Pulse width obtained using external timing resistor		C_T = 100pF, R_T = 10kΩ		600	700	800	ns
			C_T = 1μF, R_T = 10kΩ		6	7	8	ms

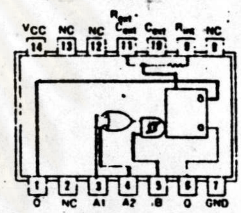
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions

‡ All typical values are at V_{CC} = 5V, T_A = 25°C

• Not more than one output should be shorted at a time

Pin Assignment (Top view)

①



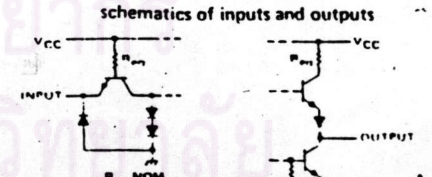
NC-No internal connection
'121···R_{int} = 2 kΩ NOM
L121···R_{int} = 4 kΩ NOM

Function Table

'121, 'L121 (See Note)

INPUTS			OUTPUTS	
A1	A2	B	Q	Q̄
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⎍	⎍
↓	H	H	⎍	⎍
↓	↓	H	⎍	⎍
L	X	↑	⎍	⎍
X	L	↑	⎍	⎍

schematics of inputs and outputs



R_{eq} NOM

INPUT	'121	'L121
A1	4 kΩ	8 kΩ
A2	4 kΩ	8 kΩ
B	2 kΩ	4 kΩ

'121 R_{eq} = 130 Ω NOM
'L121 R_{eq} = 260 Ω NOM

EQUIVALENT OF EACH INPUT — TYPICAL OF BOTH OUTPUTS

NOTES : A H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⎍ = one high-level pulse, ⎍ = one low-level pulse, X = irrelevant (any input, including transitions)

B To use the internal timing resistor connect R_{int} to V_{CC}.

C An external timing capacitor may be connected between C_{ext} (positive) and R_{ext}/C_{ext}

D For accurate repeatable pulse widths, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.

E To obtain variable pulse widths, connect external values resistance between R_{int} or R_{ext}/C_{ext} and V_{CC}

ภาคผนวก 4
ข้อมูลเกี่ยวกับไอซีเบอร์ LM311

LM311

National Semiconductor

Voltage Comparators

LM311 Voltage Comparator

General Description

The LM311 is a voltage comparator that has input currents more than a hundred times lower than devices like the LM306 or LM710C. It is also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Its output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, it can drive lamps or relays, switching voltages up to 40V at currents as high as 50 mA.

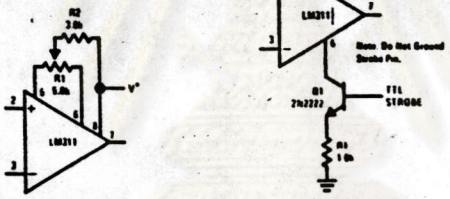
Features

- Operates from single 5V supply
- Maximum input current: 250 nA
- Maximum offset current: 50 nA
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V

Both the input and the output of the LM311 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM306 and LM710C (200 ns response time vs 40 ns) the device is also much less prone to spurious oscillations. The LM311 has the same pin configuration as the LM306 and LM710C. See the "application hints" of the LM311 for application help.

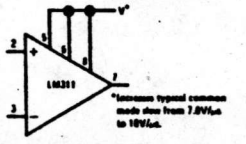
Auxiliary Circuits**

**Note: Pin connections shown on schematic diagram and typical applications are for TO-5 package.



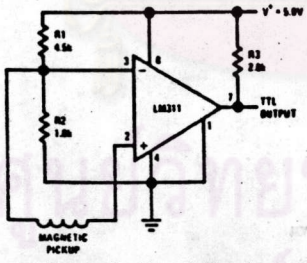
Offset Balancing

Strobing

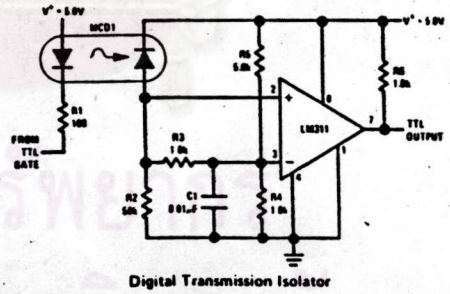


Increasing Input Stage Current*

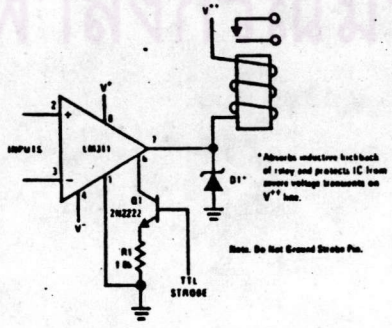
Typical Applications**



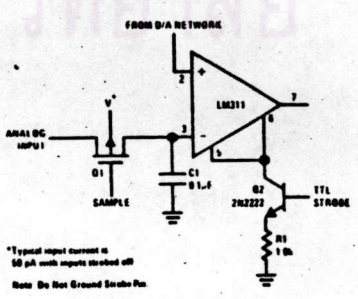
Detector for Magnetic Transducer



Digital Transmission Isolator



Relay Driver with Strobe



Strobing off Both Input* and Output Stages

Absolute Maximum Ratings

Total Supply Voltage (V_{84})	36V
Output to Negative Supply Voltage (V_{74})	40V
Ground to Negative Supply Voltage (V_{14})	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (soldering, 10 sec)	300°C
Voltage at Strobe Pin	V^+−5V

Electrical Characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$		2.0	7.5	mV
Input Offset Current (Note 4)	$T_A = 25°C$		6.0	50	nA
Input Bias Current	$T_A = 25°C$		100	250	nA
Voltage Gain	$T_A = 25°C$	40	200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -10$ mV, $I_{OUT} = 50$ mA $T_A = 25°C$		0.75	1.5	V
Strobe ON Current	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \geq 10$ mV, $V_{OUT} = 35V$ $T_A = 25°C$, $I_{STROBE} = 3$ mA		0.2	50	nA
Input Offset Voltage (Note 4)	$R_S \leq 50k$			10	mV
Input Offset Current (Note 4)				70	nA
Input Bias Current				300	nA
Input Voltage Range		−14.5	13.8,−14.7	13.0	V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -10$ mV, $I_{SINK} \leq 8$ mA		0.23	0.4	V
Positive Supply Current	$T_A = 25°C$		5.1	7.5	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LM311 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 3: These specifications apply for V_S = ±15V and the Ground pin at ground, and 0°C < T_A < +70°C, unless otherwise specified. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

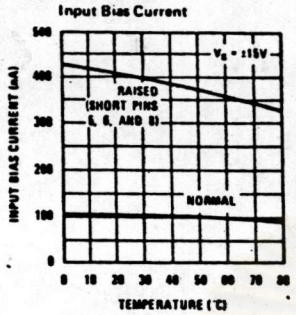
Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

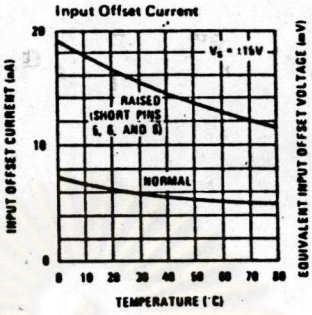
Note 6: Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

Typical Performance Characteristics

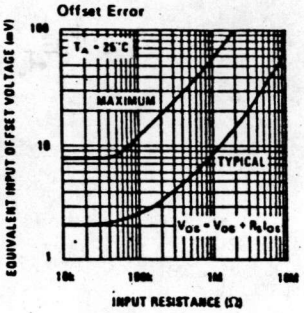
Input Bias Current



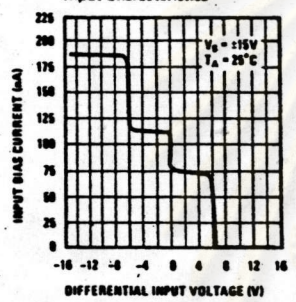
Input Offset Current



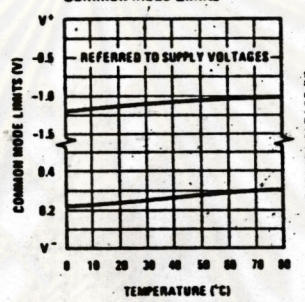
Offset Error



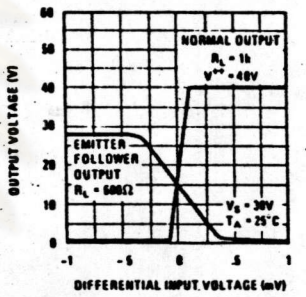
Input Characteristics



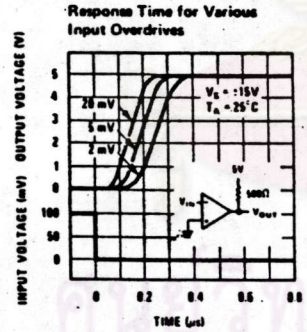
Common Mode Limits



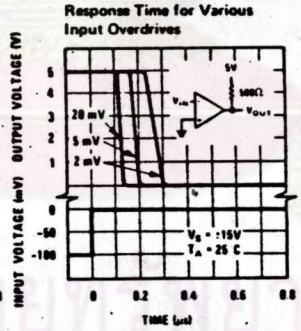
Transfer Function



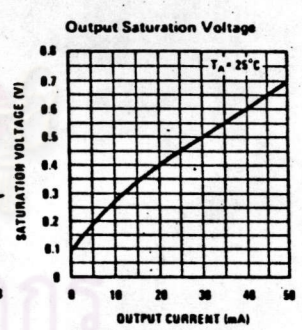
Response Time for Various Input Overdrives



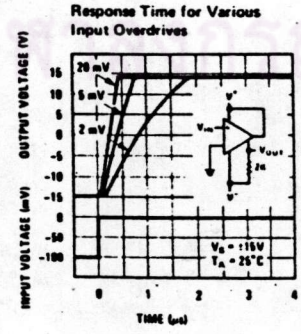
Response Time for Various Input Overdrives



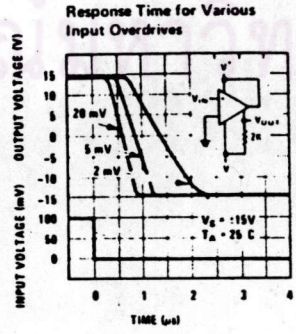
Output Saturation Voltage



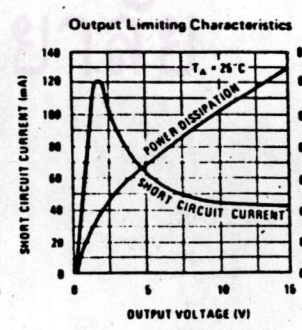
Response Time for Various Input Overdrives



Response Time for Various Input Overdrives

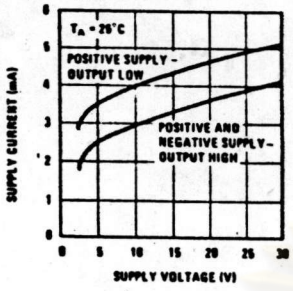


Output Limiting Characteristics

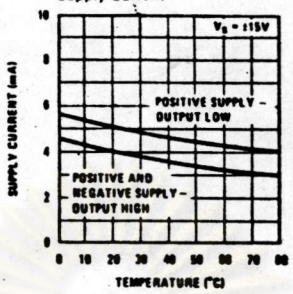


Typical Performance Characteristics (Continued)

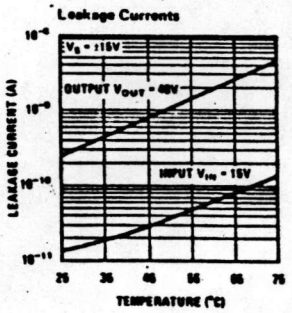
Supply Current



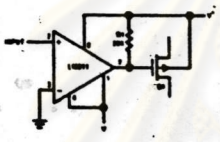
Supply Current



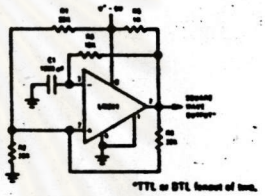
Leakage Currents



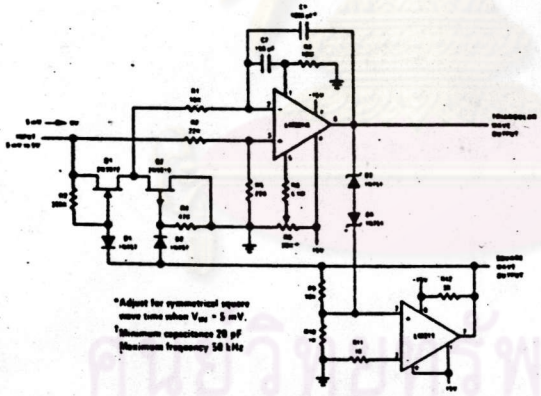
Typical Applications



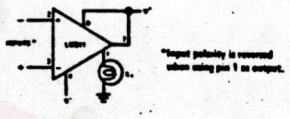
Zero Crossing Detector Driving MOS Switch



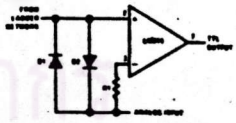
100 kHz Free Running Multivibrator



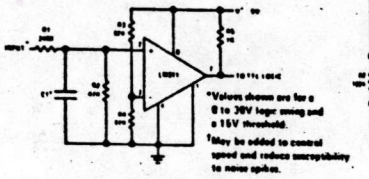
10 Hz to 10 kHz Voltage Controlled Oscillator



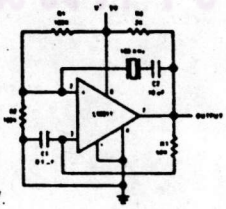
Driving Ground-Referred Load



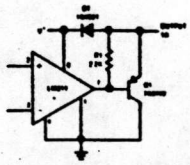
Using Clamp Diodes to Improve Response



TTL Interface with High Level Logic



Crystal Oscillator



Comparator and Solenoid Driver

ภาคผนวก 5

ข้อมูลเกี่ยวกับไอซีเบอร์ 8255

intel Silicon Gate MOS 8255

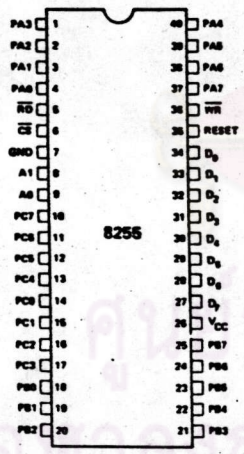
PROGRAMMABLE PERIPHERAL INTERFACE

- 24 Programmable I/O Pins
- Completely TTL Compatible
- Fully Compatible with MCS™-8 and MCS™-80 Microprocessor Families
- Direct Bit Set/Reset Capability Easing Control Application Interface
- 40 Pin Dual In-Line Package
- Reduces System Package Count

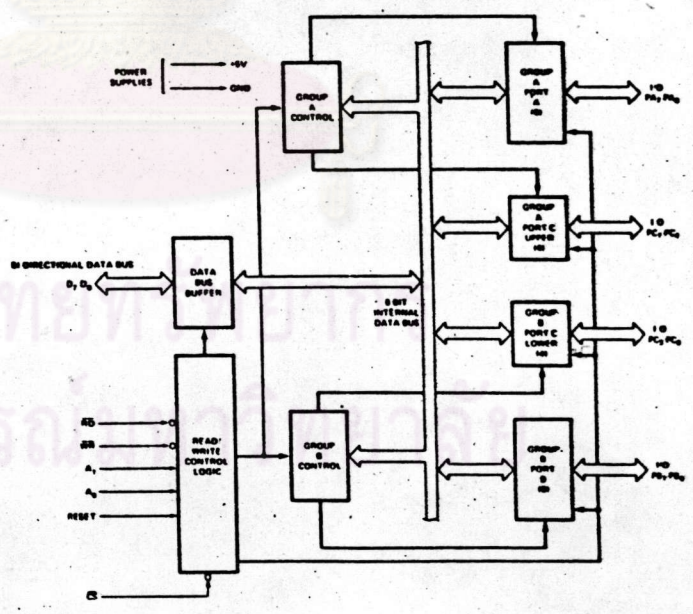
The 8255 is a general purpose programmable I/O device designed for use with both the 8008 and 8080 microprocessors. It has 24 I/O pins which may be individually programmed in two groups of twelve and used in three major modes of operation. In the first mode (Mode 0), each group of twelve I/O pins may be programmed in sets of 4 to be input or output. In Mode 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining four pins three are used for handshaking and interrupt control signals. The third mode of operation (Mode 2) is a Bidirectional Bus mode which uses 8 lines for a bidirectional bus, and five lines, borrowing one from the other group, for handshaking.

Other features of the 8255 include bit set and reset capability and the ability to source 1mA of current at 1.5 volts. This allows darlington transistors to be directly driven for applications such as printers and high voltage displays.

PIN CONFIGURATION



8255 BLOCK DIAGRAM



PIN NAMES

D_7–D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	0 VOLTS

SILICON GATE MOS 8255

8255 BASIC FUNCTIONAL DESCRIPTION

General

The 8255 is a Programmable Peripheral Interface (PPI) device designed for use in 8080 Microcomputer Systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the 8080 system bus. The functional configuration of the 8255 is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state, bi-directional, eight bit buffer is used to interface the 8255 to the 8080 system data bus. Data is transmitted or received by the buffer upon execution of INput or OUTput instructions by the 8080 CPU. Control Words and Status information are also transferred through the Data Bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the 8080 CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

($\overline{CS}$)

Chip Select: A "low" on this input pin enables the communication between the 8255 and the 8080 CPU.

($\overline{RD}$)

Read: A "low" on this input pin enables the 8255 to send the Data or Status information to the 8080 CPU on the Data Bus. In essence, it allows the 8080 CPU to "read from" the 8255.

($\overline{WR}$)

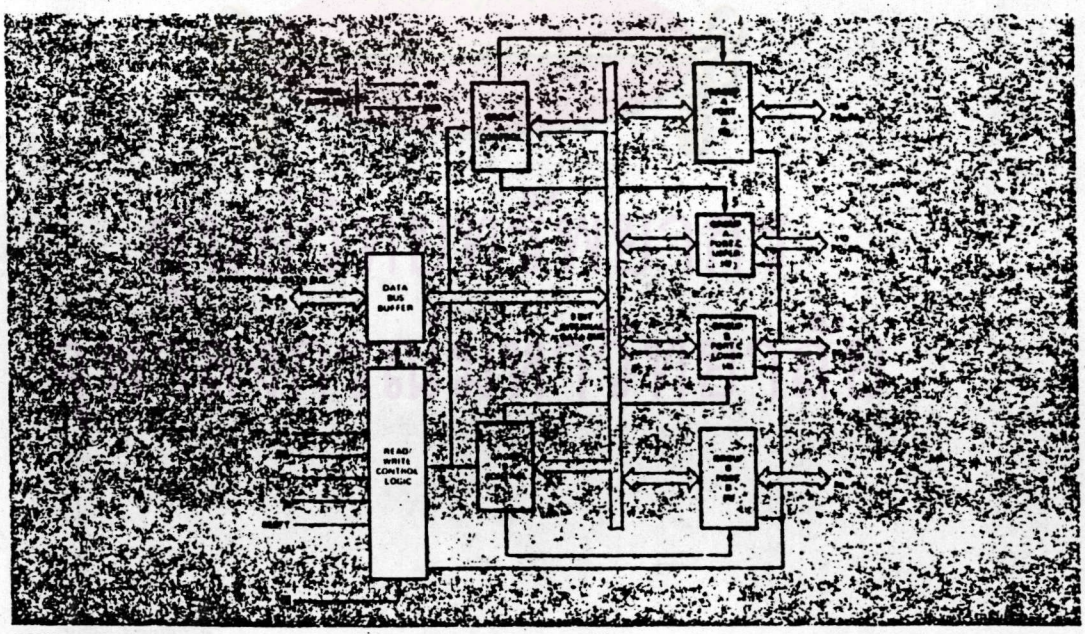
Write: A "low" on this input pin enables the 8080 CPU to write Data or Control words into the 8255.

(A_0 and A_1)

Port Select 0 and Port Select 1: These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the Control Word Register. They are normally connected to the least significant bits of the Address Bus (A_0 and A_1).

8255 BASIC OPERATION

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL
					DISABLE FUNCTION
X	X	X	X	1	DATA BUS → 3-STATE
1	1	0	1	0	ILLEGAL CONDITION



8255 Block Diagram

SILICON GATE MOS 8255

(RESET)

Reset: A "high" on this input clears all internal registers including the Control Register and all ports (A, B, C) are set to the input mode.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the 8080 CPU "outputs" a control word to the 8255. The control word contains information such as "mode", "bit set", "bit reset" etc. that initializes the functional configuration of the 8255.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A – Port A and Port C upper (C7-C4)
Control Group B – Port B and Port C lower (C3-C0)

The Control Word Register can Only be written into. No Read operation of the Control Word Register is allowed.

Ports A, B, and C

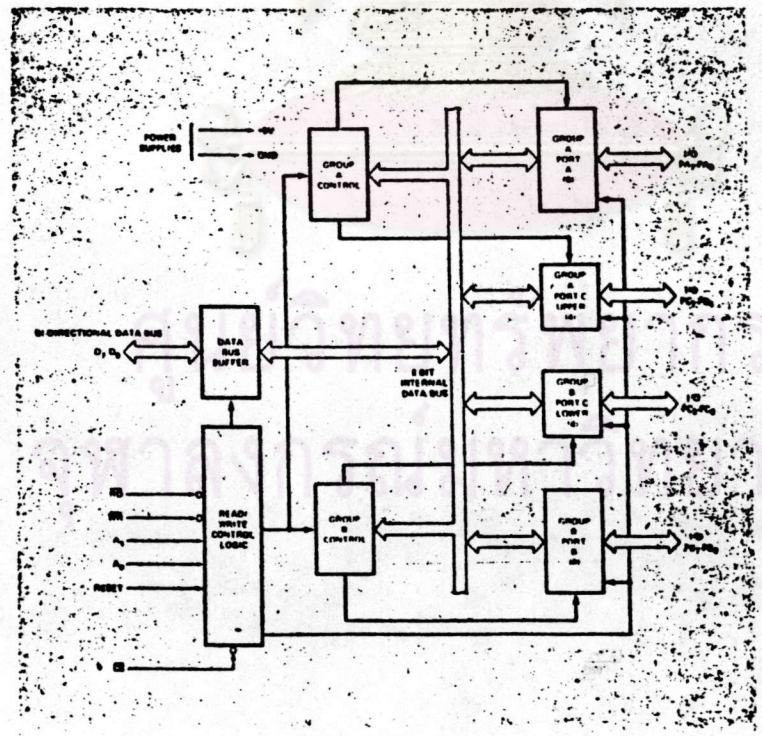
The 8255 contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255.

Port A: One 8-bit data output latch/buffer and one 8-bit data input latch.

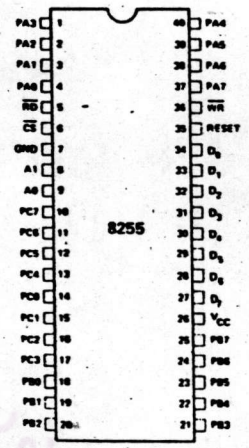
Port B: One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C: One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with Ports A and B.

8255 BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

D_7–D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	0 VOLTS

8255 DETAILED OPERATIONAL DESCRIPTION

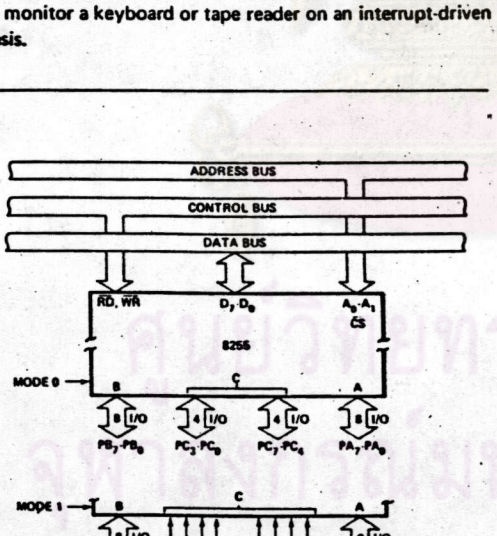
Mode Selection

There are three basic modes of operation that can be selected by the system software:

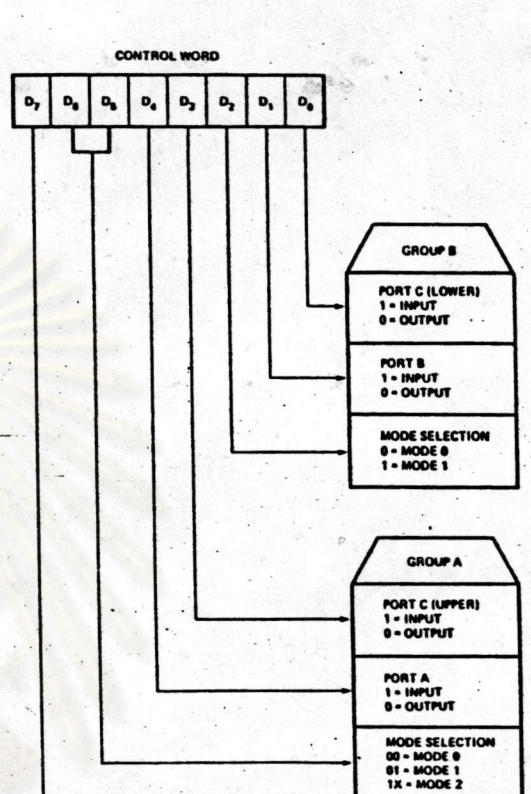
Mode 0 – Basic Input/Output
Mode 1 – Strobed Input/Output
Mode 2 – Bi-Directional Bus

When the RESET input goes "high" all ports will be set to the Input mode (i.e., all 24 lines will be in the high impedance state). After the RESET is removed the 8255 can remain in the Input mode with no additional initialization required. During the execution of the system program any of the other modes may be selected using a single OUTput instruction. This allows a single 8255 to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.



Basic Mode Definitions and Bus Interface

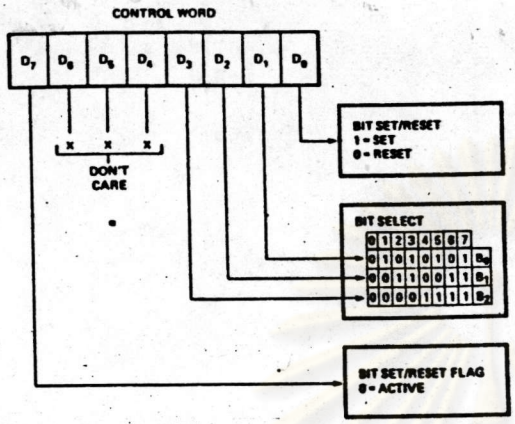


Mode Definition Format

The Mode definitions and possible Mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 8255 has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.



Bit Set/Reset Format

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the 8255 is programmed to operate in Mode 1 or Mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from Port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the Bit set/reset function of Port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without effecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET) — INTE is SET — Interrupt enable
(BIT-RESET) — INTE is RESET — Interrupt disable

Note: All Mask flip-flops are automatically reset during mode selection and device Reset.

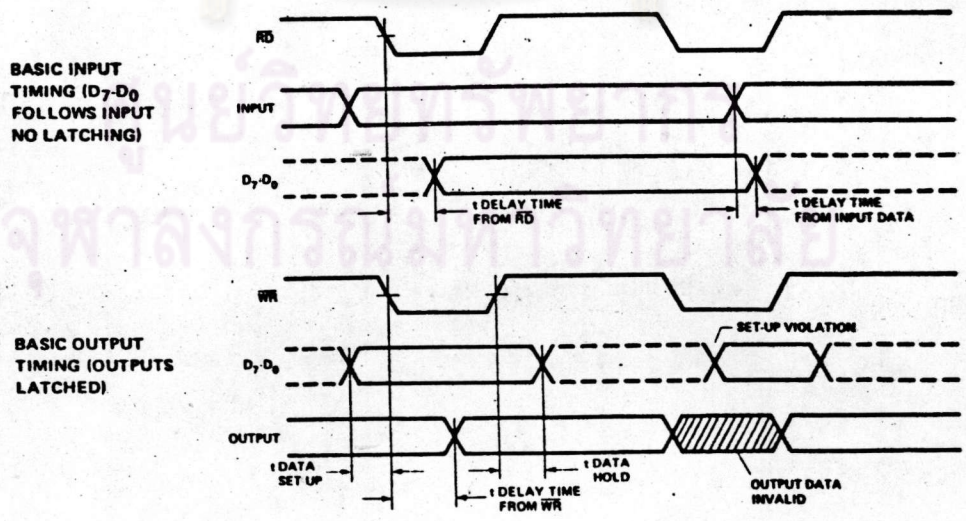
Operating Modes

Mode 0 (Basic Input/Output)

This functional configuration provides simple Input and Output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.



Mode 0 Timing

ภาคผนวก 6
ข้อมูลเกี่ยวกับไอซีเบอร์ 74138

54138/74138 3-Line-to-8-Line Decoder

	Schottky TTL					High-Speed TTL					Low-Power Schottky TTL					Standard TTL					Low-Power TTL				
	Device Type	Package C	P	M	CF	Device Type	Package C	P	M	CF	Device Type	Package C	P	M	CF	Device Type	Package C	P	M	CF	Device Type	Package C	P	M	CF
T.I.	SN54S138	J			W						SN54LS138	J			W									
	SN74S138	J	N								SN74LS138	J	N											
FAIRCHILD	/93S138	DC									93S138/93LS138	DC			FC									
	FC74S138/FC93S138	DC									FC74LS138 FC93LS138	DC	FC		FC									
MOTOROLA											SN74LS138		P											
N.S.C.											DM74LS138		J											
	DM74S138		J								DM54LS138		J											
PHILIPS																								
	N74S138		N								N74LS138		N											
SIGNETICS	S54S138	F	B		W																			
	N74S138	F	B								N74LS138		A											
SIEMENS																								
FUJITSU																								
											74LS138		M											
HITACHI																								
											HD74LS138		P											
MITSUBISHI	M74S138		P								M74LS138		P											
NEC																								
											74LS138		C											
TOSHIBA																								

Electrical Characteristics SN54LS138/SN74LS138

absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC}	7V	Operating free-air temperature range	SN54LS	−55°C to 125°C
Input voltage	7V		SN74LS	0°C to 70°C
		Storage temperature range		−65°C to 150°C

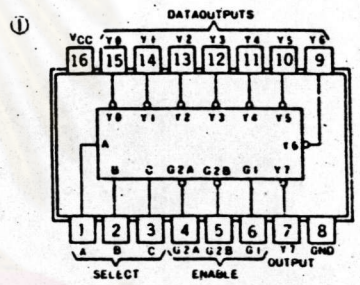
recommended operarating conditions

	SN54LS138			SN74LS138			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			400			400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18mA					1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = 400μA		SN54LS	2.5	3.4		V
				SN74LS	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 8mA				0.35	0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7V					0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V					0.4	mA
I_{OS}	Short-circuit output current *	V_{CC} = MAX			20		100	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs enabled and open				6.3	10	mA
t_{PLH}	from Binary select to Any output	V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 2kΩ	levels of delay	2		13	20	ns
t_{PHL}						27	41	
t_{PLH}				3		18	27	ns
t_{PHL}						26	39	
t_{PLH}	from Enable to Any output			2		12	18	ns
t_{PHL}						21	32	
t_{PLH}				3		17	26	ns
t_{PHL}						25	38	

Pin Assignment (Top View)



Function Table

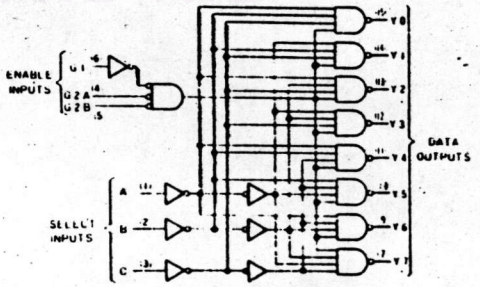
'S138 'LS138

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

* G2 = G2A + G2B

H = high level, L = low level, X = irrelevant

Functional Block Diagram



'S138 'LS138 DECODER DEMULTIPLEXER

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type

‡ All typical values are at V_{CC} = 5V, T_A = 25°C

* Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second

§ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

ภาคผนวก 7

ข้อมูลบางส่วนเกี่ยวกับไมโครโปรเซสเซอร์ Z-80

1. ซีพียู (หน่วยประมวลผลกลาง)

ใช้ซีพียูของ Zilog เบอร์ Z-80A โดยมีระบบสัญญาณนาฬิกาเท่ากับ 3.579 เมกกะเฮิรตซ์

2. รอม (หน่วยความจำอ่านอย่างเดียว)

สามารถใช้ได้ทั้งรอมเบอร์ 2732 และเบอร์ 2764 โดยมีแอดเดรสดังนี้

- กรณีใช้กับรอมเบอร์ 2732 เป็นตัวเฝ้าตรวจ (monitor) (มีขนาด 4 กิโลไบต์) มีแอดเดรสอยู่ที่ 0000 - 0FFFH
- กรณีใช้กับรอมเบอร์ 2764 เป็นตัวเฝ้าตรวจ (monitor) (มีขนาด 8 กิโลไบต์) มีแอดเดรสอยู่ที่ 0000 - 1FFFH

3. แรม (หน่วยความจำเข้าถึงแบบสุ่ม)

ใช้แรมแบบสถิตเบอร์ 6264 มีขนาด 8 กิโลไบต์ โดยมีหน่วยความจำอยู่ที่ 4000 - 5FFFH

4. ส่วนขยายหน่วยความจำ

ส่วนขยายหน่วยความจำ 8 กิโลไบต์นี้ สามารถเป็นได้ทั้งรอมและแรม กรณีที่เป็นรอมจะใช้ได้ทั้งเบอร์ 2732 และเบอร์ 2764

ถ้าใช้ 2732 ซึ่งมีขนาด 4 กิโลไบต์ มีแอดเดรสอยู่ที่ 2000 - 2FFFH
ถ้าใช้ 2764 ซึ่งมีขนาด 8 กิโลไบต์ มีแอดเดรสอยู่ที่ 2000 - 3FFFH

กรณีที่เป็นแรม (ให้ลัดวงจรภายในเข้าด้วยกัน) ใช้ 6264 ซึ่งมีขนาด 8 กิโลไบต์ มีแอดเดรสอยู่ที่ 2000 - 3FFFH

5. อุปกรณ์ติดต่อภายนอก

8255	มีแอดเดรสอยู่ที่	00 - 03H
Z-80 PIO	มีแอดเดรสอยู่ที่	40 - 43H
Z-80 CTC	มีแอดเดรสอยู่ที่	80 - 83H

6. ภาคแสดงผล

ใช้แอลอีดี (ไดโอดปล่อยแสง) แบบ 7 เซ็กเมนต์ ขนาดความสูง 0.5 นิ้ว จำนวน 6 หลัก

7. แป้นพิมพ์ ใช้แบบ 24 แป้นกด

8. แหล่งกำเนิดเสียง ลำโพงของ Sony ขนาด 1 นิ้ว

9. ลักษณะการเชื่อมโยงเครื่องเล่นเทป 83 บิตต่อวินาที

10. อัตราของสัญญาณนาฬิกาในระบบ 3.579 เมกกะเฮิรตซ์

11. ขั้วต่อ

- 40 ขา มาจากซีพียูโดยตรง
- 10 ขา มาจากวงจรถอดรหัสของหน่วยความจำ และ

ด้านออกของ Z-80 CTC

- 28 ขา มาจาก Z-80 PIO และ Z-80 CTC
- ช่องเสียบ 50 ขา โดย 40 ขา มาจากซีพียูโดยตรง,
  5 ขา มาจากวงจรถอดรหัสของหน่วยความจำ และ
  5 ขา มาจากวงจรถอดรหัสของอุปกรณ์ติดต่อภายนอก

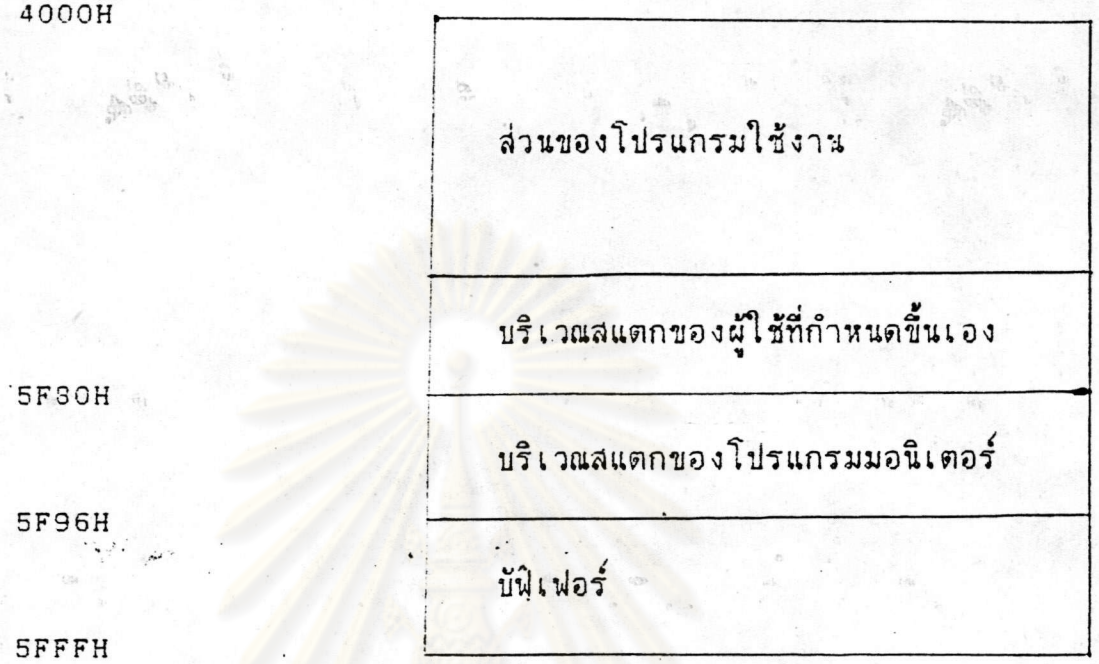
แมปของหน่วยความจำ

แอดเดรสเริ่มต้น	อุปกรณ์ที่ใช้
0000H - 0FFFH	โปรแกรมมอนิเตอร์ 4 กิโลไบต์ (2732)
1000H - 1FFFH	โปรแกรมมอนิเตอร์ส่วนขยาย 8 กิโลไบต์ (2764)
2000H - 3FFFH	ส่วนขยายหน่วยความจำ 8 กิโลไบต์ 2732 มีแอดเดรสอยู่ที่ 2000H - 2FFFH 2764,6264 มีแอดเดรสอยู่ที่ 2000H - 3FFFH
4000H - 5FFFH	หน่วยความจำ 8 กิโลไบต์ (6264)
6000H - FFFFH	สำหรับผู้ใช้ขยายหน่วยความจำ

แมปของด้านเข้าและด้านออก

หมายเลขของทางเข้าออก	ชื่อของทางเข้าออก	อุปกรณ์
00	PORT A	
01	PORT B	8255
02	PORT C	
03	CONTROL	
40	PIO DA	
41	PIO DB	Z-80 PIO
42	PIO CA	
43	PIO CB	
80	CTC 00	
81	CTC 01	Z-80 CTC
82	CTC 02	
83	CTC 03	

หน่วยความจำที่ใช้งานและหน่วยความจำสแตก



Z80®-CPU
Z80A-CPU

Product Specification
MARCH 1978

The Zilog Z80 product line is a complete set of microcomputer components, development systems and support software. The Z80 microcomputer component set includes all of the circuits necessary to build high-performance microcomputer systems with virtually no other logic and a minimum number of low cost standard memory elements.

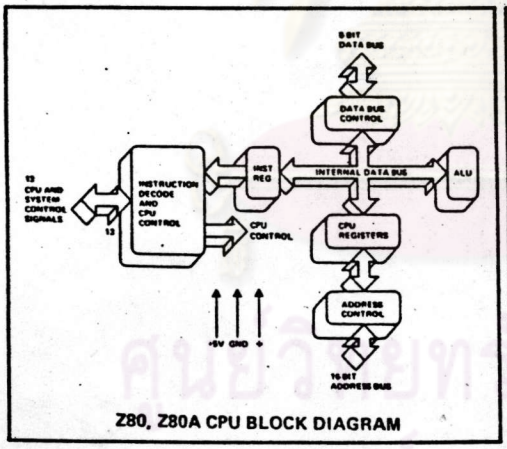
The Z80 and Z80A CPU's are third generation single chip microprocessors with unrivaled computational power. This increased computational power results in higher system through-put and more efficient memory utilization when compared to second generation microprocessors. In addition, the Z80 and Z80A CPU's are very easy to implement into a system because of their single voltage requirement plus all output signals are fully decoded and timed to control standard memory or peripheral circuits. The circuit is implemented using an N-channel, ion implanted, silicon gate MOS process.

Figure 1 is a block diagram of the CPU, Figure 2 details the internal register configuration which contains 208 bits of Read/Write memory that are accessible to the programmer. The registers include two sets of six general purpose registers that may be used individually as 8-bit registers or as 16-bit register pairs. There are also two sets of accumulator and flag registers. The programmer has access to either set of main or alternate registers through a group of exchange instructions. This alternate set allows foreground/background mode of operation or may be reserved for very fast Interrupt response. Each CPU also contains a 16-bit stack pointer which permits simple implementation of multiple level interrupts, unlimited subroutine nesting and simplification of many types of data handling.

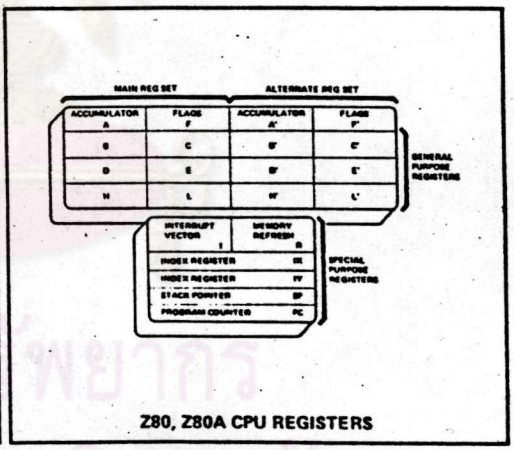
The two 16-bit index registers allow tabular data manipulation and easy implementation of relocatable code. The Refresh register provides for automatic, totally transparent refresh of external dynamic memories. The I register is used in a powerful interrupt response mode to form the upper 8 bits of a pointer to a interrupt service address table, while the interrupting device supplies the lower 8 bits of the pointer. An indirect call is then made to this service address.

FEATURES

- Single chip, N-channel Silicon Gate CPU.
- 158 instructions–includes all 78 of the 8080A instructions with total software compatibility. New instructions include 4-, 8- and 16-bit operations with more useful addressing modes such as indexed, bit and relative.
- 17 internal registers.
- Three modes of fast interrupt response plus a non-maskable interrupt.
- Directly interfaces standard speed static or dynamic memories with virtually no external logic.
- 1.0 μs instruction execution speed.
- Single 5 VDC supply and single-phase 5 volt Clock.
- Out-performs any other single chip microcomputer in 4-, 8-, or 16-bit applications.
- All pins TTL Compatible
- Built-in dynamic RAM refresh circuitry.

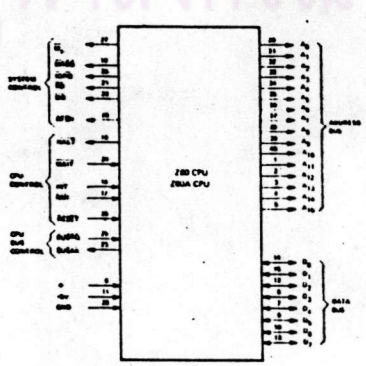


Z80, Z80A CPU BLOCK DIAGRAM



Z80, Z80A CPU REGISTERS

Z80, Z80A-CPU Pin Description



Z80, Z80A CPU PIN CONFIGURATION

A_0-A_{15} (Address Bus)	Tri-state output, active high. A_0-A_{15} constitute a 16-bit address bus. The address bus provides the address for memory (up to 64K bytes) data exchanges and for I/O device data exchanges.
D_0-D_7 (Data Bus)	Tri-state input/output, active high. D_0-D_7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchanges with memory and I/O devices.
$\overline{M_1}$ (Machine Cycle one)	Output, active low. $\overline{M_1}$ indicates that the current machine cycle is the OP code fetch cycle of an instruction execution.
$\overline{MREQ}$ (Memory Request)	Tri-state output, active low. The memory request signal indicates that the address bus holds a valid address for a memory read or memory write operation.

$\overline{IORQ}$ (Input/ Output Request) Tri-state output, active low. The $\overline{IORQ}$ signal indicates that the lower half of the address bus holds a valid I/O address for a I/O read or write operation. An $\overline{IORQ}$ signal is also generated when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus.

$\overline{RD}$ (Memory Read) Tri-state output, active low. $\overline{RD}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

$\overline{WR}$ (Memory Write) Tri-state output, active low. $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.

$\overline{RFSH}$ (Refresh) Output, active low. $\overline{RFSH}$ indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the current $\overline{MREQ}$ signal should be used to do a refresh read to all dynamic memories.

$\overline{HALT}$ (Halt state) Output, active low. $\overline{HALT}$ indicates that the CPU has executed a HALT software instruction and is awaiting either a non-maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOP's to maintain memory refresh activity.

$\overline{WAIT}$ (Wait) Input, active low. $\overline{WAIT}$ indicates to the Z-80 CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active.

$\overline{INT}$ (Interrupt Request) Input, active low. The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled.

$\overline{NMI}$ (Non Maskable Interrupt) Input, active low. The non-maskable interrupt request line has a higher priority than $\overline{INT}$ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. $\overline{NMI}$ automatically forces the Z-80 CPU to restart to location 0066_H.

$\overline{RESET}$ Input, active low. $\overline{RESET}$ initializes the CPU as follows: reset interrupt enable flip-flop, clear PC and registers I and R and set interrupt to 8080A mode. During reset time, the address and data bus go to a high impedance state and all control output signals go to the inactive state.

$\overline{BUSRQ}$ (Bus Request) Input, active low. The bus request signal has a higher priority than $\overline{NMI}$ and is always recognized at the end of the current machine cycle and is used to request the CPU address bus, data bus and tri-state output control signals to go to a high impedance state so that other devices can control these busses.

$\overline{BUSAK}$ (Bus Acknowledge) Output, active low. Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus and tri-state control bus signals have been set to their high impedance state and the external device can now control these signals.

Absolute Maximum Ratings

Temperature Under Bias	Specified operating range.
Storage Temperature	-65°C to +150°C
Voltage On Any Pin with Respect to Ground	-0.3V to +7V
Power Dissipation	1.5W

*Comment

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: For Z80-CPU all AC and DC characteristics remain the same for the military grade parts except I_{CC}

I_{CC} = 200 mA

Z80-CPU D.C. Characteristics

T_A = 0°C to 70°C, V_{CC} = 5V ± 5% unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3		0.45	V	
V_{IHC}	Clock Input High Voltage	V_{CC} -.6		V_{CC}+.3	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL}=1.8mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -250μA
I_{CC}	Power Supply Current			150	mA	
I_{LI}	Input Leakage Current			10	μA	V_{IN}=0 to V_{CC}
I_{LOH}	Tri-State Output Leakage Current in Float			10	μA	V_{OUT}=2.4 to V_{CC}
I_{LOL}	Tri-State Output Leakage Current in Float			-10	μA	V_{OUT}=0.4V
I_{LD}	Data Bus Leakage Current in Input Mode			±10	μA	$0 \leq V_{IN} \leq V_{CC}$

Capacitance

T_A = 25°C, f = 1 MHz,
unmeasured pins returned to ground

Symbol	Parameter	Max.	Unit
C_ϕ	Clock Capacitance	35	pF
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	10	pF

Z80-CPU Ordering Information

C – Ceramic
P – Plastic
S – Standard 5V ±5% 0° to 70°C
E – Extended 5V ±5% -40° to 85°C
M – Military 5V ±10% -55° to 125°C

A.C. Characteristics Z80-CPU

T_A = 0°C to 70°C, Vcc = +5V ± 5%, Unless Otherwise Noted.

Signal	Symbol	Parameter	Min	Max	Unit	Test Condition
Φ	t_c	Clock Period	4	1121	μsec	
	$t_{w(\Phi H)}$	Clock Pulse Width, Clock High	180	[E]	nsec	
	$t_{w(\Phi L)}$	Clock Pulse Width, Clock Low	180	2000	nsec	
	t_r, t_f	Clock Rise and Fall Time		30	nsec	
A_{0-15}	$t_{D(AD)}$	Address Output Delay		145	nsec	C_L = 50pF
	$t_{F(AD)}$	Delay to Float		110	nsec	
	t_{acm}	Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)	[1]		nsec	
	t_{aci}	Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)	[2]		nsec	
	t_{ca}	Address Stable from $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$ or $\overline{MREQ}$	[3]		nsec	
	t_{caf}	Address Stable from $\overline{RD}$ or $\overline{WR}$ During Float	[4]		nsec	
D_{0-7}	$t_{D(D)}$	Data Output Delay		230	nsec	C_L = 50pF
	$t_{F(D)}$	Delay to Float During Write Cycle		90	nsec	
	$t_{S\Phi(D)}$	Data Setup Time to Rising Edge of Clock During M1 Cycle	50		nsec	
	$t_{S\overline{\Phi}(D)}$	Data Setup Time to Falling Edge of Clock During M2 to M5	60		nsec	
	t_{dcm}	Data Stable Prior to $\overline{WR}$ (Memory Cycle)	[5]		nsec	
	t_{dci}	Data Stable Prior to $\overline{WR}$ (I/O Cycle)	[6]		nsec	
	t_{cdf}	Data Stable From $\overline{WR}$	[7]			
	t_H	Any Hold Time for Setup Time	0		nsec	
$\overline{MREQ}$	$t_{DL\overline{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ Low		100	nsec	C_L = 50pF
	$t_{DH\Phi(MR)}$	$\overline{MREQ}$ Delay From Rising Edge of Clock, $\overline{MREQ}$ High		100	nsec	
	$t_{DH\overline{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ High		100	nsec	
	$t_{w(\overline{MRL})}$	Pulse Width, $\overline{MREQ}$ Low	[8]		nsec	
	$t_{w(\overline{MRH})}$	Pulse Width, $\overline{MREQ}$ High	[9]		nsec	
$\overline{IORQ}$	$t_{DL\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ Low		90	nsec	C_L = 50pF
	$t_{DL\overline{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ Low		110	nsec	
	$t_{DH\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ High		100	nsec	
	$t_{DH\overline{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ High		110	nsec	
$\overline{RD}$	$t_{DL\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ Low		100	nsec	C_L = 50pF
	$t_{DL\overline{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ Low		130	nsec	
	$t_{DH\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ High		100	nsec	
	$t_{DH\overline{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ High		110	nsec	
$\overline{WR}$	$t_{DL\Phi(WR)}$	$\overline{WR}$ Delay From Rising Edge of Clock, $\overline{WR}$ Low		80	nsec	C_L = 50pF
	$t_{DL\overline{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ Low		90	nsec	
	$t_{DH\overline{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ High		100	nsec	
	$t_{w(\overline{WRL})}$	Pulse Width, $\overline{WR}$ Low	[10]		nsec	
$\overline{M1}$	$t_{DL(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ Low		130	nsec	C_L = 50pF
	$t_{DH(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ High		130	nsec	
$\overline{RFSH}$	$t_{DL(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ Low		180	nsec	C_L = 50pF
	$t_{DH(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ High		150	nsec	
$\overline{WAIT}$	$t_{s(WT)}$	$\overline{WAIT}$ Setup Time to Falling Edge of Clock	70		nsec	
$\overline{HALT}$	$t_{D(HT)}$	$\overline{HALT}$ Delay Time From Falling Edge of Clock		300	nsec	C_L = 50pF
$\overline{INT}$	$t_{s(IT)}$	$\overline{INT}$ Setup Time to Rising Edge of Clock	80		nsec	
$\overline{NMI}$	$t_{w(\overline{NML})}$	Pulse Width, $\overline{NMI}$ Low	80		nsec	
$\overline{BUSRQ}$	$t_{s(BQ)}$	$\overline{BUSRQ}$ Setup Time to Rising Edge of Clock	80		nsec	
$\overline{BUSAK}$	$t_{DL(BA)}$	$\overline{BUSAK}$ Delay From Rising Edge of Clock, $\overline{BUSAK}$ Low		120	nsec	C_L = 50pF
	$t_{DH(BA)}$	$\overline{BUSAK}$ Delay From Falling Edge of Clock, $\overline{BUSAK}$ High		110	nsec	
$\overline{RESET}$	$t_{s(RS)}$	$\overline{RESET}$ Setup Time to Rising Edge of Clock	90		nsec	
	$t_{F(C)}$	Delay to Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)		100	nsec	
	t_{ms}	$\overline{M1}$ Stable Prior to $\overline{IORQ}$ (Interrupt Ack.)	[11]		nsec	

[12] $t_c = t_{w(\Phi H)} + t_{w(\Phi L)} + t_r + t_f$

[1] $t_{acm} = t_{w(\Phi H)} + t_f - 75$

[2] $t_{aci} = t_c - 80$

[3] $t_{ca} = t_{w(\Phi L)} + t_f - 40$

[4] $t_{caf} = t_{w(\Phi L)} + t_f - 60$

[5] $t_{dcm} = t_c - 210$

[6] $t_{dci} = t_{w(\Phi L)} + t_f - 210$

[7] $t_{cdf} = t_{w(\Phi L)} + t_f - 80$

[8] $t_{w(MRL)} = t_c - 40$

[9] $t_{w(MRH)} = t_{w(\Phi H)} + t_f - 30$

[10] $t_{w(\overline{WRL})} = t_c - 40$

[11] $t_{ms} = t_c + t_{w(\Phi H)} + t_f$ nsec

NOTES

A Data should be enabled onto the CPU data bus when $\overline{RD}$ is active. During interrupt acknowledge data should be enabled when $\overline{M1}$ and $\overline{IORQ}$ are both active.

B All control signals are internally synchronized, so they may be totally asynchronous with respect to the clock.

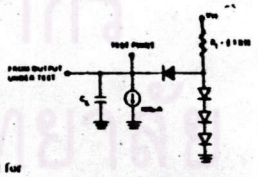
C The $\overline{RESET}$ signal must be active for a minimum of 3 clock cycles.

D Output Delay vs. Loaded Capacitance

TA = 70°C, Vcc = +5V ±5%

Add 10nsec delay for each 50pf increase in load up to a maximum of 200pf for the data bus & 100pf for address & control lines

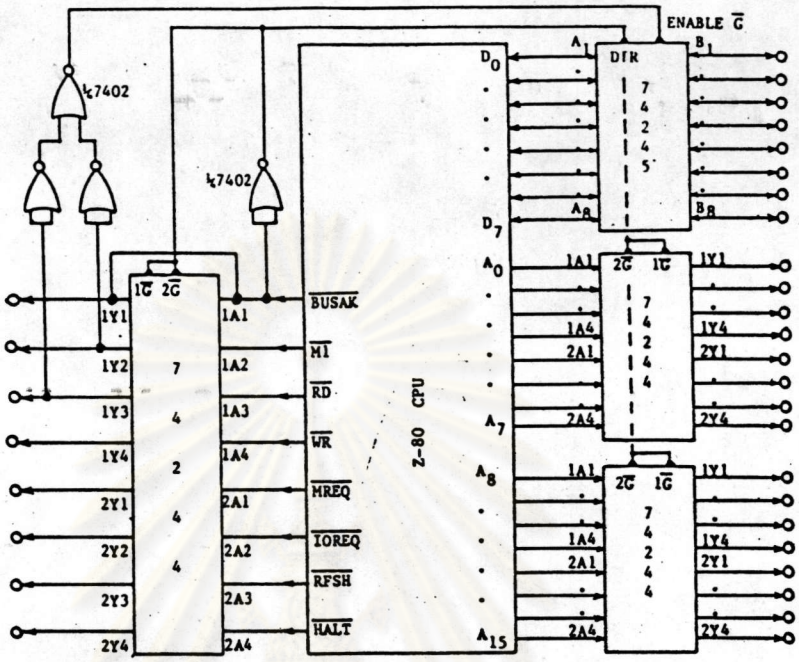
E Although static by design, testing guarantees $t_{w(\Phi H)}$ of 200 μsec maximum.



Load circuit for Output

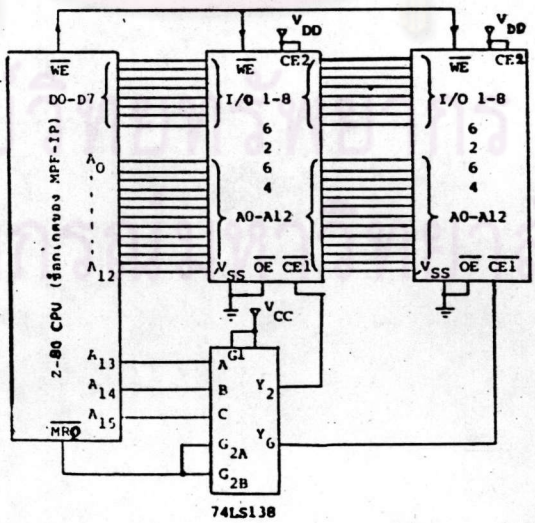
การต่อวงจรขับบัสและหน่วยความจำเพิ่มเติมให้แก่ไมโครโปรเซสเซอร์ Z-80

รูปที่ ผ7-1 แสดงการต่อวงจรขับ(driver) ให้แก่บัสต่าง ๆ ของไมโครโปรเซสเซอร์ Z-80 องค์ประกอบที่สำคัญในวงจรนี้ ก็คือไอซีเบอร์ 74244 กับ 74245 ซึ่งเป็นตัวขับสาย(line driver) และไอซีเบอร์ 7402 ซึ่งเป็นเกตแบบนอร์(NOR gate)



*รูปที่ ผ7-1 วงจรขับบัสที่ต่อเพิ่มให้แก่*ไมโครโปรเซสเซอร์ Z-80

รูปที่ ผ7-2 แสดงการต่อหน่วยความจำเพิ่มเติมให้แก่ ไมโครโปรเซสเซอร์ Z-80 ไอซีหน่วยความจำที่ใช้ก็คือแรม(RAM)เบอร์ 6264 จำนวน 2 ตัว แต่ละตัวมีขนาดความจุ 8 กิโลไบต์ องค์ประกอบที่ใช้ควบคุมการเลือกไอซีเบอร์ 6264 แต่ละตัว ก็คือไอซีเบอร์ 74LS138 ซึ่งทำหน้าที่เหมือนกับไอซีเบอร์ 74138 ในภาคผนวก 6 นั่นเอง



*รูปที่ ผ7-2 วงจรหน่วยความจำเพิ่มเติมสำหรับ*ไมโครโปรเซสเซอร์ Z-80

54244/74244 Octal Buffers/Line Drivers/Line Receivers

	Schttky TTL					High-Speed TTL					Low-Power Schottky TTL					Standard TTL					Low-Power TTL				
	Device Type	Package				Device Type	Package				Device Type	Package				Device Type	Package				Device Type	Package			
		C	P	M	CF		C	P	M	CF		C	P	M	CF		C	P	M	CF		C	P	M	CF
T. I.											SN54LS244		J												
											SN74LS244		J	N											
FAIRCHILD																									
MOTOROLA																									
N. S. C.																									
PHILIPS																									
SIGNETICS																									
SIEMENS																									
FUJITSU																									
HITACHI																									
MITSUBISHI																									
NEC																									
TOSHIBA																									

Electrical Characteristics SN54LS244/SN74LS244

absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC}	7V	Operating free-air temperature range	SN54LS	55°C to 125°C
Input voltage	5.5V		SN74LS	0°C to 70°C
Interemitter voltage	5.5V	Storage temperature range		65°C to 150°C

recommended operating conditions

	SN54LS244			SN74LS244			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			12			15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

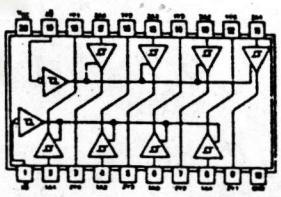
PARAMETER			TEST CONDITIONS †		SN74LS MIN	SN74LS TYP‡	SN74LS MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18mA				−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = MIN		0.2	0.4		V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2V, V_{IL} = $V_{IL\,max}$, I_{OH} = −3mA		2.4	3.4		V
			V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.5V, I_{OH} = MAX		2			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2V, V_{IL} = $V_{IL\,max}$	I_{OL} = 12mA			0.4	V
				I_{OL} = 24mA			0.5	
I_{OZH}	Off-state output current, high-level voltage applied		V_{CC} = MAX, V_{IH} = 2V, V_{IL} = $V_{IL\,max}$	V_O = 2.7V			20	μA
I_{OZL}	Off-state output current, low-level voltage applied			V_O = 0.4V			−20	
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7V				0.1	mA
I_{IH}	High-level input current, any input		V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_{IL} = 0.4V				0.2	mA
I_{OS}	Short-circuit output current ⊕		V_{CC} = MAX		−40		−225	mA
I_{CC}	Supply current	Outputs high	V_{CC} = MAX, Outputs open	All		13	23	mA
		Outputs low		'LS244		27	46	
		All outputs disabled		'LS244		32	54	

switching characteristics, V_{CC} 5V, T_A 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output			9	14	ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 45pF, R_L = 667Ω, See Note 2		12	18	ns
t_{PZL}	Output enable time to low level			20	30	ns
t_{PZH}	Output enable time to high level			15	23	ns
t_{PLZ}	Output disable time from low level	C_L = 5pF, R_L = 667Ω, See Note 2		15	25	ns
t_{PHZ}	Output disable time from high level			10	18	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5V, T_A = 25°C.
⊕ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: Load circuit and voltage waveforms are shown on page 3-11.

Pin Assignment (Top View)



SN54LS244 (J) SN74LS244 (J, N)

54245/74245 Octal Bus Transceivers with 3-state Outputs

	Schottky TTL					High-Speed TTL					Low-Power Schottky TTL					Standard TTL					Low-Power TTL				
	Device Type	Package				Device Type	Package				Device Type	Package				Device Type	Package				Device Type	Package			
		C	P	M	CF		C	P	M	CF		C	P	M	CF		C	P	M	CF		C	P	M	CF
T. I.											SN54LS245	J		W	W										
											SN74LS245	J	N												
FAIRCHILD																								
MOTOROLA																								
N. S. C																								
PHILIPS																								
SIGNETICS																								
SIEMENS																								
FUJITSU																								
HITACHI																								
MITSUBISHI																								
NEC																								
TOSHIBA																								

Electrical Characteristics SN54LS245/SN74LS245

absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC}	7 V	Operating free-air temperature range	SN54LS	−55°C to 125°C
Input voltage	7 V		SN74LS	0°C to 70°C
		Storage temperature range		−65°C to 150°C

recommended operating conditions

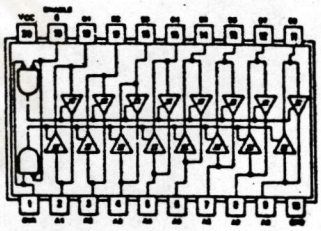
	SN54LS245			SN74LS245			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−12			−15	mA
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS†		SN74LS245 MIN	SN74LS245 TYP‡	SN74LS245 MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$) A or B input	V_{CC} = MIN			0.2	0.4	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, $V_{IL} = V_{IL\,max}$	I_{OH} = −3 mA	2.4	3.4		V
			I_{OH} = MAX	2			
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, $V_{IL} = V_{IL\,max}$	I_{OL} = 12 mA			0.4	V
			I_{OL} = 24 mA			0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, G at 2 V	V_O = 2.7 V			10	μA
I_{OZL}	Off-state output current, low-level voltage applied		V_O = 0.4 V			−200	
I_I	Input current at maximum input voltage — A or B	V_{CC} = MAX,	V_I = 5.5 V			0.1	mA
	DIR or $\overline{G}$		V_I = 7 V			0.1	
I_{IH}	High-level input current	V_{CC} = MAX, V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_{IL} = 0.4 V				−0.2	mA
I_{OS}	Short-circuit output current	V_{CC} = MAX		−40		−225	mA
I_{CC}	Supply current — Total, outputs high	V_{CC} = MAX, Outputs open			48	70	mA
	Total, outputs low				67	90	
	Outputs at Hi-Z				64	95	

switching characteristics, V_{CC} = 5 V, T_A = 25°C

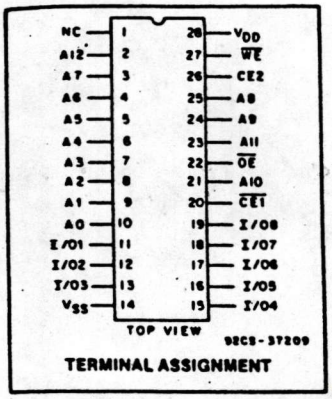
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 45 pF, R_L = 667 Ω, See Note 2		8	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output			8	12	ns
t_{PZL}	Output enable time to low level			27	40	ns
t_{PZL}	Output enable time to high level			25	40	ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF, R_L = 667 Ω, See Note 2		15	25	ns
t_{PHZ}	Output disable time from high level			15	25	ns



SN54LS245 (J) SN74LS245 (J, N)

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
*Not more than one output should be shorted at a time, and duration of the short-circuit should not not exceed one second

CDM6264



TERMINAL ASSIGNMENT

CMOS 8192-Word by 8-Bit LSI Static RAM

Features:

- *Fully static operation*
- *Single power supply: 4.5 V to 5.5 V*
- *All inputs and outputs directly TTL compatible*
- *3-state outputs*
- *Industry standard 28-pin configuration*
- *Input address buffers gated off with chip disable*
- *Fast access time: t_{AA}=150 ns/120 ns (CDM6264-3/CDM6264-4)*
- *Low standby and operating power: I_{DDS1}=2 μA typical, I_{OPER2}=40 mA maximum*
- *Data retention voltage: 2 V min.*
- *Operating temperature range (max. rating): 0° to 70°C*

The RCA-CDM6264 is a 8192-word by 8-bit static random-access memory. It is designed for use in memory systems where high-speed, low power and simplicity in use are desirable. This device has common data input and data output and utilizes a single power supply of 4.5 V to 5.5 V.

Either chip enable ($\overline{CE1}$ or CE2), when not valid, will gate off the address and output buffers and power down the chip to minimum standby power with inputs toggling. The output enable ($\overline{OE}$) controls the output buffers to eliminate bus contention.

The CDM6264 is supplied in 28-lead, hermetic, dual-in-line side-brazed ceramic (D suffix) and in 28-lead dual-in-line plastic (E suffix) packages.

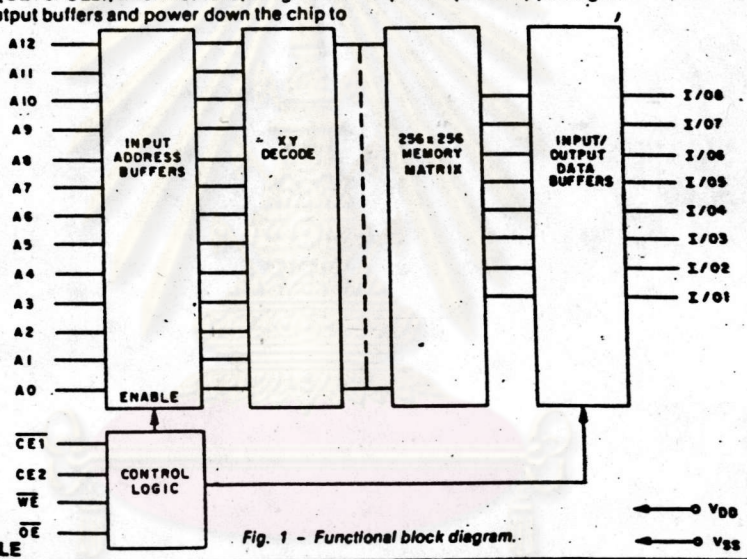


Fig. 1 – Functional block diagram.

TRUTH TABLE

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	A0 TO A12	MODE	DATA I/O	DEVICE CURRENT
H	X	X	X	X	NOT SELECTED	HIGH Z	STANDBY
X	L	X	X	X	NOT SELECTED	HIGH Z	STANDBY
L	H	L	H	STABLE	READ	DATA OUT	ACTIVE
L	H	X	L	STABLE	WRITE	DATA IN	ACTIVE
L	H	H	H	STABLE	OUTPUT DISABLE	HIGH Z	ACTIVE

L = LOW H = HIGH X = H OR L

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}):
(Voltage referenced to V_{SS} terminal) ..... -0.3 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.3 to +7 V
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = 0° to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60° to +70°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 420 mW
For T_A = 0° to +70°C (PACKAGE TYPE D) ..... 500 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D ..... 0 to +70°C
PACKAGE TYPE E ..... 0 to +70°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -55 to +125°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

OPERATING CONDITIONS at T_A = 0 to +70° C

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		LIMITS ALL TYPES MIN.	LIMITS ALL TYPES MAX.	UNITS
DC Operating Voltage Range		4.5	5.5	V
Input Voltage Range	V_{IH}	2.2	V_{DD} + 0.3	
	V_{IL}	-0.3	0.8	
Input Signal Rise or Fall Time[Δ]	t_r, t_f	—	5	μs

[Δ] Input signal rise and fall times with a duration greater than the maximum value can cause loss of stored data in the selected mode.

STATIC ELECTRICAL CHARACTERISTICS at T_A = 0 to +70°C, V_{DD} = 5 V ± 10%, Except as noted

CHARACTERISTIC		CONDITIONS		LIMITS ALL TYPES Min.	Typ.[*]	Max.	UNITS
Standby Device Current	I_{DDS}	$\overline{CE1}$=V_{IH} or CE2=V_{IL}		—	1.5	3	mA
	I_{DDS1}	$\overline{CE1}$=CE2 ≥ V_{DD}-0.2 V or CE2 ≤ 0.2 V		—	2	100	μA
Output Voltage Low Level	V_{OL} Max.	I_{OL}=2.1 mA		—	—	0.4	V
		I_{OL}=1 μA		—	0.1	—	
Output Voltage High Level	V_{OH} Min.	I_{OH}=-1 mA		2.4	—	—	V
		I_{OH}=-1 μA		—	V_{DD}-0.1	—	
Input Leakage Current	I_{IN} Max.	V_{IN}=0 V to V_{DD}		—	±0.1	±2	μA
3-State Output Leakage Current	I_{OUT}	$V_{I/O}$=0 V to V_{DD}		—	±0.5	±2	
Operating Device Current	I_{OPER1}[*]	V_{IN}=V_{IL}, V_{IH}	t_{cyc}=1 μs	—	4.5	9	mA
			t_{cyc}=120 ns	—	22.5	45	
	I_{OPER2}[#]	V_{IN}=0.2 V, V_{DD}-0.2 V	t_{cyc}=1 μs	—	2	4	
			t_{cyc}=120 ns	—	20	40	
Input Capacitance	C_{IN}	V_{IN}=0 V, f=1 MHz, T_A=25°C		—	4	6	pF
Output Capacitance	$C_{I/O}$	$V_{I/O}$=0 V, f=1 MHz, T_A=25°C		—	6	8	

[*] Typical values are for T_A=25°C and nominal V_{DD}.

[#] Outputs open circuited.

ประวัติผู้เขียน

อรุณ บูรณะนิตย์ สำเร็จการศึกษาระดับปริญญาตรี จากคณะวิศวกรรมศาสตร์ จุฬาลงกรณ์มหาวิทยาลัยใน สาขาวิศวกรรมไฟฟ้า เมื่อปีพ.ศ. 2527 ขณะศึกษาเคยเป็นตัวแทนมหาวิทยาลัยไปแข่งขันกีฬามหาวิทยาลัย ในปี พ.ศ. 2528 เคยได้รับรางวัลชมเชยจากการประกวดสิ่งประดิษฐ์ จัดโดยฝ่ายวิจัย จุฬาลงกรณ์มหาวิทยาลัย เรื่อง "เครื่องพล็อตสนามไฟฟ้า" ในปี พ.ศ. 2529 ปัจจุบันเป็นวิศวกรอิสระ