รายการอ้างอิง

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ภาคผนวก

HARRIS

IRFP460
IRFP462

N-Channel Power MOSFETs Avalanche-Energy Rated

August 1991

Features

- 20A and 17A, 500V
- $r_{DS}(on)$ = 0.27Ω and 0.35Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

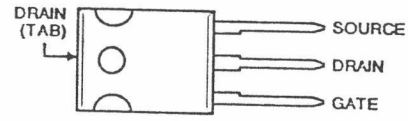
Description

The IRFP460 and IRFP462 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFP-types are supplied in the JEDEC TO-247 plastic package.

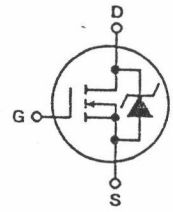
Package

TO-247
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		IRFP460	IRFP462	UNITS
Continuous Drain Current				
T_C = +25°C	I_D	20	17	A
T_C = +100°C	I_D	12	11	A
Pulsed Drain Current (1)	I_{DM}	80	68	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C	P_D	250	250	W
Linear Derating Factor		2.0	2.0	W/°C
Single Pulse Avalanche Energy Rating (2) See Figure 14	E_{AS}	960	960	mJ
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300	300	°C

NOTES:

1. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 5).
2. V_{DD} = 50V, starting T_J = +25°C, L = 4.3mH, R_{GS} = 25Ω, Peak I_L = 20A. See Fig. 14.
3. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number 2291.1

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_J) = 25°C Unless Otherwise Specified*

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	ALL	500	–	–	V	V_{GS} = 0V, I_D = 250 μA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance ③	IRFP460	–	0.24	0.27	Ω	V_{GS} = 10V, I_D = 11A
		IRFP462	–	0.27	0.35		
$I_{D(on)}$	On-State Drain Current ③	IRFP460	20	–	–	A	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ Max., V_{GS} = 10V
		IRFP462	17				
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0	–	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
g_{fs}	Forward Transconductance ③	ALL	13	19	–	S (℧)	V_{DS} ≥ 50V, I_{DS} = 11A
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	1000		V_{DS} = 0.8 x Max. Rating, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	ALL	–	–	500	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	ALL	–	–	-500	nA	V_{GS} = -20V
Q_g	Total Gate Charge	ALL	–	120	190	nC	V_{GS} = 10V, I_D = 21A, V_{DS} = 0.8 x Max. Rating, See Fig. 16 (Independent of operating temperature)
Q_{gs}	Gate-to-Source Charge	ALL	–	18	—	nC	
Q_{gd}	Gate-to-Drain ("Miller") Charge	ALL	–	62	—	nC	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	23	35	ns	V_{DD} = 250V, I_D = 21A, R_G = 4.3Ω, R_D = 12Ω, See Fig. 15 (Independent of operating temperature)
t_r	Rise Time	ALL	–	81	120	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	85	130	ns	
t_f	Fall Time	ALL	–	65	98	ns	
L_D	Internal Drain Inductance	ALL	–	5.0	–	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die. Modified MOSFET symbol showing the internal inductances
L_S	Internal Source Inductance	ALL	–	13	–	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad
C_{iss}	Input Capacitance	ALL	–	4100	–	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1.0 MHz, See Fig. 10
C_{oss}	Output Capacitance	ALL	–	480	–	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	84	–	pF	
R_{thJC}	Junction-to-Case	ALL	–	–	0.50	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.10	–	°C/W	Mounting surface flat, smooth, and greased
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free air operation
	Mounting Torque	ALL	–	–	10	in. • lbs	Standard 6-32 screw

① Repetitive Rating; Pulse width limited by maximum junction temperature (see figure 5) Refer to current HEXFET reliability report

② @ V_{DD} = 50V, Starting T_J = 25°C, L = 4.3 mH, R_G = 25Ω, Peak I_L = 20A. See Fig. 14.

③ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	ALL	—	—	20	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier
I_{SM}	Pulsed Source Current (Body Diode) ①	ALL	–	–	80	A	
V_{SD}	Diode Forward Voltage ③	ALL	–	–	1.8	V	T_J = 25°C, I_S = 21A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	280	580	1200	ns	T_J = 25°C, I_F = 21A, di/dt = 100 A/μs
Q_{RR}	Reverse Recovery Charge	ALL	3.8	8.1	18	μC	
t_{on}	Forward Turn-On Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D				

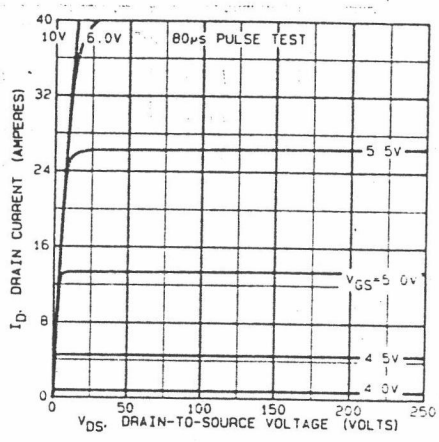


Fig. 1 - Typical output characteristics.

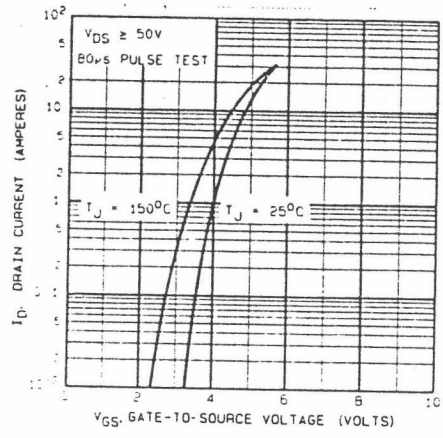


Fig. 2 - Typical transfer characteristics.

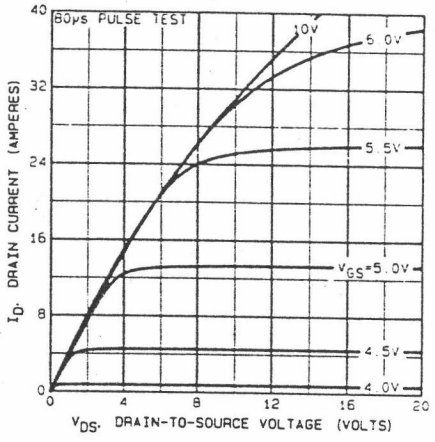


Fig. 3 - Typical saturation characteristics.

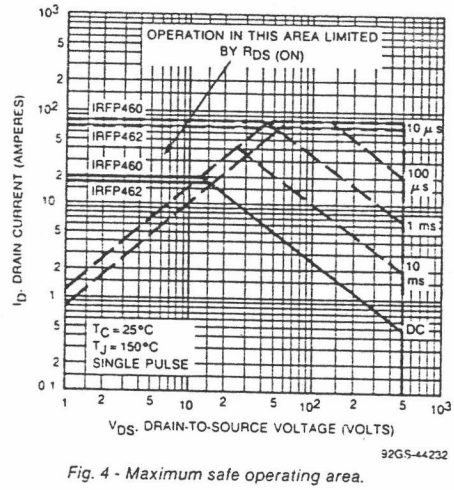


Fig. 4 - Maximum safe operating area.

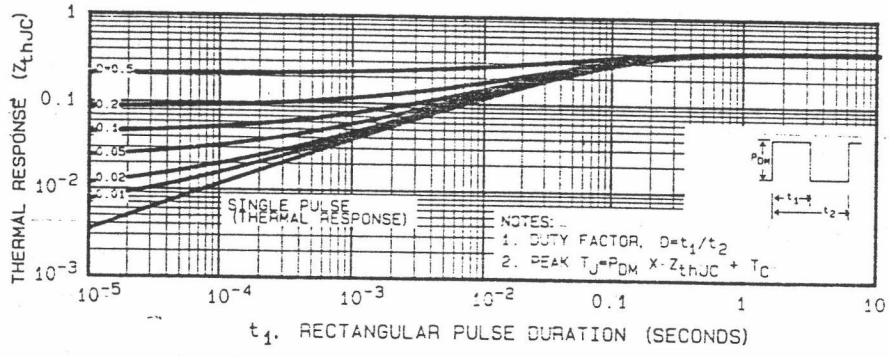


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

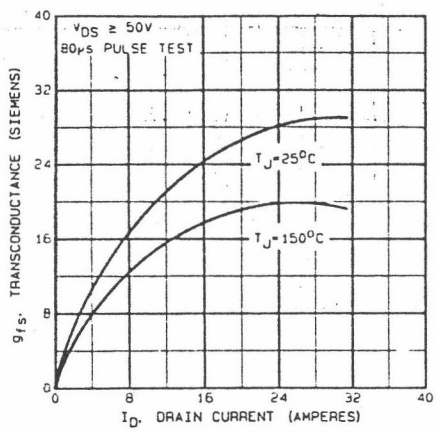


Fig. 6 - Typical transconductance vs. drain current.

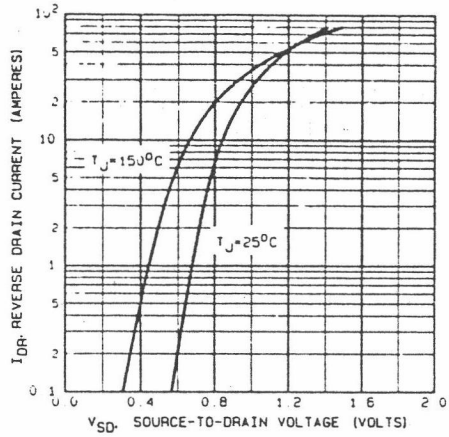


Fig. 7 - Typical source-drain diode forward voltage.

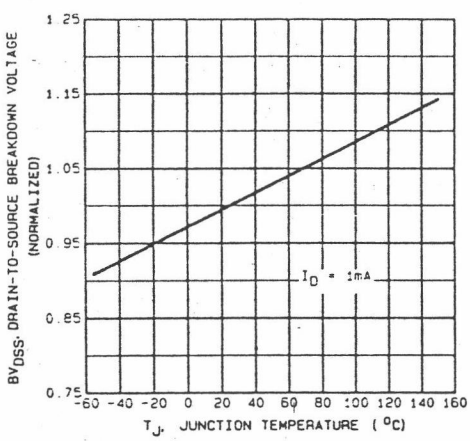


Fig. 8 - Breakdown voltage vs. temperature.

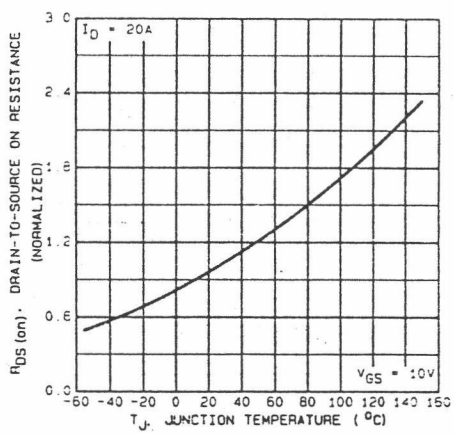


Fig. 9 - Normalized on-resistance vs. temperature.

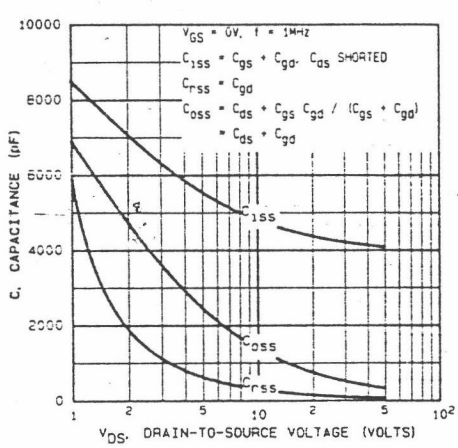


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

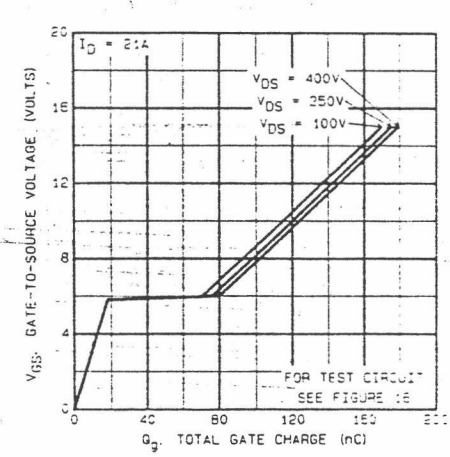


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

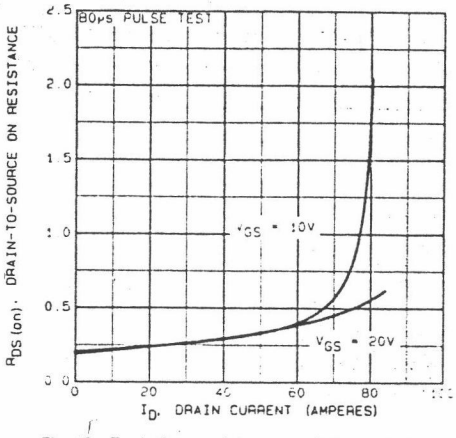


Fig. 12 - Typical on-resistance vs. drain current.

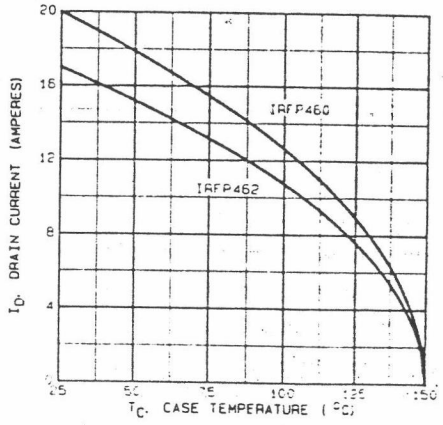


Fig. 13 - Maximum drain current vs. case temperature.

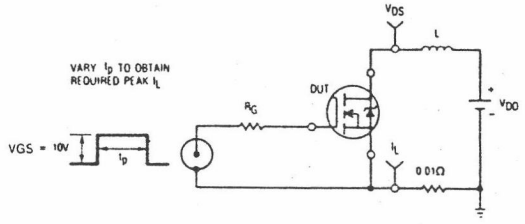


Fig. 14a - Unclamped inductive test circuit.

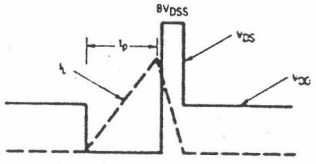


Fig. 14b - Unclamped inductive waveforms.

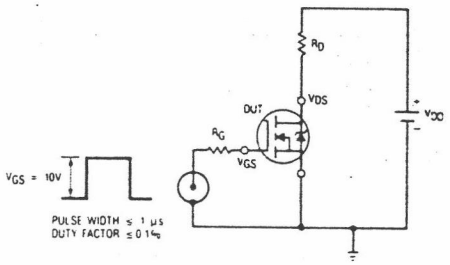


Fig. 15a - Switching time test circuit.

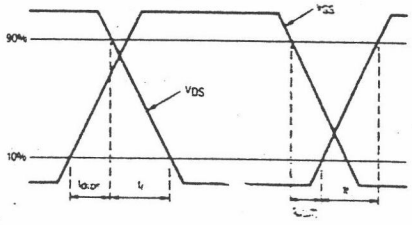


Fig. 15b - Switching time waveforms.

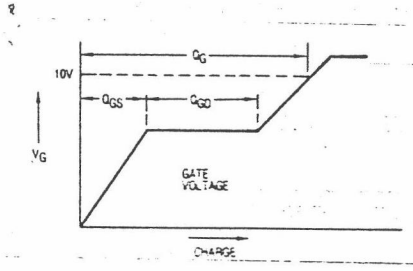


Fig. 16a - Basic gate charge waveform.

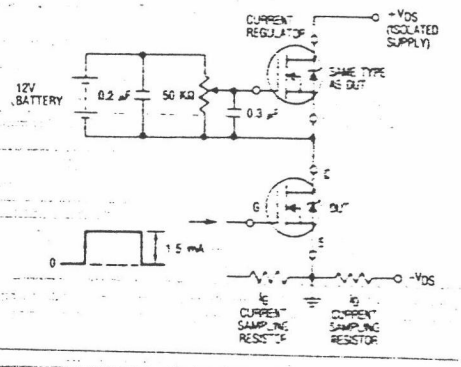
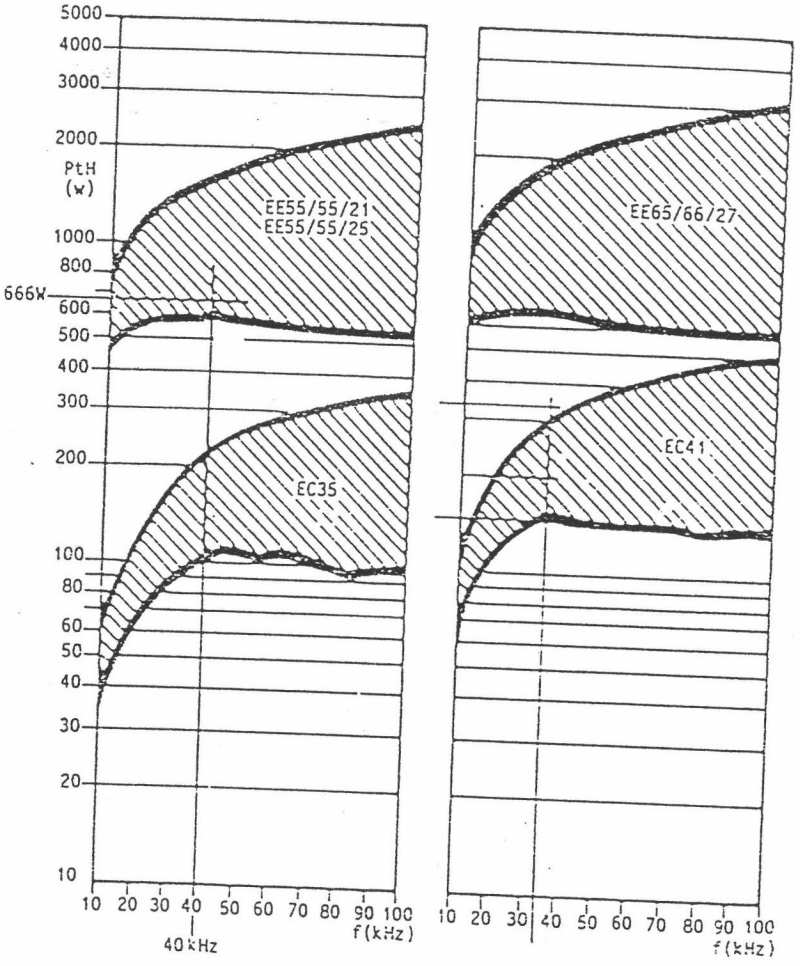


Fig. 16b - Gate charge test circuit.

ภาคผนวก ข


5000
4000
3000
2000
PtH
(w)
1000
800
666W
600
500
400
300
200
100
80
60
50
40
30
20
10
EE55/55/21
EE55/55/25
EC35
10 20 30 40 50 60 70 80 90 100
40kHz
f(kHz)
EE65/66/27
EC41
10 20 30 40 50 60 70 80 90 100
f(kHz)

Shape code	Magnetic parameter				Center leg area	Minimum cross sectional area		Window area	Approx. weight
	C_1 (mm^{-1})	A_e (mm^2)	ℓ_e (mm)	V_e (mm^3)	A_c (mm^2)	Amin. (mm^2)		A_w (mm^2)	(g/pr.)
EE12.6/13	2.4057	12.4	29.7	367	12.6	12.1	L	26.3	1.90
EE13/13B	1.1934	25.1	30.0	752	24.9	23.8	B	26.6	3.70
EE16/14K	1.8662	18.9	35.2	663	18.2	18.2	C	42.6	3.20
EE19/16K	1.7168	23.1	39.6	915	22.8	22.8	C	55.7	4.58
EE19/16Z	1.7715	22.7	40.1	909	22.7	22.7	LBC	55.9	4.56
EE22/20	1.9594	26.1	51.2	1340	24.4	24.4	C	102	13.8
EE25/19A	1.2387	39.8	49.2	1960	41.1	37.1	B	85.6	9.96
EE25/19Z	1.1970	40.2	48.1	1940	40.3	40.0	B	81.0	10.3
EE25/20	1.1561	42.6	49.3	2100	41.0	41.0	C	80.5	10.3
EE30/26K	0.52756	110	57.9	6360	114	107	L	75.8	32.2
EE30/30	1.1538	57.3	66.1	3790	47.6	47.6	C	134	20.7
EE34/28A	0.85153	82.1	69.9	5750	85.9	79.7	B	164	29.5
EE40/34B	0.54389	142	77.5	11000	137	137	C	167	52.0
EE40/34K	0.60782	127	77.4	9860	114	114	C	178	52.0
EE40/35A	0.52569	149	78.1	11600	155	145	L	178	58.8
EE40/44	0.66917	145	97.2	14100	137	137	C	248	71.7
EE42/42-15W	0.54243	180	97.8	17600	180	180	BC	276	86.9
EE42/42-20W	0.41512	236	97.8	23000	235	235	BC	276	118
EE43/34	0.47780	165	78.7	13000	159	159	C	171	65.0
EE47/39A	0.38524	232	89.5	20800	243	223	B	206	106
EE50/42K	0.42677	226	96.3	21700	213	213	C	261	113
EE55/55A	0.34989	353	124	43700	352	352	C	400	218
EE56/47A	0.31597	339	107	36400	352	329	B	292	186
EE80/76	0.49137	377	185	69700	392	352	L	1480	354

Note: Minimum cross sectional area B; Back area C; Center leg area L; Side leg area

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

SG1526
SG2526
SG3526

PULSE WIDTH MODULATION CONTROL CIRCUIT

The SG1526 is a high performance pulse width modulator integrated circuit intended for fixed frequency switching regulators and other power control applications.

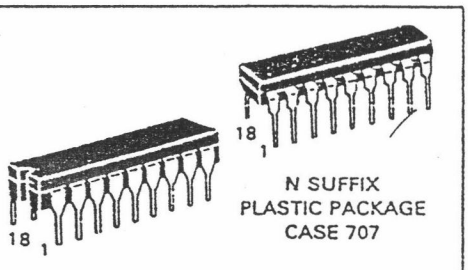
Functions included in this IC are a temperature compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and steering logic, and two high current totem pole outputs ideally suited for driving the capacitance of power FETs at high speeds.

Additional protective features include soft start and undervoltage lockout, digital current limiting, double pulse inhibit, adjustable dead time and a data latch for single pulse metering. All digital control ports are TTL and B-series CMOS compatible. Active low logic design allows easy wired-OR connections for maximum flexibility. The versatility of this device enables implementation in single-ended or push-pull switching regulators that are transformerless or transformer coupled. The SG1526 is specified over the full military junction temperature range of −55°C to +150°C. The SG2526 is specified over a junction temperature range of −40°C to +150°C while the SG3526 is specified over a range of 0°C to +125°C.

- 8.0 to 35 Volt Operation
- 5.0 Volt ±1% Trimmed Reference
- 1.0 Hz to 400 kHz Oscillator Range
- Dual Source/Sink Current Outputs: ±100 mA
- Digital Current Limiting
- Programmable Dead Time
- Undervoltage Lockout
- Single Pulse Metering
- Programmable Soft Start
- Wide Current Limit Common Mode Range
- Guaranteed 6 Unit Synchronization

PULSE WIDTH MODULATION CONTROL CIRCUITS

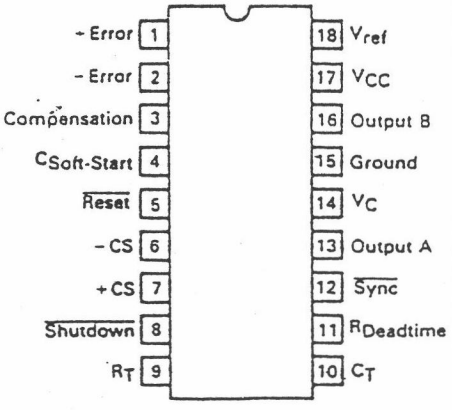
SILICON MONOLITHIC INTEGRATED CIRCUITS



N SUFFIX
PLASTIC PACKAGE
CASE 707

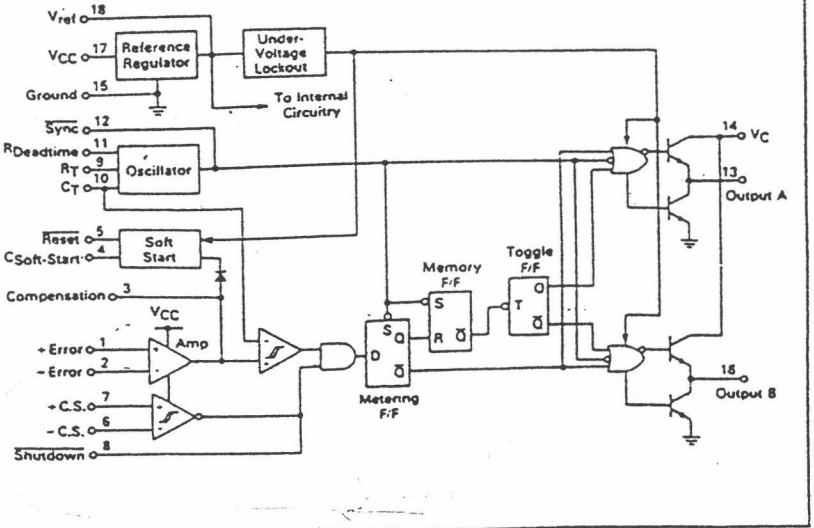
J SUFFIX
CERAMIC PACKAGE
CASE 726

PIN CONNECTIONS



Top View

BLOCK DIAGRAM



ORDERING INFORMATION

Device	Junction Temperature Range	Package
SG1526J	−55 to +150°C	Ceramic DIP
SG2526J SG2526N	−40 to +150°C	Ceramic DIP Plastic DIP
SG3526J SG3526N	0 to +125°C	Ceramic DIP Plastic DIP

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 Vdc, T_J = T_{low} to T_{high} [Note 4] unless otherwise specified)

Characteristic	Symbol	SG1526/2526			SG3526			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION (Note 5)								
Reference Output Voltage (T_J = +25°C)	V_{ref}	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation (+8.0 V ≤ V_{CC} ≤ +35 V)	Reg_{line}	—	10	20	—	10	30	mV
Load Regulation, 0 mA ≤ I_L ≤ 20 mA	Reg_{load}	—	10	30	—	10	50	mV
Temperature Stability	$\Delta V_{ref}/\Delta T_J$	—	15	50	—	15	50	mV
Total Reference Output Voltage Variation (+8.0 V ≤ V_{CC} ≤ +35 V, 0 mA ≤ I_L ≤ 20 mA)	ΔV_{ref}	4.90	5.00	5.10	4.85	5.00	5.15	V
Short Circuit Current (V_{ref} = 0 V)	I_{SC}	25	50	100	25	50	100	mA
UNDERVOLTAGE LOCKOUT								
$\overline{\text{Reset}}$ Output Voltage (V_{ref} = +3.8 V)	—	—	0.2	0.4	—	0.2	0.4	V
$\overline{\text{Reset}}$ Output Voltage (V_{ref} = +4.8 V)	—	2.4	4.8	—	2.4	4.8	—	V
OSCILLATOR SECTION (Note 6)								
Initial Accuracy (T_J = +25°C)	—	—	±3.0	±8.0	—	±3.0	±8.0	%
Frequency Stability over Power Supply Range (+8.0 V ≤ V_{CC} ≤ +35 V)	$\frac{\Delta f_{osc}}{\Delta V_{CC}}$	—	0.5	1.0	—	0.5	1.0	%
Frequency Stability over Temperature (ΔT_J = T_{low} to T_{high})	$\frac{\Delta f_{osc}}{\Delta T_J}$	—	7.0	10	—	3.0	5.0	%
Minimum Frequency (R_T = 150 kΩ, C_T = 20 μF)	f_{min}	—	—	1.0	—	—	1.0	Hz
Maximum Frequency (R_T = 2.0 kΩ, C_T = 0.001 μF)	f_{max}	400	—	—	400	—	—	kHz
Sawtooth Peak Voltage (V_{CC} = +35 V)	$V_{osc(P)}$	—	3.0	3.5	—	3.0	3.5	V
Sawtooth Valley Voltage (V_{CC} = +8.0 V)	$V_{osc(V)}$	0.5	1.0	—	0.5	1.0	—	V
ERROR AMPLIFIER SECTION (Note 7)								
Input Offset Voltage (R_S ≤ 2.0 kΩ)	V_{IO}	—	2.0	5.0	—	2.0	10	mV
Input Bias Current	I_{IB}	—	−350	−1000	—	−350	−2000	nA
Input Offset Current	I_{IO}	—	35	100	—	35	200	nA
DC Open Loop Gain (R_L ≥ 10 MΩ)	A_{Vol}	64	72	—	60	72	—	dB
High Output Voltage ($V_{Pin\ 1}$−$V_{Pin\ 2}$ ≥ +150 mV, I_{source} = 100 μA)	V_{OH}	3.6	4.2	—	3.6	4.2	—	V
Low Output Voltage ($V_{Pin\ 2}$−$V_{Pin\ 1}$ ≥ +150 mV, I_{sink} = 100 μA)	V_{OL}	—	0.2	0.4	—	0.2	0.4	V
Common Mode Rejection Ratio (R_S ≤ 2.0 kΩ)	CMRR	70	94	—	70	94	—	dB
Power Supply Rejection Ratio (+12 V ≤ V_{CC} ≤ +18 V)	PSRR	66	80	—	66	80	—	dB
PWM COMPARATOR SECTION (Note 6)								
Minimum Duty Cycle ($V_{compensation}$ = +0.4 V)	DC_{min}	—	—	0	—	—	0	%
Maximum Duty Cycle ($V_{compensation}$ = +3.6 V)	DC_{max}	45	49	—	45	49	—	%

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Symbol	SG1526/2526			SG3526			Unit
		Min	Typ	Max	Min	Typ	Max	
DIGITAL PORTS (SYNC, SHUTDOWN, RESET)								
Output Voltage — High Logic Level (I_{source} = 40 µA)	V_{OH}	2.4	4.0	—	2.4	4.0	—	V
Output Voltage — Low Logic Level (I_{sink} = 3.6 mA)	V_{OL}	—	0.2	0.4	—	0.2	0.4	V
Input Current — High Logic Level (V_{IH} = +2.4 V)	I_{IH}	—	-125	-200	—	-125	-200	µA
Input Current — Low Logic Level (V_{IL} = +0.4 V)	I_{IL}	—	-225	-360	—	-225	-360	µA
CURRENT LIMIT COMPARATOR SECTION (Note 8)								
Sense Voltage ($R_S \leq 50\ \Omega$)	V_{sense}	90	100	110	80	100	120	mV
Input Bias Current	I_{IB}	—	-3.0	-10	—	-3.0	-10	µA
SOFT-START SECTION								
Error Clamp Voltage ($\overline{Reset}$ = +0.4 V)	—	—	0.1	0.4	—	0.1	0.4	V
Soft-Start Charging Current ($\overline{Reset}$ = +2.4 V)	I_{CS}	50	100	150	50	100	150	µA
OUTPUT DRIVERS (Each Output, V_C = +15 Vdc unless otherwise specified)								
Output High Level I_{source} = 20 mA I_{source} = 100 mA	V_{OH}	 12.5 12	 13.5 13	 — —	 12.5 12	 13.5 13	 — —	V
Output Low Level I_{sink} = 20 mA I_{sink} = 100 mA	V_{OL}	 — —	 0.2 1.2	 0.3 2.0	 — —	 0.2 1.2	 0.3 2.0	V
Collector Leakage, V_C = +40 V	$I_{C(leak)}$	—	50	150	—	50	150	µA
Rise Time (C_L = 1000 pF)	t_r	—	0.3	0.6	—	0.3	0.6	µs
Fall Time (C_L = 1000 pF)	t_f	—	0.1	0.2	—	0.1	0.2	µs
Supply Current (Shutdown = +0.4 V, V_{CC} = +35 V, R_T = 4.12 kΩ)	I_{CC}	—	18	30	—	18	30	mA

Notes:

4. T_{low} = -55°C for SG1526
   -40°C for SG2526
   0°C for SG3526
   T_{high} = +150°C for SG1526/2526
   +125°C for SG3526
5. I_L = 0 mA unless otherwise noted.
6. f_{osc} = 40 kHz (R_T = 4.12 kΩ ±1%, C_T = 0.01 µF ±1%, R_D = 0 Ω)
7. $0 V \leq V_{CM} \leq +5.2 V$
8. $0 V \leq V_{CM} \leq +12 V$

TYPICAL CHARACTERISTICS

FIGURE 1 — SG1526 REFERENCE STABILITY OVER TEMPERATURE

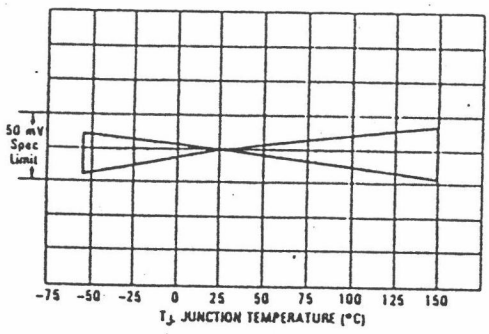


FIGURE 2 — REFERENCE VOLTAGE AS A FUNCTION SUPPLY VOLTAGE

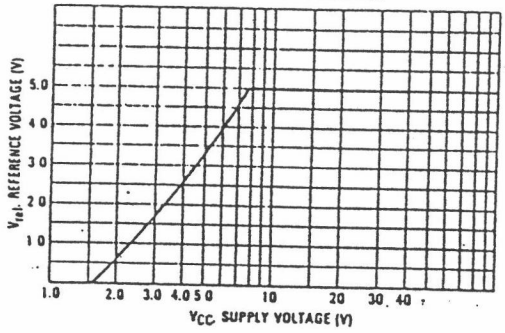


FIGURE 3 — ERROR AMPLIFIER OPEN LOOP FREQUENCY RESPONSE

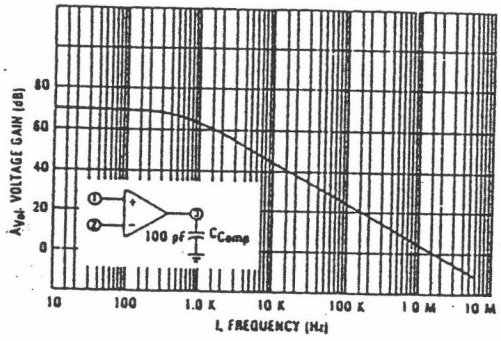


FIGURE 4 — CURRENT LIMIT COMPARATOR THRESHOLD

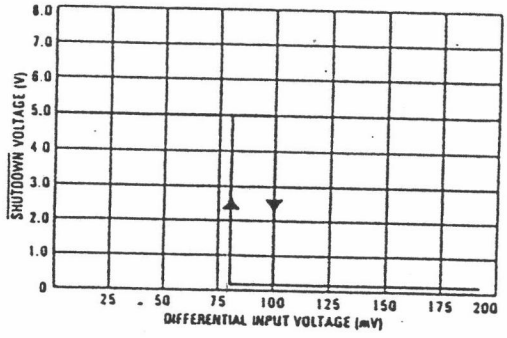


FIGURE 5 — UNDERVOLTAGE LOCKOUT CHARACTERISTIC

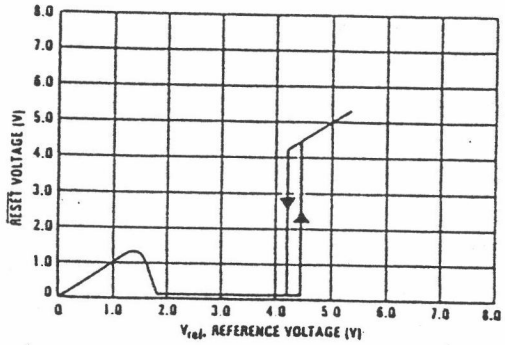


FIGURE 6 — OUTPUT DRIVER SATURATION VOLTAGE AS A FUNCTION OF SINK CURRENT

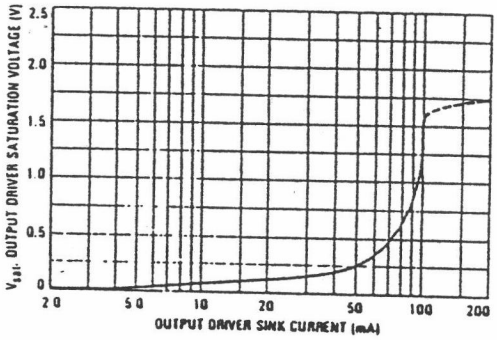


FIGURE 7 — V_C SATURATION VOLTAGE AS A FUNCTION OF SINK CURRENT

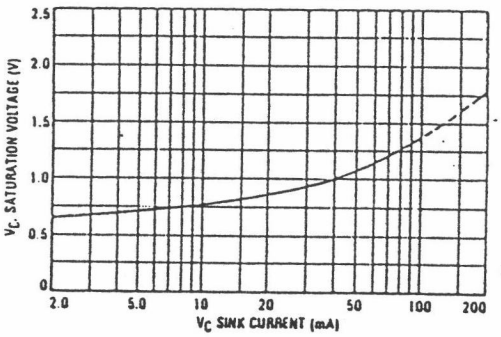


FIGURE 8 — SG1526 OSCILLATOR PERIOD

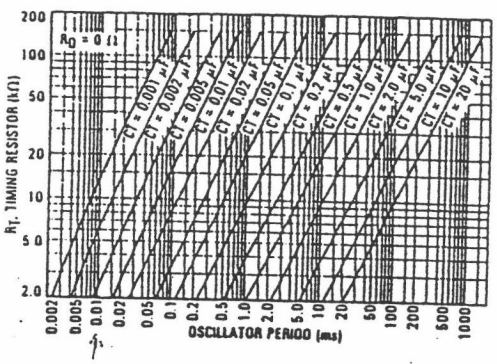


FIGURE 9 — OUTPUT DEADTIME AS A FUNCTION OF DEADTIME RESISTOR VALUE

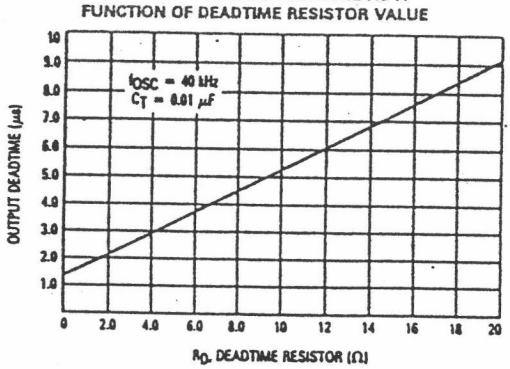


FIGURE 10 — SG1526 ERROR AMPLIFIER

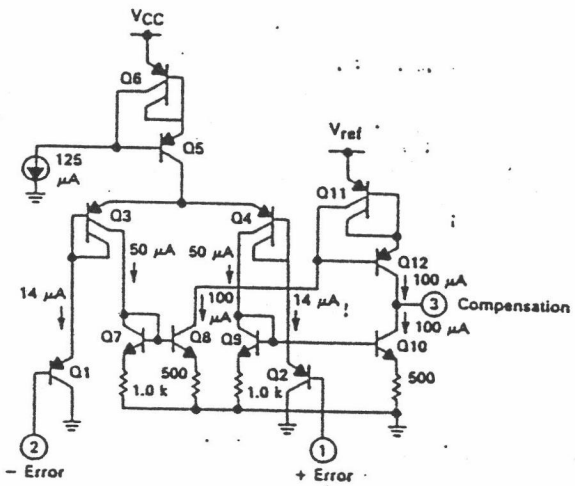


FIGURE 11 — SG1526 UNDERVOLTAGE LOCKOUT

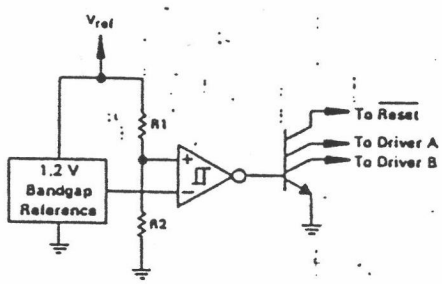
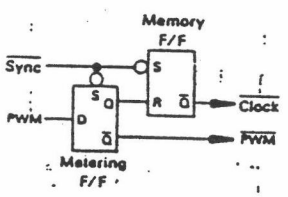


FIGURE 12 — SG1526 PULSE PROCESSING LOGIC

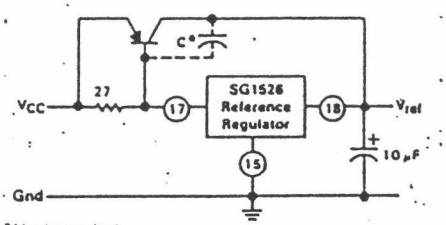


The metering FLIP-FLOP is an asynchronous data latch which suppresses high frequency oscillations by allowing only one PWM pulse per oscillator cycle.

The memory FLIP-FLOP prevents double pulsing in a push-pull configuration by remembering which output produced the last pulse.

APPLICATIONS INFORMATION

FIGURE 13 — EXTENDING REFERENCE OUTPUT CURRENT CAPABILITY



*May be required with some types of transistors

FIGURE 14 — ERROR AMPLIFIER CONNECTIONS

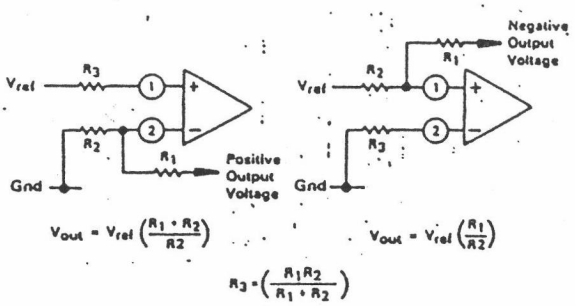


FIGURE 15 — OSCILLATOR CONNECTIONS

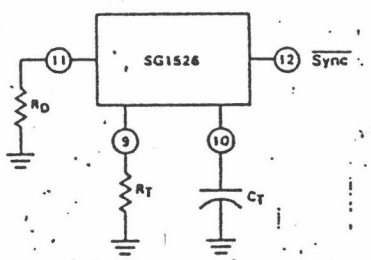


FIGURE 16 — FOLDBACK CURRENT LIMITING

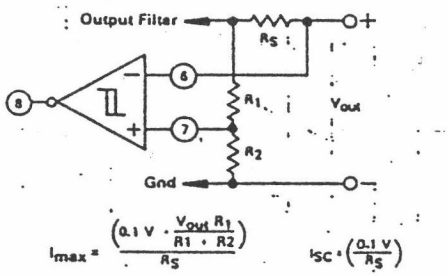


FIGURE 17 — SG1526 SOFT-START CIRCUITRY

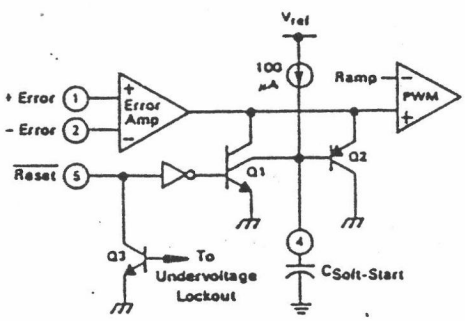
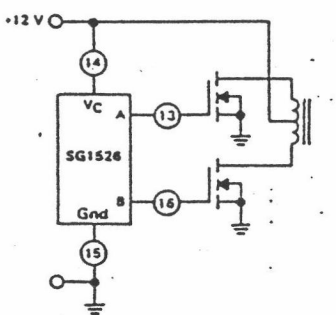


FIGURE 18 — DRIVING TMOS POWER FETS



The totem-pole output drivers of the SG1526 are ideally suited for driving the input capacitance of power FETs at high speeds.

FIGURE 19 — HALF-BRIDGE CONFIGURATION

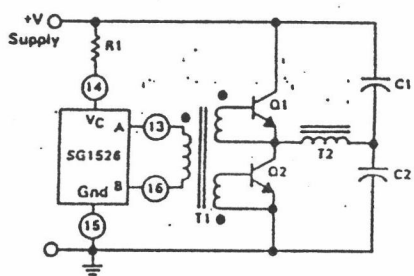
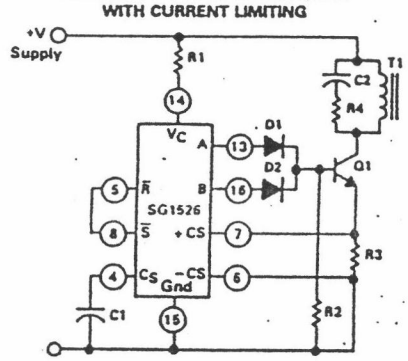


FIGURE 20 — FLYBACK CONVERTER WITH CURRENT LIMITING



In the above circuit, current limiting is accomplished by using the current limit comparator output to reset the soft-start capacitor.

FIGURE 21 — SINGLE-ENDED CONFIGURATION

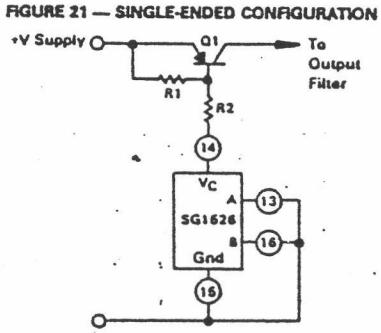
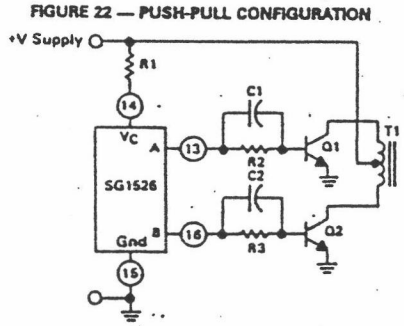


FIGURE 22 — PUSH-PULL CONFIGURATION



ประวัติผู้เขียน

นายคุปต์ โพธิ์แก้ว เกิดวันที่ 9 กุมภาพันธ์ พ.ศ. 2511 ที่จังหวัดกรุงเทพมหานคร สำเร็จการศึกษาปริญญาตรีวิศวกรรมศาสตรบัณฑิต สาขาวิศวกรรมไฟฟ้า จากมหาวิทยาลัยเกษตรศาสตร์ ในปีการศึกษา 2533 และทำงานเป็นวิศวกรระดับ 4 ฝ่ายควบคุมระบบกำลังไฟฟ้า การไฟฟ้าฝ่ายผลิตแห่งประเทศไทย พ.ศ. 2533 ถึง พ.ศ. 2535 เข้าศึกษาต่อในหลักสูตรวิศวกรรมศาสตรมหาบัณฑิต สาขาวิชานิวเคลียร์เทคโนโลยี ที่จุฬาลงกรณ์มหาวิทยาลัย เมื่อ พ.ศ. 2536 ปัจจุบันทำงานอยู่ที่มหาวิทยาลัยเทคโนโลยีมหานคร