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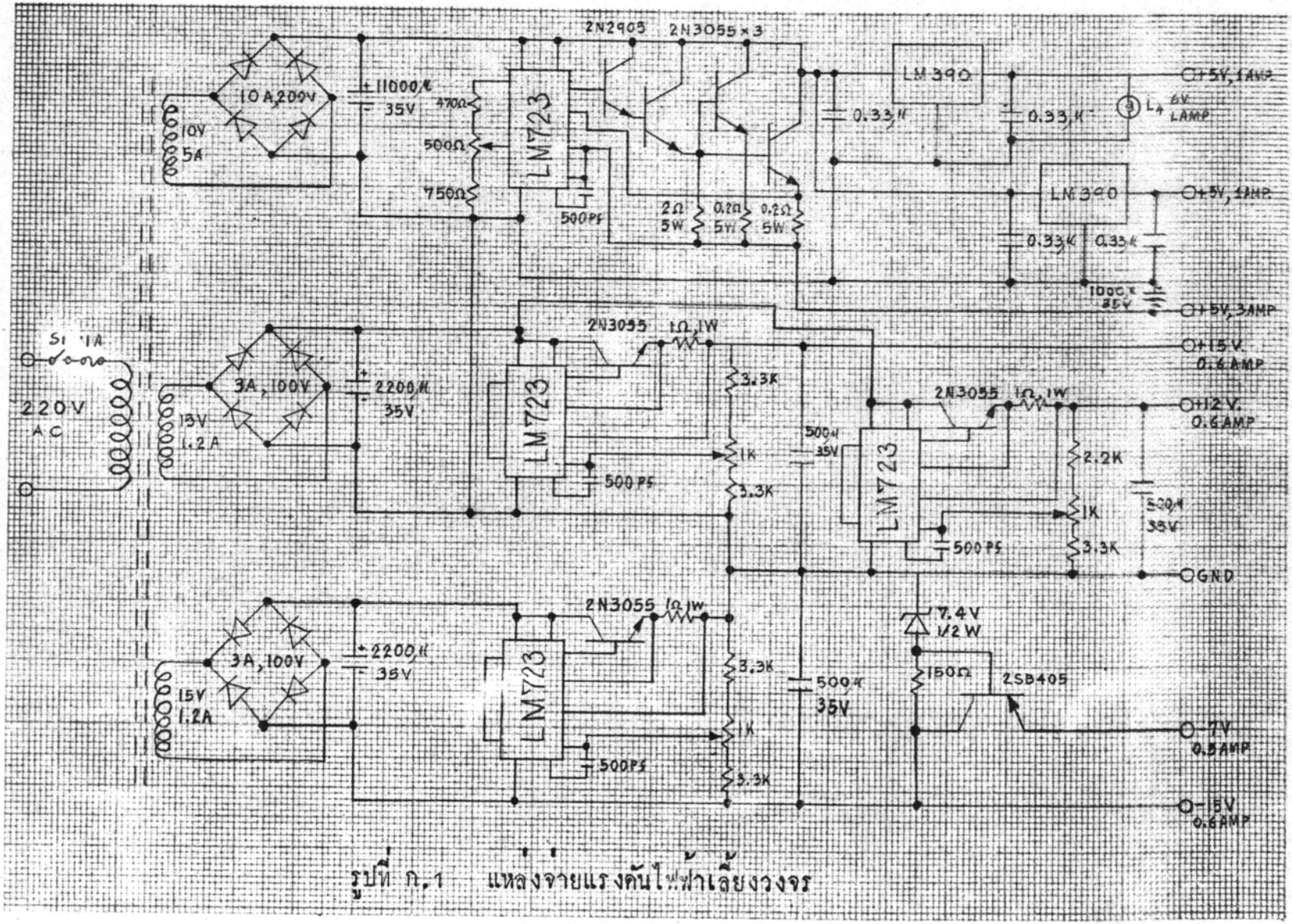
ภาคผนวก

ภาคผนวก ก.

แหล่งจ่ายแรงดันไฟฟ้า

แรงดันไฟฟ้าที่ใช้ในวงจรมีหลายระดับ คือ 5, 12, 15, -6 และ -15 โวลท์ แหล่งจ่ายแรงดันแต่ละแหล่งใช้จ่ายกระแสให้วงจรไม่เท่ากัน ที่แรงดัน 5 โวลท์เครื่องๆจะดึงกระแสประมาณ 4 แอมป์ เพื่อจ่ายให้แก่ไอซีในตระกูล TTL ที่แรงดัน 15 โวลท์ เครื่องๆดึงกระแสประมาณ 300 มิลิแอมป์ เพื่อจ่ายให้แก่ไอซี ออบแอมป์ แรงดัน 12 โวลท์เครื่องๆจะดึงกระแสประมาณ 200 มิลิแอมป์เพื่อจ่ายให้แก่วงจรรีเลย์ไดรเวอร์ และตัวเปรียบเทียบ และแรงดัน-6 โวลท์ ดึงกระแส 100 มิลิแอมป์ เพื่อจ่ายให้ตัวเปรียบเทียบ

เราใช้วงจรจ่ายแรงดันในรูปที่ ก.1 ระดับแรงดัน 5 โวลท์นั้นเราสร้างแหล่งจ่ายแรงดัน 3 แหล่ง เพื่อช่วยในการแบ่งจ่ายกระแสให้แก่วงจรต่างๆ ทำให้ปัญหาเรื่องสัญญาณรบกวนระหว่างวงจร-เนื่องจ่ายแรงดันลดลง



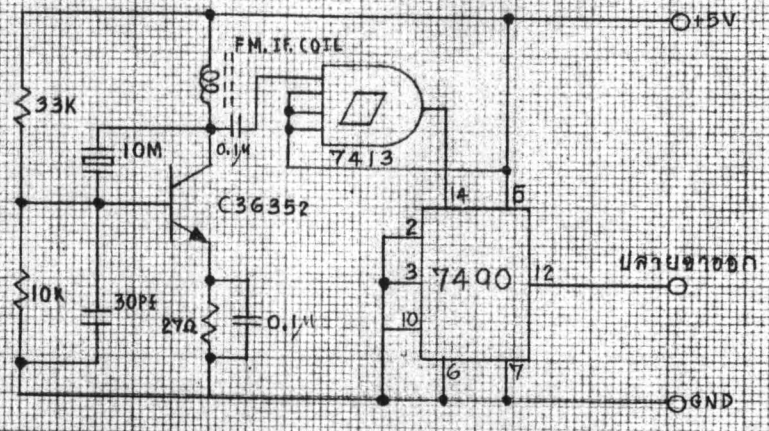
รูปที่ ก.1 แหล่งจ่ายแรงดันไฟฟ้าเลี้ยงวงจร

ภาคผนวก ข.

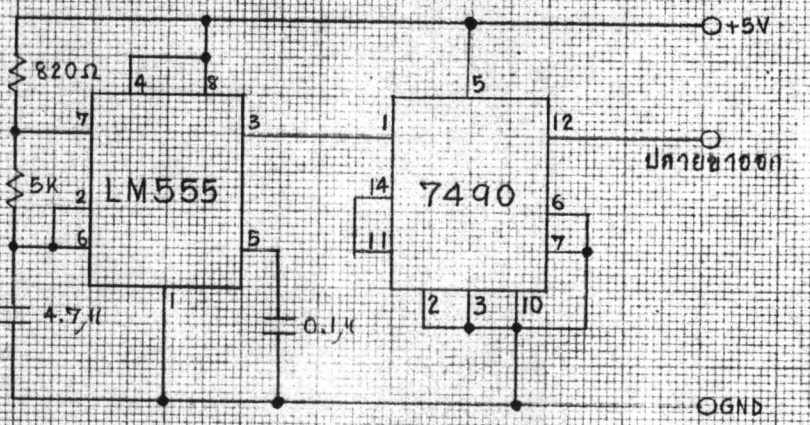
วงจรสร้างสัญญาณความถี่คงที่

ความถี่คงที่ที่ใช้ในเครื่องฯมีอยู่ 2 ความถี่ คือ 5 เมกกะเฮิร์ท และ 2 เฮิร์ท โดยสัญญาณความถี่ทั้งสองจะต้องเป็นสัญญาณสี่เหลี่ยมที่มีระดับแรงดัน 2 ระดับ คือ ศูนย์ และมากกว่า 2 โวลท์ เนื่องจากสัญญาณความถี่ 5 เมกกะเฮิร์ทนั้นเราต้องการความคงที่ของความถี่สูงมาก เราจึงใช้วงจร Crystal control oscillator โดยใช้ผลึกควอตที่ใช้ควบคุมความถี่ขนาด 10 เมกกะเฮิร์ท เมื่อหารสัญญาณที่ได้ด้วย 2 จะทำให้ได้ความถี่ 5 เมกกะเฮิร์ท วงจรสร้างสัญญาณความถี่คงที่ 5 เมกกะเฮิร์ทได้แสดงในรูปที่ ข.1 ส่วนความถี่ 2 เฮิร์ทเราสร้างโดยใช้ไอซีเบอร์ LM 555 โดยต่อเป็นวงจรเอนกระรัวแบบอะเสถียร ที่มีความถี่ขาออกประมาณ 20 เฮิร์ท แล้วหารความถี่ที่ได้ด้วย 10 จะได้สัญญาณออกมีความถี่ 2 เฮิร์ท รูปที่ ข.2 แสดงวงจรสร้างสัญญาณความถี่คงที่ 2 เฮิร์ท

หอสมุดกลาง จุฬาลงกรณมหาวิทยาลัย



รูปที่ ข.1 วงจรสร้างสัญญาณความถี่คงที่ 5 เมกกะเฮิร์ท

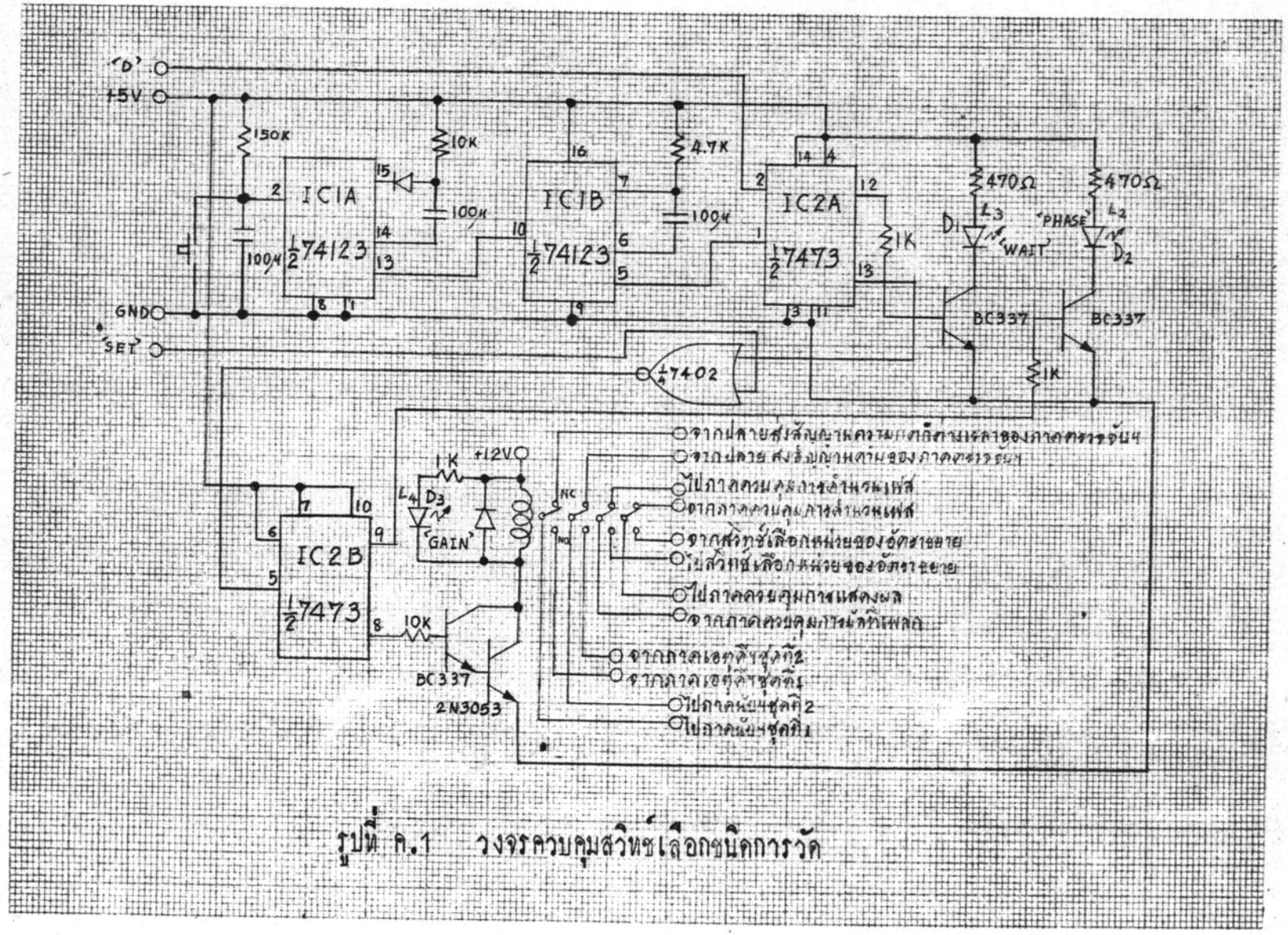


รูปที่ ข.2 วงจรสร้างสัญญาณความถี่คงที่ 2 เฮิร์ท

ภาคผนวก ค.

วงจรควบคุมสวิทช์เลือกชนิดการวัด

เนื่องจากการทำงานของภาคควบคุมจะทำงานตามลำดับก่อนหลัง ดังนั้นเราจะเปลี่ยนชนิดการวัดก่อนที่ภาคคำนวนทำงานเสร็จสิ้นไม่ได้ แต่ในขณะที่เครื่องวิเคราะห์วงจรแบบดิจิทอลทำงาน เราจะไม่มีทางรู้เลยว่าภาคควบคุมทำงานเสร็จสิ้นหรือยัง เราจึงใช้วงจรอีเลคโทรนิคในการควบคุมให้เปลี่ยนชนิดการวัดในเวลาที่เหมาะสม วงจรควบคุมสวิทช์เลือกชนิดการวัดที่ได้ออกแบบแสดงในรูปที่ ค.1 ตัว IC1A เป็นไอซีเอนกระรัวทำหน้าที่สร้างสัญญาณหนึ่งลูกคลื่นที่มีความกว้างมาก เพื่อลดปัญหาของสัญญาณรบกวน-เนื่องจากตัวสวิทช์ ตัว IC1B ทำหน้าที่สร้างพัลซ์แคบๆไปทำให้ IC2A ซึ่งเป็น JK ฟลิบฟลอบมีปลายขา 13 เป็น "0" ดังนั้นถ้าปลายที่ใช้ลบตัวฟลิบฟลอบของภาคควบคุมการแสดงผลส่งสัญญาณพัลซ์มา ตัว IC2B เปลี่ยนสภาวะของปลายขาออกทำให้รีเลย์เปลี่ยนสภาวะด้วย หลังจากนั้นเมื่อปลาย D จากภาคควบคุมการแสดงผลส่งสัญญาณมา จะทำให้ปลายขา 13ของ IC2A มีระดับแรงดันเป็น "1" ตัว LED D_1 ทำหน้าที่แสดงผลว่ามีคำสั่งให้เปลี่ยนชนิดการวัดแต่ยังไม่ได้เปลี่ยนชนิดการวัด LED D_2 ทำหน้าที่แสดงผลว่ากำลังทำการวัดความแตกความแตกต่างมุม LED D_3 ทำหน้าที่แสดงผลว่ากำลังทำการวัดอัตราขยาย



รูปที่ ค.1 วงจรควบคุมสวิทช์เลือกชนิดการวัด

หอสมุดกลาง จุฬาลงกรณมหาวิทยาลัย

ภาคผนวก ง.

วิธีใช้เครื่องวิเคราะห์วงจรแบบดิจิทอล

หลังจากที่เราได้ออกแบบเครื่องวิเคราะห์วงจรแบบดิจิทอลแล้ว เราได้สร้างเครื่องต้นแบบดังแสดงในรูปที่ ง.1 รายละเอียดของการใช้งานของส่วนต่างๆบนหน้าปัดของเครื่องฯ ที่ได้แสดงในรูปที่ ง.2 มีดังนี้คือ

1. สวิทช์ S_1(POWER) เป็นสวิทช์แบบเปิดปิดทำหน้าที่เปิดปิดแหล่งจ่ายไฟฟ้ากำลังของเครื่องฯ

2. สวิทช์ S_2(RESET) เป็นสวิทช์แบบกดทำหน้าที่หยุดการทำงานของเครื่องฯ การทำงานของสวิทช์นี้ใช้วิธีการตัดแหล่งจ่ายแรงดันของภาคควบคุมและแคลคูเลเตอร์ชิพ

3. สวิทช์ S_3(MODE) เป็นสวิทช์แบบกดทำหน้าที่เปลี่ยนชนิดของการวัด (ดูภาคผนวก ก)

4. สวิทช์ S_4(GAIN) เป็นสวิทช์แบบเปิดปิด ทำหน้าที่เลือกชนิดการวัดอัตราขยายให้มีหน่วยเป็นเดซิเบล หรือเท่าตามต้องการ

5. สวิทช์ S_5(CHANNEL A) เป็นสวิทช์แบบเปิดปิดทำหน้าที่เลือกอัตราขยายของวงจรขยายขาเข้าของ Channel A ให้เป็นหนึ่งหรือสิบเท่า

6. สวิทช์ S_6(CHANNEL B) เป็นสวิทช์แบบเปิดปิดทำหน้าที่เลือกอัตราขยายของวงจรขยายขาเข้าของ Channel B ให้เป็นหนึ่งหรือสิบเท่า

7. หลอดไฟ L_1(RESET) จะสว่างในขณะที่กดสวิทช์ S_2

8. หลอดไฟ L_2(PHASE) จะสว่างในขณะที่กดเครื่องฯกำลังทำการวัดความแตกต่างมุม

9. หลอดไฟ L_3(WAIT) จะสว่างหลังจากกดสวิทช์ S_3แล้วแต่เครื่องยังไม่ได้เปลี่ยนชนิดการวัด

10. หลอดไฟ L_4(GAIN) จะสว่างในขณะที่เครื่องฯกำลังทำการวัดอัตราขยาย

11. หลอดไฟ L_5 จะสว่างทันทีที่เครื่องเริ่มทำงาน

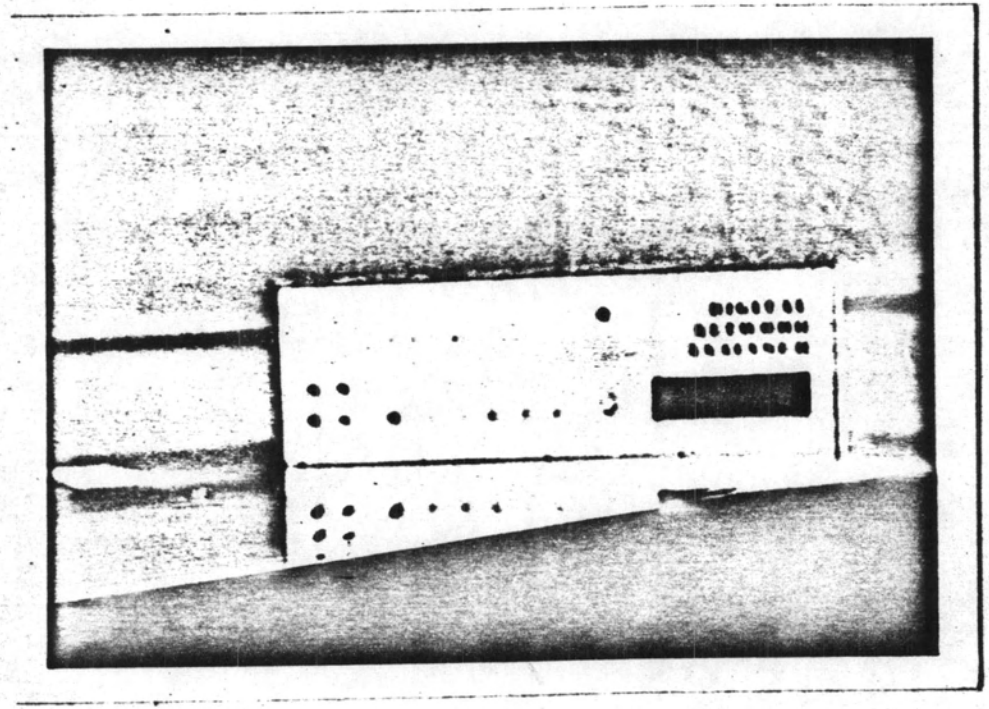
12. รูเลียบสาย J_1 และ J_2(CHANNEL A และ CHANNEL B) เป็นปลายต่อสัญญาณขาเข้าทั้งสองของเครื่องฯ

13. รูเลียบสาย J_3(GND) เป็นปลายสายดินของเครื่อง

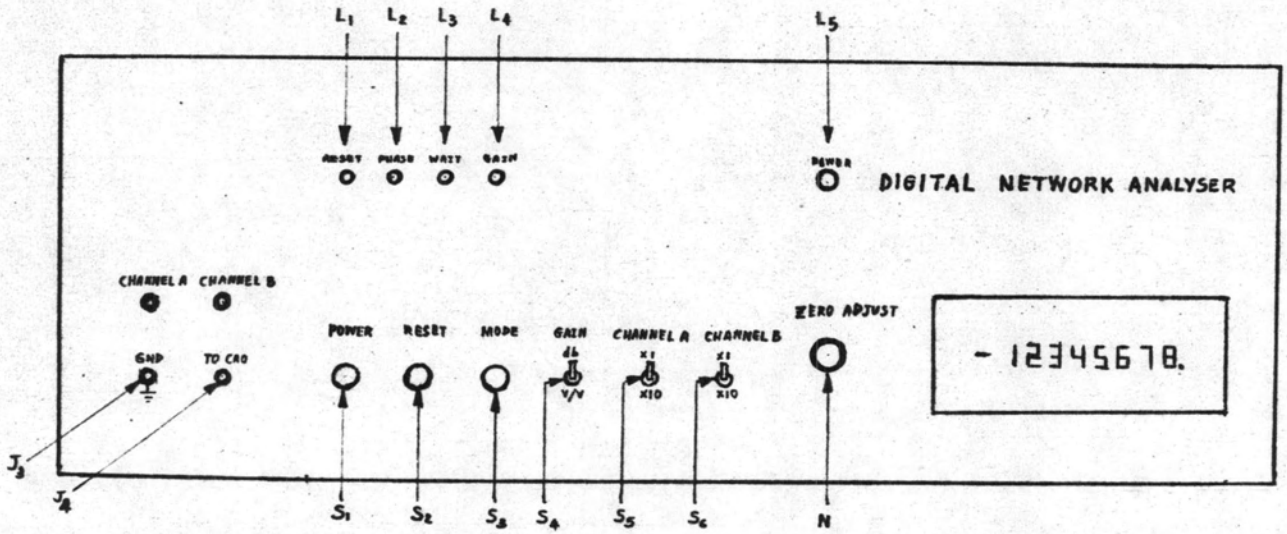
14. รูเลียบสาย J_4(To CRO) เป็นปลายที่ใช้ต่อเข้ากับ Cathode-ray osciloscope เพื่อดูความแตกต่างมุมของสัญญาณขาเข้าทั้งสอง

15. ปุ่มปรับ N (Zero Adjust) ทำหน้าที่ปรับให้การวัดความแตกต่างมุมทำได้อย่างถูกต้อง การปรับจะกระทำโดยป้อนสัญญาณสองอันที่ความถี่ที่ต้องการวัดที่มีความแตกต่างมุมเป็นศูนย์เข้าสู่เครื่อง แล้วปรับปุ่ม N ให้ค่าที่อ่านได้เป็นศูนย์ การปรับด้วยวิธีนี้ทำได้ยากเราจะใช้วิธีเอา Cathode-ray osciloscope จับสัญญาณจากรูเลียบสาย J_4 แล้วปรับปุ่ม N จนกระทั่งรูปคลื่นที่ปรากฏเป็นเส้นตรง การปรับปุ่ม N นี้ควรจะทำทุกๆครั้งที่เปลี่ยนความถี่ของสัญญาณที่เข้าสู่เครื่อง

ในการวัดอัตราขยายค่าที่แสดงจะเป็นอัตราส่วนของสัญญาณจาก CHANNEL A ต่อ CHANNEL B ส่วนการวัดความแตกต่างมุมค่าที่อ่านจะเป็นค่าของมุมของสัญญาณจาก CHANNEL A โดยเทียบกับสัญญาณขาเข้าจาก CHANNEL B



รูปที่ ง.1: เครื่องวิเคราะห์วงจรแบบดิจิทอลต้นแบบที่สร้างขึ้น.



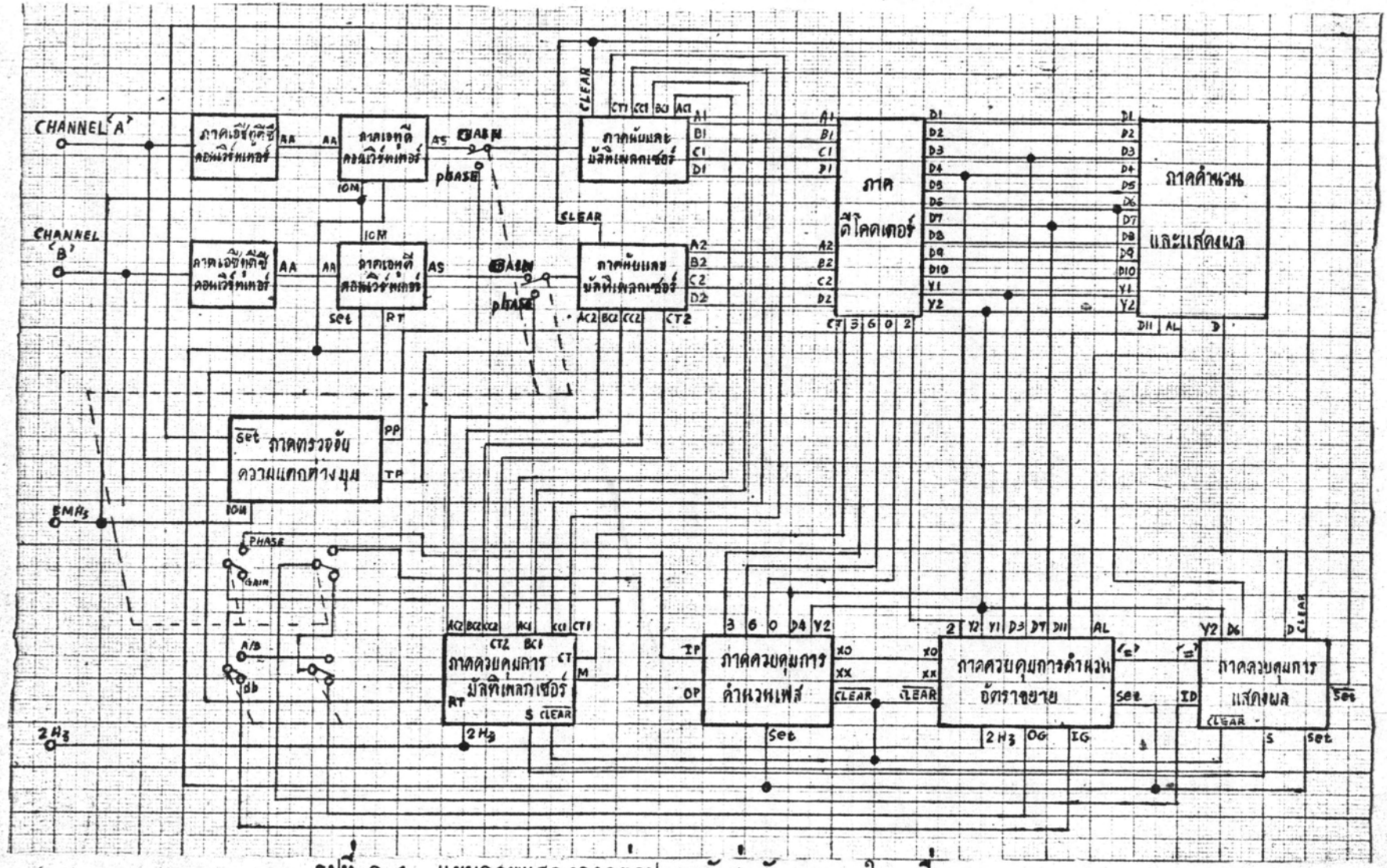
รูปที่ ง.2 ภาพแสดงหน้าปัดของเครื่องวิเคราะห์วงจรต้นแบบที่สร้างขึ้น

หอสมุดกลาง
จุฬาลงกรณมหาวิทยาลัย

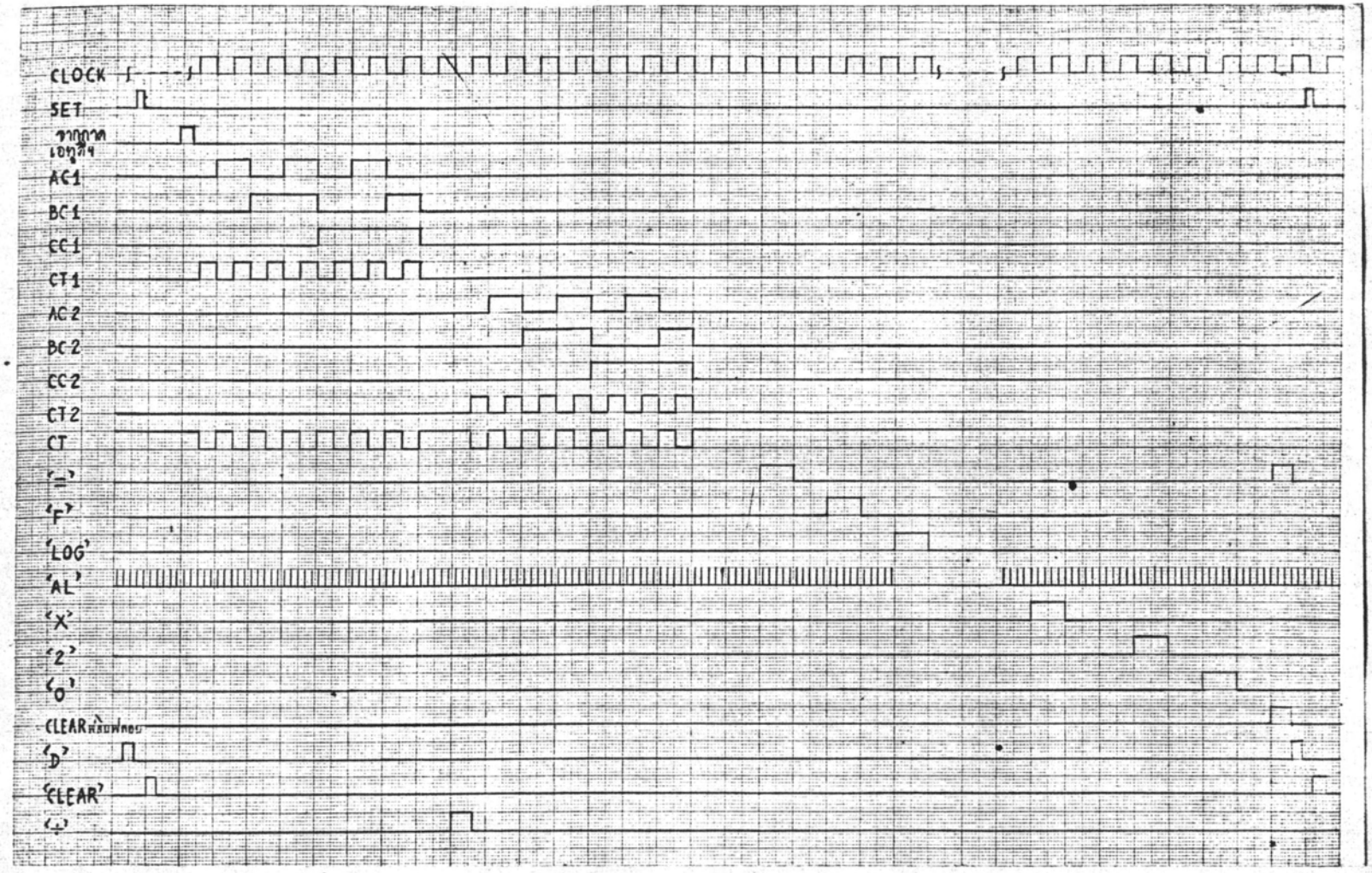
ภาคผนวก จ.

แผนภาพที่สมบูรณ์ของเครื่องวิเคราะห์วงจรแบบดิจิทอลที่ได้ออกแบบ

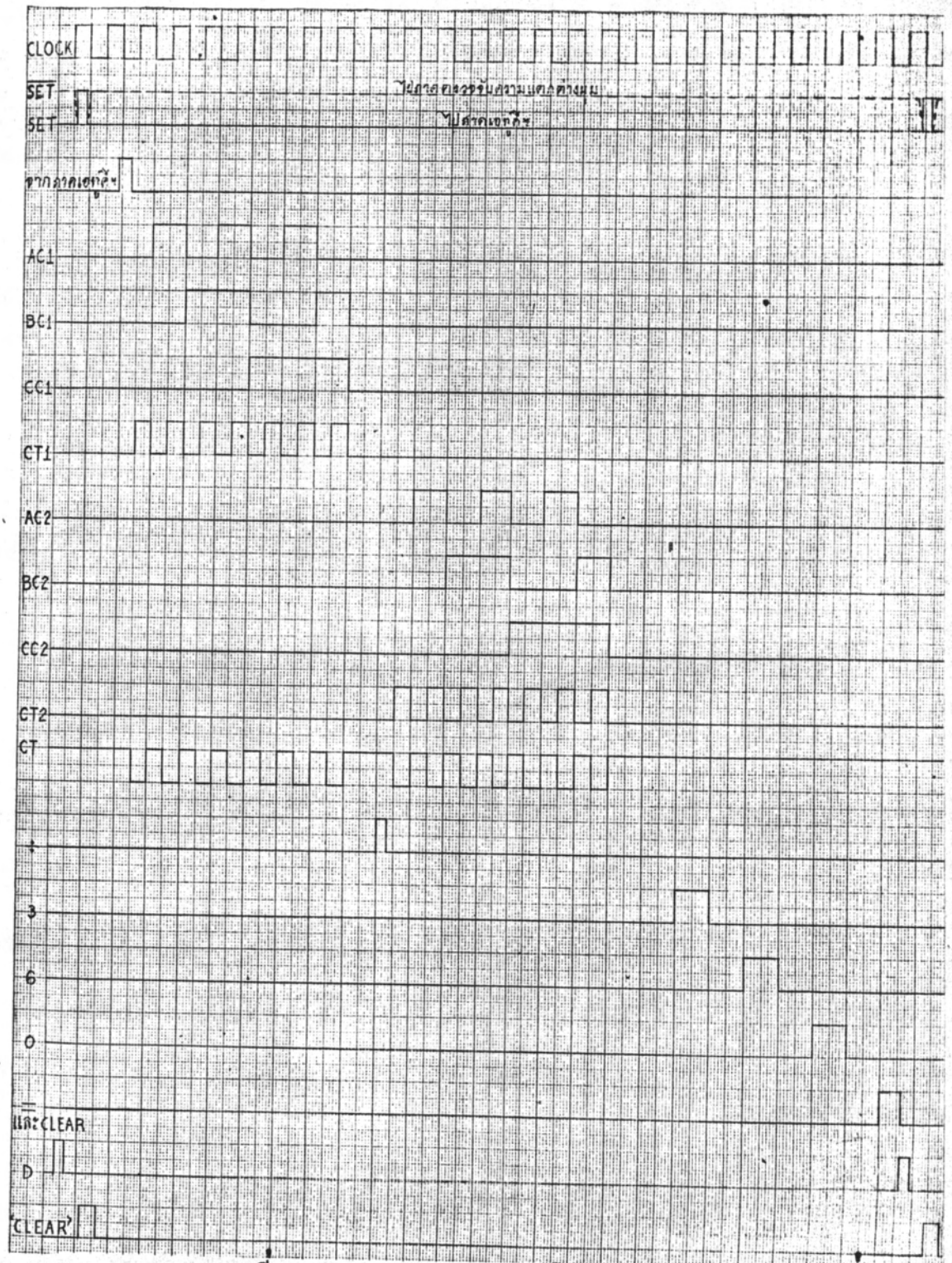
จากวงจรต่างๆที่ได้ออกแบบไว้ในบทที่ 3 เรานำมาประกอบกันเข้าเป็นเครื่องวิเคราะห์วงจรแบบดิจิทอลโดยมีแผนภาพการต่อปลายรับและส่งสัญญาณต่างๆของภาคต่างๆภายในเครื่องฯ ดังแสดงในรูป จ.1 สัญญาลักษณ์ต่างๆที่กำหนดลงตรงปลายต่อสัญญาณต่างๆจะตรงกับปลายรับหรือส่งสัญญาณในวงจรนั้นที่ได้แสดงในบทที่ 3 รูปที่ จ.2 และ จ.3 เป็น Timing diagram ของการวัดอัตราขยายและความแตกต่างมุมตามลำดับ



รูปที่ จ.1 แผนภาพแสดงการตอปลายรับสงสัญญาณภายในเครื่องฯ



รูปที่ จ.2 Timing Diagram ของการวัดอัตราขยาย



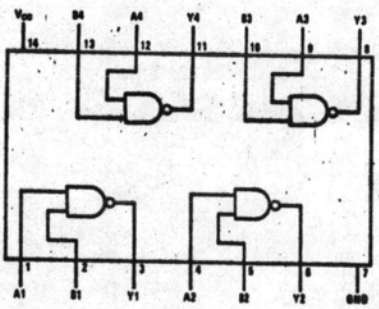
รูปที่ จ.3 Timing Diagram ของการวัดความแตกต่างมุม

ภาคผนวก ฉ.
ข้อมูลของไอซีต่างๆที่ใช้

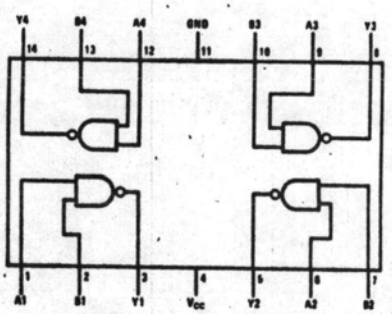
SSI — **DM54/DM74 Connection Diagrams/Gates**

00 Quad 2-Input NAND Gates

$Y = \overline{AB}$



5400/7400(J), (N); 54H00/74H00(J), (N); 54L00/74L00(J), (N); 54LS00/74LS00(J),(N),(W); 74S00(N)

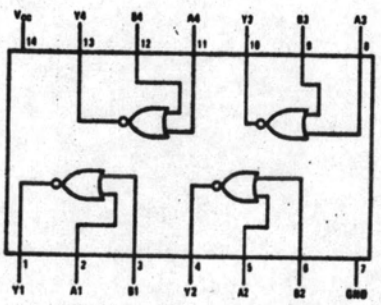


5400/7400(W); 54L00/74L00(W)

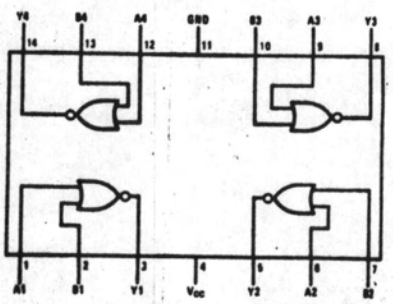
See page 1-36 for electrical tables.

02 Quad 2-Input NOR Gates

$Y = \overline{A+B}$



5402/7402(J), (N); 54L02/74L02(J), (N); 54LS02/74LS02(J), (N), (W); 74S02(N)

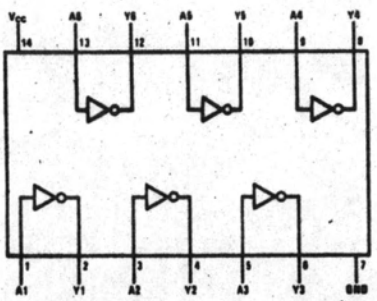


5402/7402(W); 54L02/74L02(W)

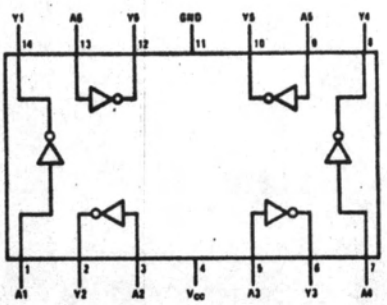
See page 1-40 for electrical tables.

04 Hex Inverters

$Y = \overline{A}$



5404/7404(J), (N); 54H04/74H04(J), (N); 54L04/74L04(J), (N), 54LS04/74LS04(J),(N),(W); 74S04(N)

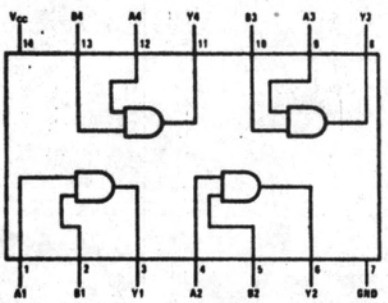


5404/7404(W); 54L04/74L04(W)

See page 1-36 for electrical tables.

08 Quad 2-Input AND Gates

$Y = AB$

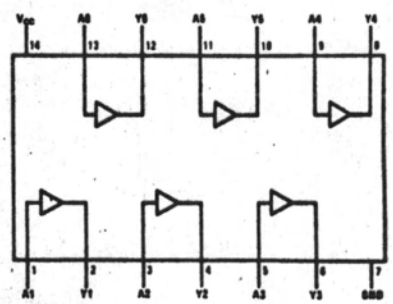


5408/7408(J), (N), (W); 54H08/74H08(J), (N); 54L08/74L08(J), (N), (W); 54LS08/74LS08(J), (N), (W)

See page 1-44 for electrical tables.

17 Hex Buffers with Open-Collector High-Voltage Outputs

$Y = A$

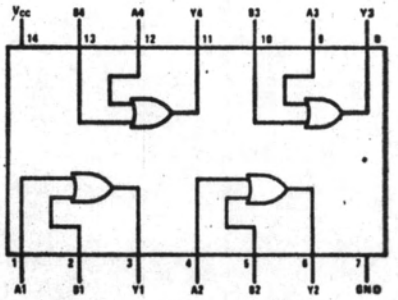


5417/7417(J),(N),(W)

See page 1-42 for electrical tables.

32 Quad 2-Input OR Gates

$Y = A + B$



5432/7432(J),(N),(W);54L32/74L32(J),(N),(W);
54LS32/74LS32(J),(N),(W)

See page 1-52 for electrical tables.

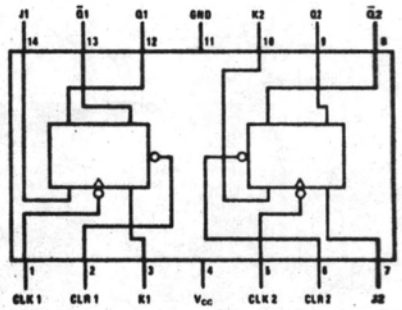
73 Dual J-K Flip-Flops with Clear

TRUTH TABLE
73, H73, L73

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	⊓	L	L	Q0	$\bar{Q}$0
H	⊓	H	L	H	L
H	⊓	L	H	L	H
H	⊓	H	H	TOGGLE	

TRUTH TABLE
LS73

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	Q0	$\bar{Q}$0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\bar{Q}$0



5473/7473(J), (N), (W); 54H73/74H73(J), (N);
54L73/74L73 (J), (N), (W);
54LS73/74LS73(J), (N), (W)

See page 1-62 (73), 1-64 (H73), 1-66 (L73), 1-68 (LS73) for electrical tables.

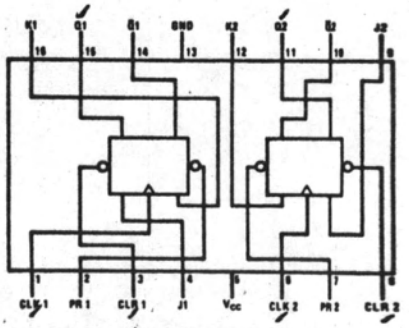
76 Dual J-K Flip-Flops with Preset and Clear

TRUTH TABLE
76, H76

INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⊓	L	L	Q0	$\bar{Q}$0
H	H	⊓	H	L	H	L
H	H	⊓	L	H	L	H
H	H	⊓	H	H	TOGGLE	

TRUTH TABLE
LS76

INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q0	$\bar{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	$\bar{Q}$0



5476/7476(J), (N), (W); 54H76/74H76(J), (N);
54LS76/74LS76(J), (N), (W)

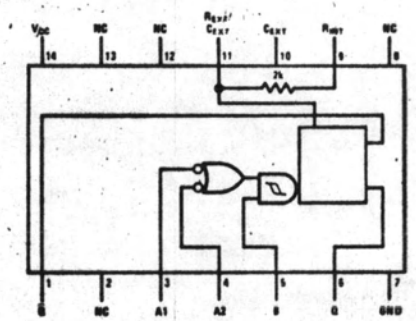
See page 1-62 (76), 1-64 (H76), 1-68 (LS76) for electrical tables.

121 One Shots

TRUTH TABLE

INPUTS			OUTPUTS	
A1	A2	B	Q	$\bar{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⎍	⎎
↓	H	H	⎍	⎎
↓	↓	H	⎍	⎎
L	X	↑	⎍	⎎
X	L	↑	⎍	⎎

See page 1-76 for electrical tables.



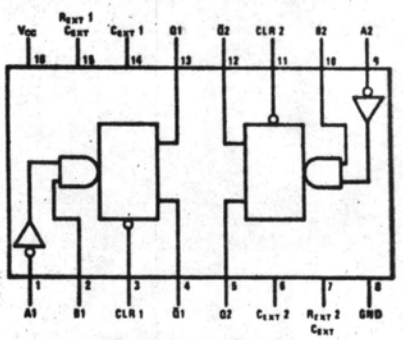
54121/74121(J), (N), (W)

123,123A Dual Retriggerable One Shots with Clear

TRUTH TABLE

INPUTS			OUTPUTS	
A	B	CLR	Q	$\bar{Q}$
H	X	H	L	H
X	L	H	L	H
L	↑	H	⎍	⎎
↓	H	H	⎍	⎎
X	X	L	L	H

See page 1-78 for electrical tables.



54123/74123(J), (N), (W);
54L123A/74L123A(J), (N), (W);
54LS123/74LS123(J), (N), (W)

Notes: ⎍ = one high-level pulse, ⎎ = one low-level pulse.
To use the internal timing resistor of 54121/74121, connect R_{INT} to V_{CC}.
An external timing capacitor may be connected between C_{EXT} and R_{EXT}/C_{EXT} (positive).
For accurate repeatable pulse widths, connect an external resistor between R_{EXT}/C_{EXT} and V_{CC} with R_{INT} open-circuited.
To obtain variable pulse widths, connect external variable resistance between R_{INT} or R_{EXT}/C_{EXT} and V_{CC}.

MSI

DM54/DM7475,L75A,LS75,LS77

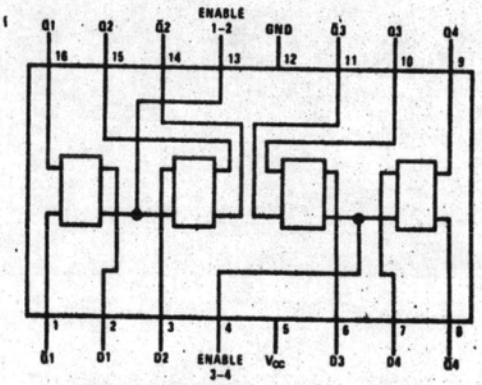
Quad Latches

General Description

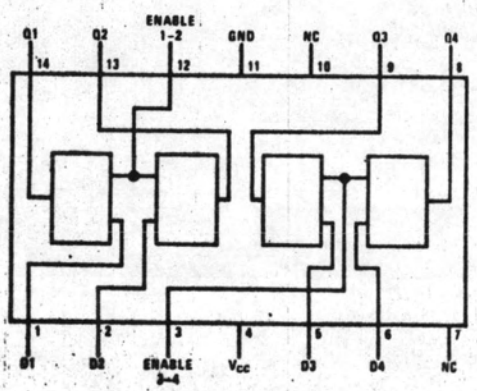
These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high, and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

The DM5475/DM7475, DM54L75A/DM74L75A, and DM54LS75/DM74LS75 feature complementary Q and $\overline{Q}$ outputs from a 4-bit latch, and are available in 16-pin packages. For higher component density applications, the DM54LS77/DM74LS77 4-bit latches are available in 14-pin flat packages (only).

Connection Diagrams



5475/7475(J), (N), (W); 54L75A/74L75A(J), (N), (W); 54LS75/74LS75(J), (N), (W)



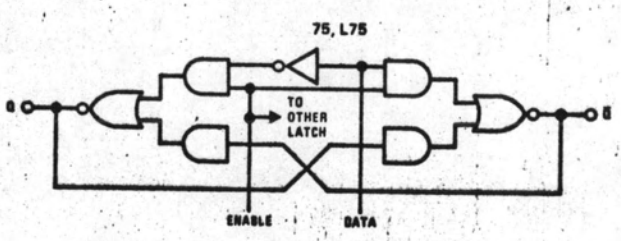
54LS77/74LS77(W)

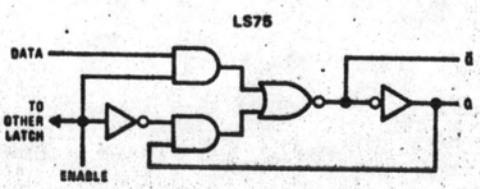
Truth Table (Each Latch)

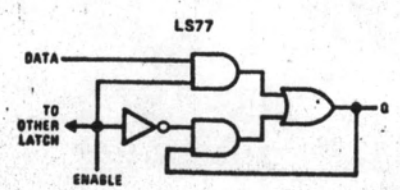
INPUTS		OUTPUTS	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = High Level, L = Low Level, X = Don't Care
Q_0 = The Level of Q Before the High-to-Low Transition of G

Logic Diagrams (Each Latch)







MSI

DM54/DM7490A,L90,LS90,92A,LS92,93A,L93,LS93

Decade, Divide by 12, and Binary Counters

General Description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the 90A, L90, and LS90, divide-by-six for the 92A and LS92, and divide-by-eight for the 93A, L93, and LS93.

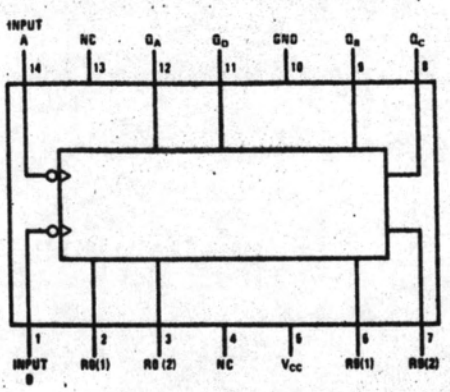
All of these counters have a gated zero reset and the 90A, L90, and LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the 90A, L90, or LS90 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

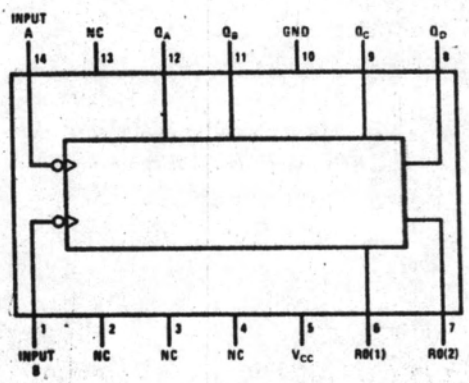
Features

TYPE	TYPICAL POWER DISSIPATION	COUNT FREQUENCY
90A	145 mW	42 MHz
L90	20 mW	11 MHz
LS90	45 mW	42 MHz
92A, 93A	130 mW	42 MHz
LS92, LS93	45 mW	42 MHz
L93	16 mW	15 MHz

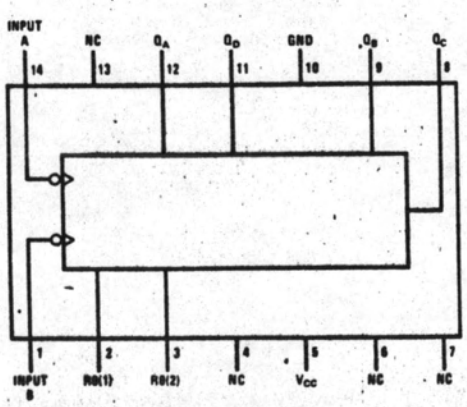
Connection Diagrams



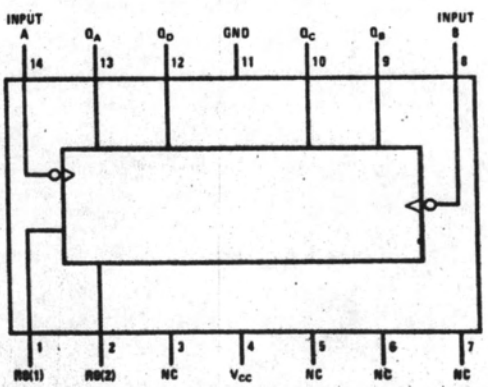
5490A/7490A(J), (N), (W);
54L90/74L90(J), (N), (W);
54LS90/74LS90(J), (N), (W)



5492A/7492A(J), (N), (W);
54LS92/74LS92(J), (N), (W)



5493A/7493A(J), (N), (W);
54LS93/74LS93(J), (N), (W)



54L93/74L93(J), (N), (W)

Truth Tables

90A, L90, LS90
BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

90A, L90, LS90
BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

92A, LS92
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

93A, L93, LS93
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

90A, L90, LS90
RESET/COUNT TRUTH TABLE

RESET INPUTS				OUTPUT			
R0(1)	R0(2)	R9(1)	R9(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

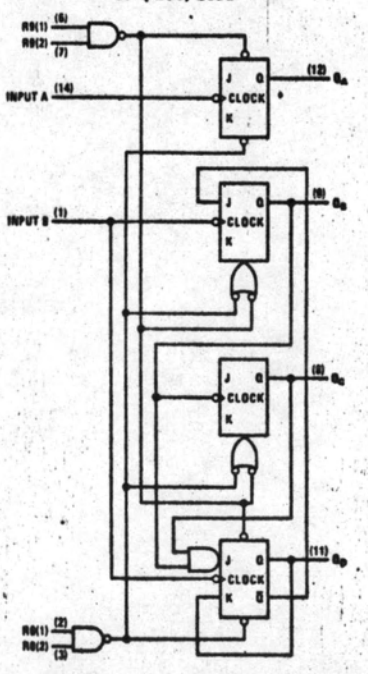
92A, LS92, 93A, L93, LS93
RESET/COUNT TRUTH TABLE

RESET INPUTS		OUTPUT			
R0(1)	R0(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

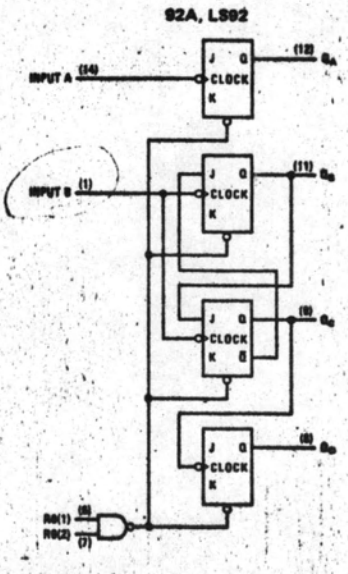
Notes:
(A) Output Q_A is connected to input B for BCD count.
(B) Output Q_D is connected to input A for bi-quinary count.
(C) Output Q_A is connected to input B.
(D) H = High Level, L = Low Level, X = Don't Care.

Logic Diagrams

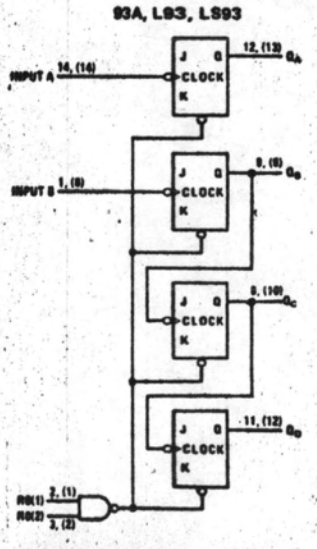
90A, L90, LS90



92A, LS92



93A, L93, LS93



Note: Numbers in parentheses are for L93 only.

The J and K inputs shown without connection are for reference only and are functionally at a high level.

MSI **DM54/DM7496,LS96**

5-Bit Shift Registers

General Description

These shift registers consist of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs for all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may also be performed.

All flip-flops are simultaneously set to a low output level by applying a low-level voltage to the clear input while the preset is low. Clearing is independent of the level of the clock input.

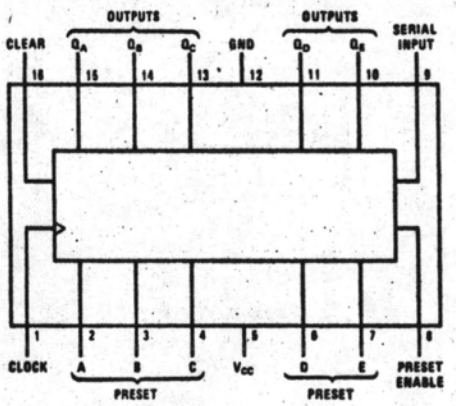
The register may be parallel loaded by using the clear input in conjunction with the preset inputs. After clearing all stages to low output levels, data to be loaded is applied to the individual preset inputs (A, B, C, D, and E) and a high-level load pulse is applied to the preset enable input. Presetting is also independent of the level of the clock input.

Transfer of information to the outputs occurs on the positive-going edge of the clock pulse. The proper information must be set up at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be high and the preset or preset enable inputs must be low when clocking occurs.

Features

- N-bit serial-to-parallel converter
- N-bit parallel-to-serial converter
- N-bit storage register

Connection Diagram



5496(J), (W); 7496(J), (N), (W);
54LS96/74LS96(J), (N), (W)

Truth Table

INPUTS									OUTPUTS				
CLEAR	PRESET ENABLE	PRESET A	B	C	D	E	CLOCK	SERIAL	Q_A	Q_B	Q_C	Q_D	Q_E
L	L	X	X	X	X	X	X	X	L	L	L	L	L
L	X	L	L	L	L	L	X	X	L	L	L	L	L
H	H	H	H	H	H	H	X	X	H	H	H	H	H
H	H	L	L	L	L	L	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	H	H	L	H	L	H	L	X	H	Q_{B0}	H	Q_{D0}	H
H	L	X	X	X	X	X	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	L	X	X	X	X	X	↑	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}
H	L	X	X	X	X	X	↑	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}

H = high level (steady state), L = low level (steady state)
X = don't care (any input, including transitions)
↑ = transition from low to high level
Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc., respectively before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, etc. = the level of Q_A, Q_B, etc., respectively before the most recent ↑ transition of the clock.

MSI **DM54/DM7445,145**

BCD/Decimal Decoders/Drivers

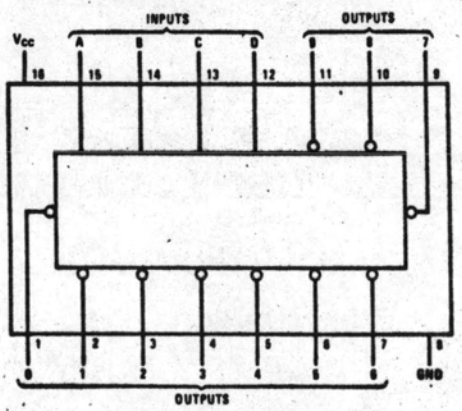
General Description

These BCD-to-decimal decoders/drivers consist of eight inverters and ten, four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of BCD input logic ensures that all outputs remain off for all invalid (10-15) binary input conditions. These decoders feature high-performance, NPN output transistors designed for use as indicator/relay drivers, or as open-collector logic-circuit drivers. The high-breakdown output transistors are compatible for interfacing with most MOS integrated circuits.

Features

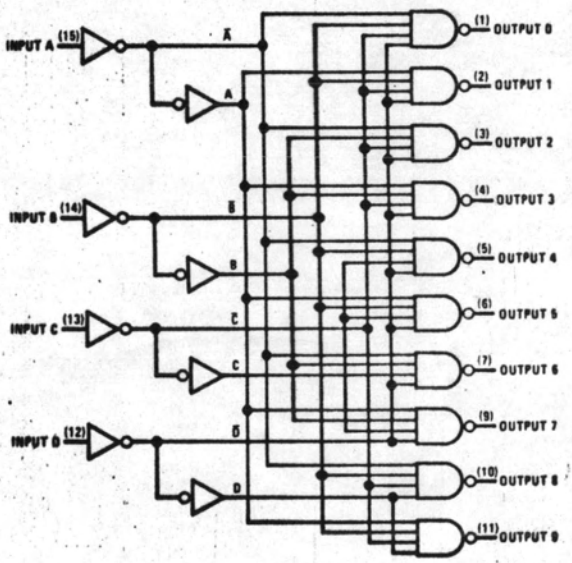
- Full decoding of input logic
- 80 mA sink-current capability
- All outputs are off for invalid BCD input conditions

Connection Diagram



5445(J), (W); 7445(J), (N), (W);
54145(J), (W); 74145(J), (N), (W)

Logic Diagram



Truth Table

NO.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level (Off), L = Low Level (On)

MSI **DM54/DM74150,151A,LS151,S151**

Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain full on-chip decoding to select the desired data source. The 150 selects one-of-sixteen data sources; the 151A, LS151, and S151 select one-of-eight data sources. The 150, 151A, LS151, and S151 have a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high, and the Y output (as applicable) low.

The 151A, LS151, and S151 feature complementary W and Y outputs whereas the 150 has an inverted (W) output only.

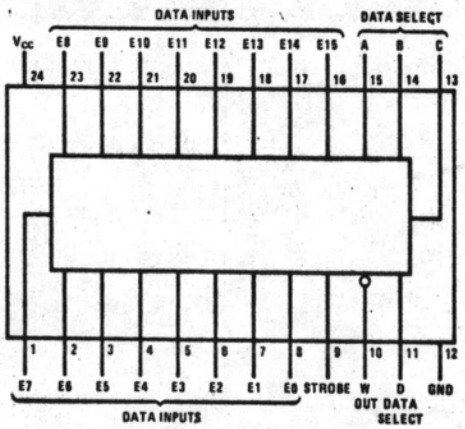
The 151A incorporates address buffers which have symmetrical propagation delay times through the complementary paths. This reduces the possibility of transients occurring at the output(s) due to changes made at the select inputs, even when the 151A outputs are enabled (i.e., strobe low).

Features

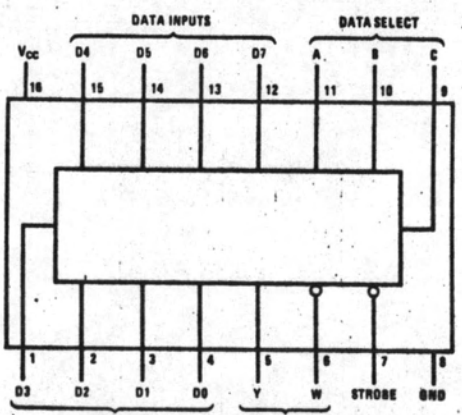
- 150 selects one-of-sixteen data lines
- Others select one-of-eight data lines
- Performs parallel-to-serial conversion
- Permits multiplexing from N lines to one line
- Also for use as Boolean function generator

TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIME DATA INPUT TO W OUTPUT	TYPICAL POWER DISSIPATION
150	11 ns	200 mW
151A	9 ns	135 mW
LS151	12.5 ns	30 mW
S151	4.5 ns	225 mW

Connection Diagrams



54150(J), (F); 74150(J), (N), (F)



54151A(J), (W); 74151A(J), (N), (W);
54LS151/74LS151(J), (N), (W); 74S151(N)

Truth Tables

54150/74150

INPUTS SELECT D	C	B	A	STROBE S	OUTPUT W
X	X	X	X	H	H
L	L	L	L	L	$\overline{E0}$
L	L	L	H	L	$\overline{E1}$
L	L	H	L	L	$\overline{E2}$
L	L	H	H	L	$\overline{E3}$
L	H	L	L	L	$\overline{E4}$
L	H	L	H	L	$\overline{E5}$
L	H	H	L	L	$\overline{E6}$
L	H	H	H	L	$\overline{E7}$
H	L	L	L	L	$\overline{E8}$
H	L	L	H	L	$\overline{E9}$
H	L	H	L	L	$\overline{E10}$
H	L	H	H	L	$\overline{E11}$
H	H	L	L	L	$\overline{E12}$
H	H	L	H	L	$\overline{E13}$
H	H	H	L	L	$\overline{E14}$
H	H	H	H	L	$\overline{E15}$

54151A/74151A, 54LS151/74LS151, 74S151

INPUTS SELECT C	B	A	STROBE S	OUTPUTS Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level, L = Low Level, X = Don't Care
$\overline{E0}$, $\overline{E1}$ . . . $\overline{E15}$ = the complement of the level of the respective E input
D0, D1 . . . D7 = the level of the respective D input

Voltage Regulators

LM309 five-volt regulator

general description

The LM309 is a complete 5V regulator fabricated on a single silicon chip. It is designed for local regulation on digital logic cards, eliminating the distribution problems associated with single-point regulation. The device is available in two common transistor packages. In the solid-kovar TO-5 header, it can deliver output currents in excess of 200 mA, if adequate heat sinking is provided. With the TO-3 power package, the available output current is greater than 1A.

The regulator is essentially blow-out proof. Current limiting is included to limit the peak output current to a safe value. In addition, thermal shutdown is provided to keep the IC from overheating. If internal dissipation becomes too great, the regulator will shut down to prevent excessive heating.

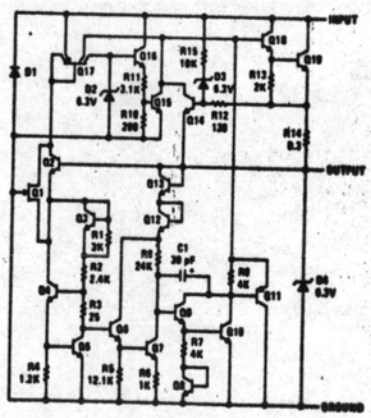
Considerable effort was expended to make the LM309 easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response somewhat. Input bypassing is needed, however, if the regulator is located very far from the filter capacitor of the power supply. Stability is also achieved by methods that provide very good rejection of load or line transients as are usually seen with TTL logic.

Although designed primarily as a fixed-voltage regulator, the output of the LM309 can be set to voltages above 5V, as shown below. It is also possible to use the circuit as the control element in precision regulators, taking advantage of the good current-handling capability and the thermal overload protection.

To summarize, outstanding features of the regulator are:

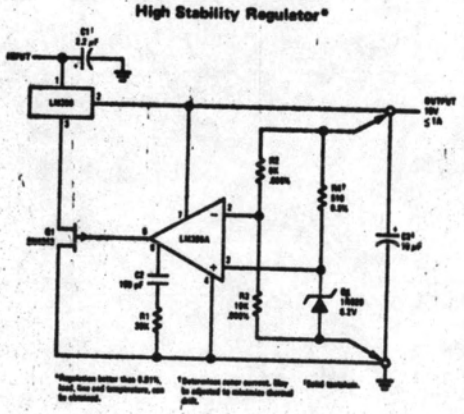
- Specified to be compatible, worst case, with TTL and DTL
- Output current in excess of 1A
- Internal thermal overload protection
- No external components required

schematic diagram



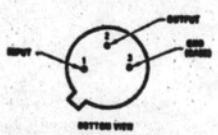
typical application

High Stability Regulator*



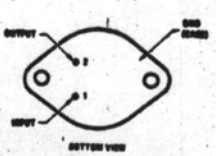
connection diagrams

TO-5 (H)



Order Number LM309H
See Package 9

TO-3 (K)



Order Number LM309K
See Package 18

absolute maximum ratings

Input Voltage	35V
Power Dissipation	Internally Limited
Operating Junction Temperature Range	0°C to 125°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

design characteristics (Note 1)

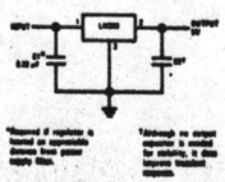
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	$T_j = 25°C$	4.8	5.05	5.2	V
Line Regulation	$T_j = 25°C$ $7V \leq V_{IN} \leq 25V$		4.0	50	mV
Load Regulation LM309H LM309K	$T_j = 25°C$ $5\ mA \leq I_{OUT} \leq 0.5A$ $5\ mA \leq I_{OUT} \leq 1.5A$		20 50	50 100	mV mV
Output Voltage	$7V \leq V_{IN} \leq 25V$ $5\ mA \leq I_{OUT} \leq I_{max}$ $P < P_{max}$	4.75		5.25	V
Quiescent Current	$7V \leq V_{IN} \leq 25V$		5.2	10	mA
Quiescent Current Change	$7V \leq V_{IN} \leq 25V$ $5\ mA \leq I_{OUT} \leq I_{max}$			0.5 0.8	mA mA
Output Noise Voltage	$T_A = 25°C$ $10\ Hz \leq f \leq 100\ kHz$		40		μV
Long Term Stability				20	mV
Thermal Resistance Junction to Case (Note 2) LM309H LM309K			15 3.0		°C/W °C/W

Note 1: Unless otherwise specified, these specifications apply for $0°C \leq T_j \leq 125°C$, $V_{IN} = 10V$ and $I_{OUT} = 0.1A$ for the LM309H or $I_{OUT} = 0.5A$ for the LM309K. For the LM309H, $I_{max} = 0.2A$ and $P_{max} = 2.0W$. For the LM309K, $I_{max} = 1.0A$ and $P_{max} = 20W$.

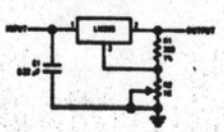
Note 2: Without a heat sink, the thermal resistance of the TO-5 package is about 150°C/W, while that of the TO-3 package is approximately 35°C/W. With a heat sink, the effective thermal resistance can only approach the values specified, depending on the efficiency of the sink.

typical applications(con't)

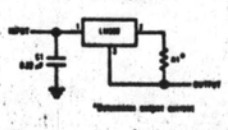
Fixed 5V Regulator



Adjustable Output Regulator



Current Regulator



Voltage Regulators

LM723/LM723C voltage regulator

general description

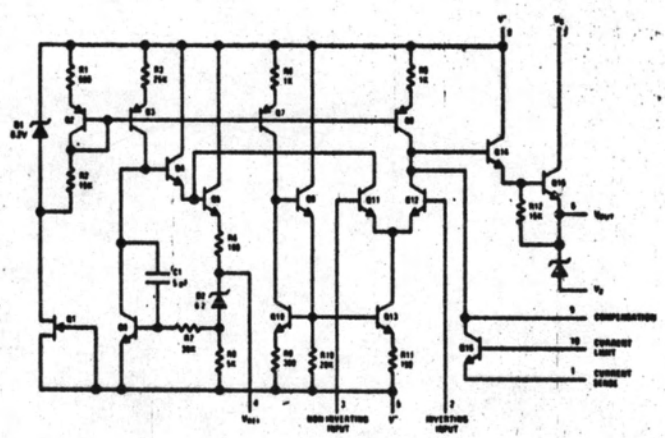
The LM723/LM723C is a voltage regulator designed primarily for series regulator applications. By itself, it will supply output currents up to 150 mA; but external transistors can be added to provide any desired load current. The circuit features extremely low standby current drain, and provision is made for either linear or foldback current limiting. Important characteristics are:

- 150 mA output current without external pass transistor
- Output currents in excess of 10A possible by adding external transistors
- Input voltage 40V max
- Output voltage adjustable from 2V to 37V
- Can be used as either a linear or a switching regulator.

The LM723/LM723C is also useful in a wide range of other applications such as a shunt regulator, a current regulator or a temperature controller.

The LM723C is identical to the LM723 except that the LM723C has its performance guaranteed over a 0°C to 70°C temperature range, instead of −55°C to +125°C.

schematic and connection diagrams*



Dual-In-Line Package

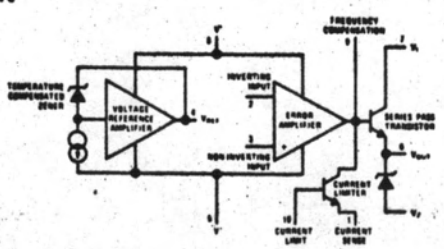
Order Number LM723D or LM723CD
See Package 1

Order Number LM723N or LM723CN
See Package 22

Metal Can Package

Order Number LM723H or LM723CH
See Package 13

equivalent circuit*



* See number for metal can package with Note 7

absolute maximum ratings

Pulse Voltage from V^+ to V^- (50 ms)	50V
Continuous Voltage from V^+ to V^-	40V
Input-Output Voltage Differential	40V
Maximum Amplifier Input Voltage (Either Input)	7.5V
Maximum Amplifier Input Voltage (Differential)	5V
Current from V_Z	25 mA
Current from V_{REF}	15 mA
Internal Power Dissipation Metal Can (Note 1)	800 mW
Cavity DIP (Note 1)	900 mW
Molded DIP (Note 1)	660 mW
Operating Temperature Range LM723	−55°C to +125°C
LM723C	0°C to +70°C
Storage Temperature Range Metal Can	−65°C to +150°C
DIP	−55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	LM723			LM723C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Line Regulation	V_{IN} = 12V to V_{IN} = 15V		.01	0.1		.01	0.1	% V_{OUT}
	−55°C ≤ T_A ≤ +125°C			0.3				% V_{OUT}
	0°C ≤ T_A ≤ +70°C						0.3	% V_{OUT}
	V_{IN} = 12V to V_{IN} = 40V		.02	0.2		0.1	0.5	% V_{OUT}
Load Regulation	I_L = 1 mA to I_L = 50 mA		.03	0.15		.03	0.2	% V_{OUT}
	−55°C ≤ T_A ≤ +125°C			0.6				%V_{OUT}
	0°C ≤ T_A ≤ +70°C						0.6	%V_{OUT}
Ripple Rejection	f = 50 Hz to 10 kHz, C_{REF} = 0		74			74		dB
	f = 50 Hz to 10 kHz, C_{REF} = 5 μF		86			86		dB
Average Temperature Coefficient of Output Voltage	−55°C ≤ T_A ≤ +125°C		.002	.015				%/°C
	0°C ≤ T_A ≤ +70°C					.003	.015	%/°C
Short Circuit Current Limit	R_{SC} = 10Ω, V_{OUT} = 0		65			65		mA
Reference Voltage		6.95	7.15	7.35	6.80	7.15	7.50	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, C_{REF} = 0		20			20		μVrms
	BW = 100 Hz to 10 kHz, C_{REF} = 5 μF		2.5			2.5		μVrms
Long Term Stability			0.1			0.1		%/1000 hrs
Standby Current Drain	I_L = 0, V_{IN} = 30V		1.3	3.5		1.3	4.0	mA
Input Voltage Range		9.5		40	9.5		40	V
Output Voltage Range		2.0		37	2.0		37	V
Input-Output Voltage Differential		3.0		38	3.0		38	V

Note 1: See derating curves for maximum power rating above 25°C.

Note 2: Unless otherwise specified, T_A = 25°C, V_{IN} = V^+ = V_C = 12V, V^- = 0, V_{OUT} = 5V, I_L = 1 mA, R_{SC} = 0, C_1 = 100 pF, C_{REF} = 0 and divider impedance as seen by error amplifier ≤ 10 kΩ connected as shown in Figure 1. Line and load regulation specifications are given for the condition of constant chip temperature. Temperature drifts must be taken into account separately for high dissipation conditions.

Note 3: L_1 is 40 turns of No. 20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009 in. air gap.

Note 4: Figures in parentheses may be used if R1/R2 divider is placed on opposite input of error amp.

Note 5: Replace R1/R2 in figures with divider shown in Figure 13.

Note 6: V^+ must be connected to a +3V or greater supply.

Note 7: For metal can applications where V_Z is required, an external 6.2 volt zener diode should be connected in series with V_{OUT}.

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Operational Amplifiers

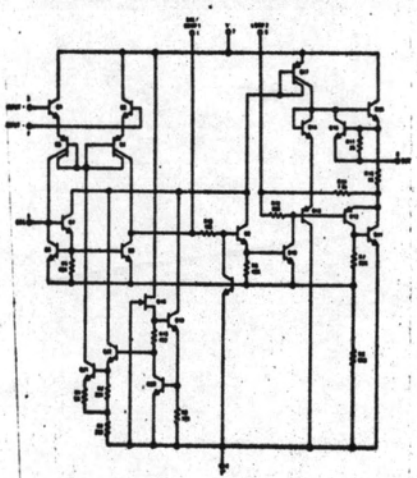
LM301A operational amplifier general description

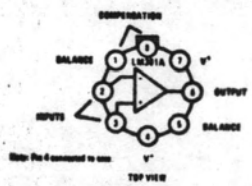
The LM301A is a general-purpose operational amplifier which features improved performance over the 709C and other popular amplifiers. Advanced processing techniques make possible an order of magnitude reduction in input currents, and a redesign of the biasing circuitry reduces the temperature drift of input current.

This amplifier offers many features which make its application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, freedom from oscillations and compensation with a single 30 pF capacitor. It has advantages over internally compensated amplifiers in that the compensation can be tailored to the particular application. For example, as a summing amplifier, slew rates of 10 V/μs and bandwidths of 10 MHz can be realized. In addition, the circuit can be used as a comparator with differential inputs up to ±30V; and the output can be clamped at any desired level to make it compatible with logic circuits.

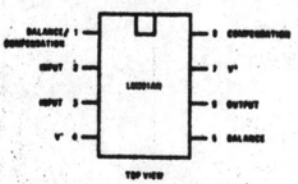
The LM301A provides better accuracy and lower noise than its predecessors in high impedance circuitry. The low input currents also make it particularly well suited for long interval integrators or timers, sample and hold circuits and low frequency waveform generators. Further, replacing circuits where matched transistor pairs buffer the inputs of conventional IC op amps, it can give lower offset voltage and drift at reduced cost.

schematic** and connection diagrams





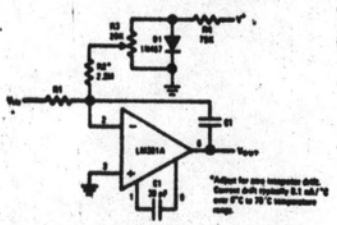
Order Number LM301AH
See Package 11



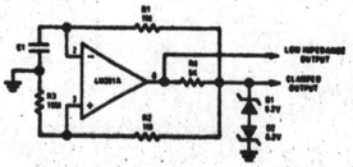
Order Number LM301AN
See Package 20

typical applications **

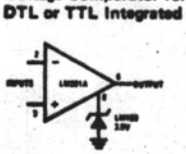
Integrator with Bias Current Compensation



Low Frequency Square Wave Generator



Voltage Comparator for Driving DTL or TTL Integrated Circuits



**Pin connections shown are for metal can.

absolute maximum ratings

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration (Note 3)	Indefinite
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 50\,k\Omega$		2.0	7.5	mV
Input Offset Current	$T_A = 25°C$		3	50	nA
Input Bias Current	$T_A = 25°C$		70	250	nA
Input Resistance	$T_A = 25°C$	0.5	2		MΩ
Supply Current	$T_A = 25°C$, $V_S = \pm 15V$		1.8	3.0	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2\,k\Omega$	25	160		V/mV
Input Offset Voltage	$R_S \leq 50\,k\Omega$			10	mV
Average Temperature Coefficient of Input Offset Voltage			6.0	30	µV/°C
Input Offset Current				70	nA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 70°C$ $0°C \leq T_A \leq 25°C$		0.01 0.02	0.3 0.6	nA/°C nA/°C
Input Bias Current				300	nA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2\,k\Omega$	15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\,k\Omega$ $R_L = 2\,k\Omega$	±12 ±10	±14 ±13		V V
Input Voltage Range	$V_S = \pm 15V$	±12			V
Common Mode Rejection Ratio	$R_S \leq 50\,k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 50\,k\Omega$	70	96		dB

Note 1: For operating at elevated temperatures, the device must be derated based on a 100°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Continuous short circuit is allowed for case temperatures to 70°C and ambient temperatures to 55°C.

Note 4: These specifications apply for $0°C \leq T_A < 70°C$, $\pm 5V \leq V_S \leq \pm 15V$ and C1 = 30 pF unless otherwise specified.

Operational Amplifiers

LM308 operational amplifier

general description

The LM308 is a precision operational amplifier featuring input currents nearly a thousand times lower than industry standards like the LM709C. In fact, its performance approaches that of high quality FET amplifiers. The circuit is directly interchangeable with the LM301A in low frequency circuits and incorporates the same protective features which make its application nearly foolproof.

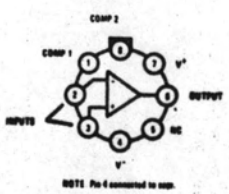
The device operates with supply voltages from ±2V to ±15V and has sufficient supply rejection to use unregulated supplies. Although the circuit is designed to work with the standard compensation for the LM301A, an alternate compensation scheme can be used to make it particularly insensitive to power supply noise and to make supply bypass capacitors unnecessary. Power consumption is extremely low, so the amplifiers are ideally suited for battery powered applications. Outstanding characteristics include:

- Maximum input bias current of 7.0 nA
- Offset current less than 1.0 nA
- Supply current of only 300 μA, even in saturation
- Guaranteed drift characteristics

The low current error of the LM308 makes possible many designs that are not practical with conventional amplifiers. In fact, it operates from 10 MΩ source resistances, introducing less error than devices like the 709C with 10 kΩ sources. Integrators with worst case drifts less than 1 mV/sec and analog time delays in excess of one hour can be made using capacitors no larger than 1 μF. The device is well suited for use with piezoelectric, electrostatic or other capacitive transducers, in addition to low frequency active filters with small capacitor values.

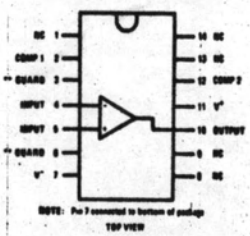
connection diagrams*

Metal Can Package



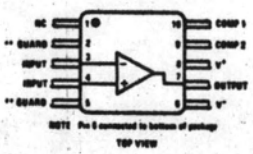
Order Number LM308H
See Package 11

Dual-In-Line Package



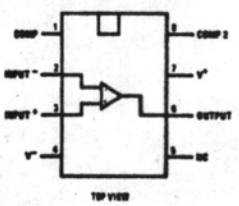
Order Number LM308D
See Package 1

Flat Package



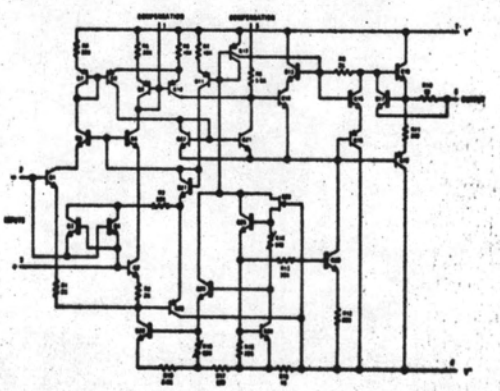
Order Number LM308F
See Package 3

Dual-In-Line Package

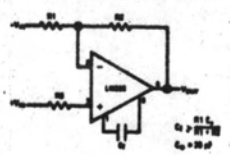


Order Number LM308N
See Package 20.

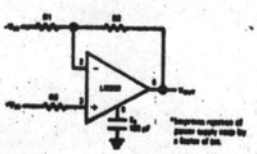
schematic diagram* and compensation circuits



Standard Compensation Circuit



Alternate* Frequency Compensation



absolute maximum ratings

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$T_A = 25°C$		2.0	7.5	mV
Input Offset Current	$T_A = 25°C$		0.2	1	nA
Input Bias Current	$T_A = 25°C$		1.5	7	nA
Input Resistance	$T_A = 25°C$	10	40		MΩ
Supply Current	$T_A = 25°C$, $V_S = ±15V$		0.3	0.8	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = ±15V$ $V_{OUT} = ±10V$, $R_L \geq 10\ k\Omega$	25	300		V/mV
Input Offset Voltage				10	mV
Average Temperature Coefficient of Input Offset Voltage			6.0	30	µV/°C
Input Offset Current				1.5	nA
Average Temperature Coefficient of Input Offset Current			2.0	10	pA/°C
Input Bias Current				10	nA
Large Signal Voltage Gain	$V_S = ±15V$, $V_{OUT} = ±10V$ $R_L \geq 10\ k\Omega$	15			V/mV
Output Voltage Swing	$V_S = ±15V$, $R_L = 10\ k\Omega$	±13	±14		V
Input Voltage Range	$V_S = ±15V$	±14			V
Common Mode Rejection Ratio		80	100		dB
Supply Voltage Rejection Ratio		80	96		dB

Note 1: The maximum junction temperature of the LM308 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten, 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $±5V \leq V_S \leq ±15V$ and $0°C \leq T_A \leq 70°C$, unless otherwise specified.

Operational Amplifiers

LM741/LM741C operational amplifier

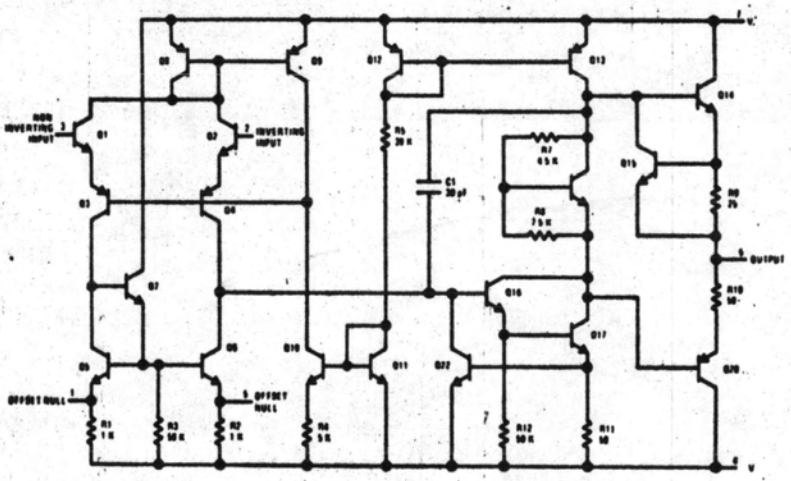
general description

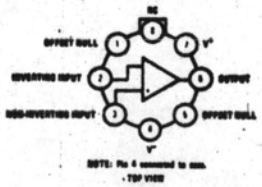
The LM741 and LM741C are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

The offset voltage and offset current are guaranteed over the entire common mode range. The amplifiers also offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

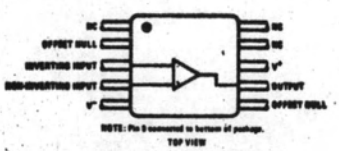
The LM741C is identical to the LM741 except that the LM741C has its performance guaranteed over a 0°C to 70°C temperature range, instead of −55°C to 125°C.

schematic and connection diagrams

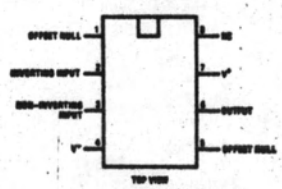




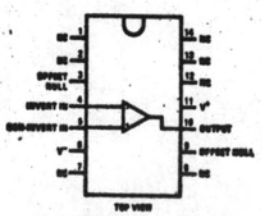
Order Number LM741H or LM741CH
See Package 11



Order Number LM741F
See Package 3



Order Number LM741CN
See Package 20



Order Number
LM741CD or LM741CN-14
See Package 1 See Package 22

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absolute maximum ratings

Supply Voltage	LM741	±22V
	LM741C	±18V
Power Dissipation (Note 1)		500 mW
Differential Input Voltage		±30V
Input Voltage (Note 2)		±15V
Output Short-Circuit Duration		Indefinite
Operating Temperature Range	LM741	-55°C to 125°C
	LM741C	0°C to 70°C
Storage Temperature Range		-65°C to 150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 3)

PARAMETER	CONDITIONS	LM741			LM741C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 10\ k\Omega$		1.0	5.0		1.0	6.0	mV
Input Offset Current	$T_A = 25°C$		30	200		30	200	nA
Input Bias Current	$T_A = 25°C$		200	500		200	500	nA
Input Resistance	$T_A = 25°C$	0.3	1.0		0.3	1.0		MΩ
Supply Current	$T_A = 25°C$, $V_S = ±15V$		1.7	2.8		1.7	2.8	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = ±15V$ $V_{OUT} = ±10V$, $R_L \geq 2\ k\Omega$	50	160		25	160		V/mV
Input Offset Voltage	$R_S \leq 10\ k\Omega$			6.0			7.5	mV
Input Offset Current				500			300	nA
Input Bias Current				1.5			0.8	μA
Large Signal Voltage Gain	$V_S = ±15V$, $V_{OUT} = ±10V$ $R_L \geq 2\ k\Omega$	25			15			V/mV
Output Voltage Swing	$V_S = ±15V$, $R_L = 10\ k\Omega$	±12	±14		±12	±14		V
	$R_L = 2\ k\Omega$	±10	±13		±10	±13		V
Input Voltage Range	$V_S = ±15V$	±12			±12			V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	77	96		77	96		dB

Note 1: The maximum junction temperature of the LM741 is 150°C, while that of the LM741C is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to case.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $V_S = ±15V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified. With the LM741C, however, all specifications are limited to $0°C \leq T_A \leq 70°C$ and $V_S = ±15V$.

Voltage Comparators/Buffers

LM311 voltage comparator

general description

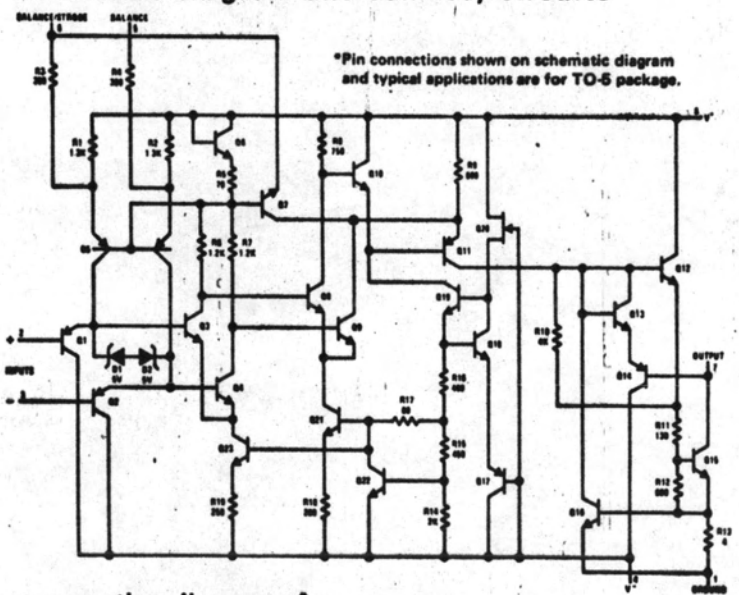
The LM311 is a voltage comparator that has input currents more than a hundred times lower than devices like the LM306 or LM710C. It is also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Its output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, it can drive lamps or relays, switching voltages up to 40V at currents as high as 50 mA.

features

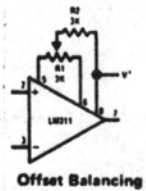
- Operates from single 5V supply
- Maximum input current: 250 nA
- Maximum offset current: 50 nA
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V

Both the input and the output of the LM311 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM306 and LM710C (200 ns response time vs 40 ns) the device is also much less prone to spurious oscillations. The LM311 has the same pin configuration as the LM306 and LM710C.

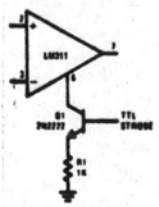
schematic diagram and auxiliary circuits



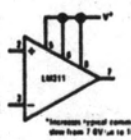
*Pin connections shown on schematic diagram and typical applications are for TO-5 package.



Offset Balancing



Strobing



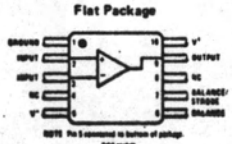
Increasing Input Stage Current*

connection diagrams *

Metal Can

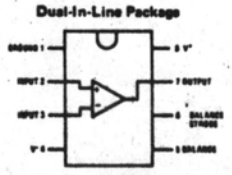
Order Number LM311H
See Package 11

Flat Package



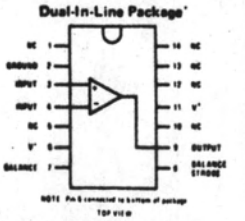
Order Number LM311F
See Package 3

Dual-In-Line Package



Order Number LM311N
See Package 20

Dual-In-Line Package



Order Number LM311D
See Package 1 or
Order Number LM311N-14
See Package 22

absolute maximum ratings

Total Supply Voltage (V_{84})	36V
Output to Negative Supply Voltage (V_{74})	40V
Ground to Negative Supply Voltage (V_{14})	30V
Differential Input Voltage	±30V
Input Voltage (Note 1)	±15V
Power Dissipation (Note 2)	500 mW
Output Short Circuit Duration	10 sec
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (soldering, 10 sec)	300°C

electrical characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50K$		2.0	7.5	mV
Input Offset Current (Note 4)	$T_A = 25°C$		6.0	50	nA
Input Bias Current	$T_A = 25°C$		100	250	nA
Voltage Gain	$T_A = 25°C$		200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200		ns
Saturation Voltage	$V_{IN} \leq -10$ mV, $I_{OUT} = 50$ mA, $T_A = 25°C$		0.75	1.5	V
Strobe On Current	$T_A = 25°C$		3.0		mA
Output Leakage Current	$V_{IN} \geq 10$ mV, $V_{OUT} = 35V$, $T_A = 25°C$		0.2	50	nA
Input Offset Voltage (Note 4)	$R_S \leq 50K$			10	mV
Input Offset Current (Note 4)				70	nA
Input Bias Current				300	nA
Input Voltage Range			±14		V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$, $V_{IN} \leq -10$ mV, $I_{SINK} \leq 8$ mA		0.23	0.4	V
Positive Supply Current	$T_A = 25°C$		5.1	7.5	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0	mA

Note 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LM311 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten, 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$ and $0°C < T_A < 70°C$, unless otherwise specified. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Voltage Comparators/Buffers

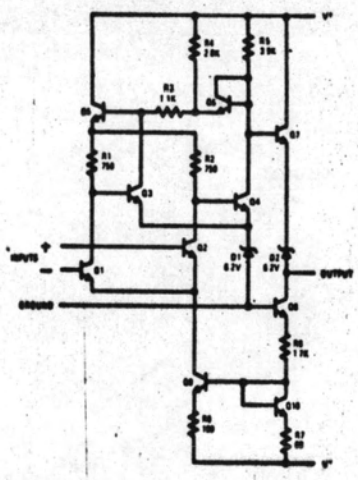
LM710 voltage comparator general description

The LM710 is a high-speed voltage comparator intended for use as an accurate, low-level digital level sensor or as a replacement for operational amplifiers in comparator applications where speed is of prime importance. The circuit has a differential input and a single-ended output, with saturated output levels compatible with practically all types of integrated logic.

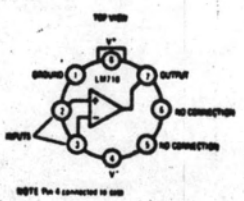
The device is built on a single silicon chip which insures low offset and thermal drift. The use of a minimum number of stages along with minority-carrier lifetime control (gold doping) makes the circuit much faster than operational amplifiers in saturating comparator applications. In fact, the low stray and wiring capacitances that can be realized with monolithic construction make the device difficult to duplicate with discrete components operating at equivalent power levels.

The LM710 is useful as a pulse height discriminator, a voltage comparator in high-speed A/D converters or a go, no-go detector in automatic test equipment. It also has applications in digital systems as an adjustable-threshold line receiver or an interface between logic types. In addition, the low cost of the unit suggests it for applications replacing relatively simple discrete component circuitry.

schematic* and connection diagrams



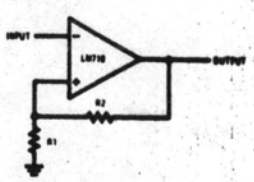
Metal Can



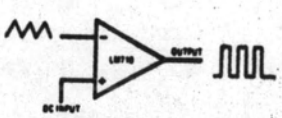
Order Number LM710H
See Package 11

typical applications*

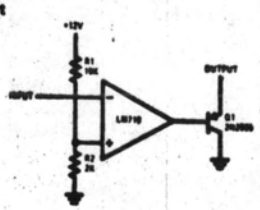
Schmidt Trigger



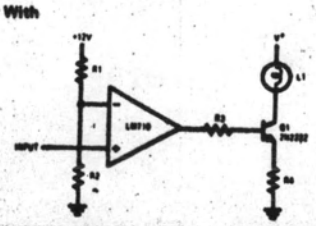
Pulse Width Modulator



Line Receiver With Increased Output Sink Current



Level Detector With Lamp Driver



*Pin connections shown are for metal can.

absolute maximum ratings

Positive Supply Voltage	14.0V
Negative Supply Voltage	−7.0V
Peak Output Current	10 mA
Differential Input Voltage	±5.0V
Input Voltage	±7.0V
Power Dissipation	
TO-99 (Note 1)	300 mW
Flat Package (Note 2)	200 mW
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 3)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 200\Omega$ $V_{CM} = 0V$		0.6	2.0	mV
Input Offset Current	$T_A = 25°C$, $V_{OUT} = 1.4V$		0.75	3.0	μA
Input Bias Current	$T_A = 25°C$		13	20	μA
Voltage Gain	$T_A = 25°C$	1250	1700		
Output Resistance	$T_A = 25°C$		200		Ω
Output Sink Current	$T_A = 25°C$, $V_{IN} \leq -5$ mV $V_{OUT} = 0$	2.0	2.5		mA
Response Time (Note 4)	$T_A = 25°C$		40		ns
Input Offset Voltage	$R_S \leq 200\Omega$, $V_{CM} = 0V$			3.0	mV
Average Temperature Coefficient of Input Offset Voltage	$-55°C \leq T_A \leq 125°C$ $R_S \leq 50\Omega$		3.0	10	μV/°C
Input Offset Current	$T_A = 125°C$		0.25	3.0	μA
	$T_A = -55°C$		1.8	7.0	μA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 125°C$		5.0	25	nA/°C
	$-55°C \leq T_A \leq 25°C$		15	75	nA/°C
Input Bias Current	$T_A = -55°C$		27	48	μA
Input Voltage Range	$V^- = -7.0V$	±5.0			V
Common Mode Rejection Ratio	$R_S \leq 200\Omega$	80	100		dB
Differential Input Voltage Range		±5.0V			V
Voltage Gain		1000			
Positive Output Level	$V_{IN} \geq 5$ mV, $0 \leq I_{OUT} \leq -5$ mA	2.5	3.2	4.0	V
Negative Output Level	$V_{IN} \leq -5$ mV	−1.0	−0.5	0	V
Output Sink Current	$T_A = 125°C$, $V_{IN} \leq -5$ mV $V_{OUT} = 0V$	0.5	1.7		mA
	$T_A = -55°C$, $V_{IN} \leq -5$ mV $V_{OUT} = 0$	1.0	2.3		mA
Positive Supply Current	$V_{IN} \leq -5$ mV		5.2	9.0	mA
Negative Supply Current			4.6	7.0	mA
Power Consumption	$V_{IN} \leq -5$ mV $I_{OUT} = 0$ mA		90	150	mW

Note 1: Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +105°C.

Note 2: Derate linearly at 4.4 mW/°C for ambient temperatures above +100°C.

Note 3: These specifications apply for $V^+ = 12.0V$, $V^- = -6.0V$, $-55°C \leq T_A \leq +125°C$ unless otherwise specified. The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.8V at −55°C, 1.4V at +25°C, and 1.0V at +125°C.

Note 4: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Functional Blocks

LM555/LM555C timer

general description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits.

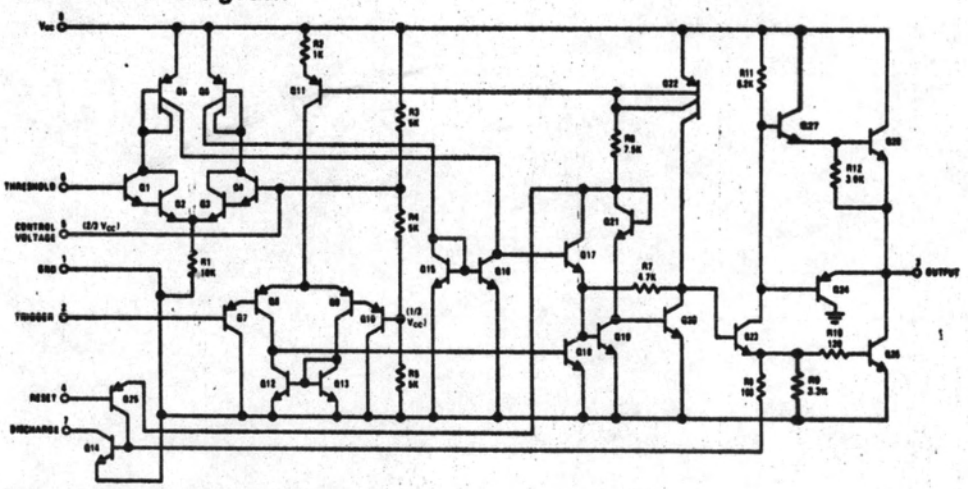
features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200mA
- Output and supply TTL compatible
- Temperature stability better than .005% per °C
- Normally on and normally off output

applications

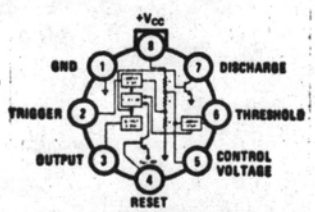
- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

schematic diagram



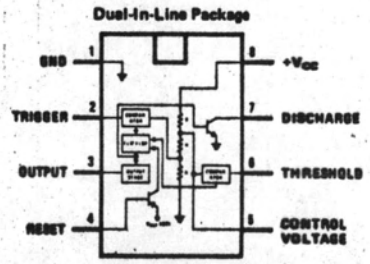
connection diagrams

Metal Can Package



TOP VIEW
Order Number LM555H or LM555CH
See Package 11

Dual-In-Line Package



TOP VIEW
Order Number LM555CN
See Package 20

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absolute maximum ratings

Supply Voltage	+18V
Power Dissipation	600 mW
Operating Temperature Ranges	
LM555C	0°C to +70°C
LM555	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (T_A = 25°C, V_{CC} = +5V to +15V unless otherwise specified)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LM555			LM555C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞		3	5		3	6	mA
	V_{CC} = 15V, R_L = ∞ (Low State) (Note 1)		10	12		10	15	mA
Timing Error, Monostable								
Initial Accuracy	R_A, R_B = 1k to 100k, C = .1μF, (Note 2)		.5	2		1		%
Drift with Temperature			30	100		50		ppm/°C
Drift with Supply			.005	.02		.01		%/V
Threshold Voltage			.667			.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V	4.8	5	5.2		5		V
	V_{CC} = 5V	1.45	1.67	1.9		1.67		V
Trigger Current			.5			.5		μA
Reset Voltage		.4	.7	1	.4	.7	1	V
Reset Current			.1			.1		mA
Threshold Current	(Note 3)		.1	.25		.1	.25	μA
Control Voltage Level	V_{CC} = 15V	9.6	10	10.4	9	10	11	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Output Voltage Drop (Low)	V_{CC} = 15V							
	I_{SINK} = 10 mA		.1	.15		.1	.25	V
	I_{SINK} = 50 mA		.4	.5		.4	.75	V
	I_{SINK} = 100 mA		2	2.2		2	2.5	V
	I_{SINK} = 200 mA		2.5			2.5		V
	V_{CC} = 5V							
	I_{SINK} = 8 mA		.1	.25				V
	I_{SINK} = 5 mA					.25	.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200 mA							
	V_{CC} = 15V		12.5			12.5		V
	I_{SOURCE} = 100 mA							
	V_{CC} = 15V	13	13.3		12.75	13.3		V
	V_{CC} = 5V	3	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns

Note 1: Supply current when output high typically 1 mA less at V_{CC} = 5V.
Note 2: Tested at V_{CC} = 5V and V_{CC} = 15V.
Note 3: This will determine the maximum value of $R_A + R_B$ for 15V operation. The max total ($R_A + R_B$) = 20 MΩ.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Vdd Supply Voltage*	-20v to +0.3v
Data Input Voltage*	-30v to +0.3v
Operating Temperature Range	$0^{\circ}C$ to $+70^{\circ}C$
Storage Temperature Range	$-55^{\circ}C$ to $+150^{\circ}C$

* Referenced to Vss.

D.C. Characteristics

Parameter	Symbol	Minimum	Typ.	Maximum	Units	Conditions
Segment Output High	V_{SH}	Vdd+2.5			V	I_{SH} = 10M
Segment Output Low	V_{SL}			Vdd+1.0	V	Note 1
Digit Output High	V_{DH}	Vss-1.0			V	I_{DH} = 2MA
Digit Output Low	V_{DL}			Vdd_1.0		Note 1
Segment Output High	V_{SH}	Vss-2.0			V	I_{SH} = 3MA
Segment Output Low	V_{SL}	Vss-30		Vc+1	V	Note 2
Digit Output High	V_{DH}	Vss-2.0			V	I_{DH} = 6MA
Digit Output Low	V_{DL}	Vss-30		V_{Grid}+1	V	Note 2
Keyboard Input High	Y_H	Vss-3.0		Vss	V	
Keyboard Input Low	Y_L			Vdd+1.0	V	
Vss Supply	Vss	0	0	0	V	
Vdd Supply	Vdd	-6	-7.5	-9.5	V	

MPS 7529

MECHANICAL CHARACTERISTICS

Package

The MPS 7529 Calculator Array is supplied in a 28 pin dual-in-line plastic package. Package dimensions and tolerances are detailed in Figure 5.

Pin Connections

Pin	Function	Pin	Function
1	S_D	15	D_{10}
2	S_C	16	D_{11}
3	S_B	17	D_{12}
4	S_A	18	Y_1
5	V_{DD}	19	Y_2
6	D_1	20	Y_3
7	D_2	21	Y_4
8	D_3	22	Slide Switch
9	D_4	23	Low voltage Idicator
10	D_5	24	S_P
11	D_6	25	S_G
12	D_7	26	S_F
13	D_8	27	S_E
14	D_9	28	V_{SS}

KEYBOARD SCHEMATIC

	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12
Y1	x 0	ln 1	log 2	$\sqrt{x}$ 3	e^x 4	10^x 5	y^x 6	Sin 7	Cox 8	Tan 9	CF F	x^2 +/-
Y2	(.	m+ +	Rcl -	Sto x	ARC -	1/x c/ce	) =	C. N. eex				

ประวัติผู้ทำการวิจัย

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