9 APPENDIX

9.1 Pole-Zero Cancellation

Pole-zero cancellation is a method for eliminating pulse undershoot after the first differentiating network. The technique employed is described by referring to the waveforms and equations shown in Fig. 9.1 and 9.2. In an amplifier without pole-zero cancellation the exponential tail on the preamplifier output signal (usually 50 to 500-μs) causes an undershoot whose peak amplitude is roughly.

$$\frac{\text{undershoot amplitude}}{\text{differentiated pulse amplitude}} = \frac{\text{differentiation time}}{\text{preamplifier pulse decay time}}$$

For a 1-μs differentiation time and a 50-μs preamplifier pulse decay time, the maximum undershoot is 2 % and decays with a 50-μs time constant. Under overload conditions this undershoot is often sufficiently large to saturate the amplifier during a considerable portion of the undershoot, causing excessive dead time. This effect can be reduced by increasing the preamplifier pulse decay time (which generally reduces the counting rate capabilities of the preamplifier) or compensating for the undershoot by using pole-zero cancellation.
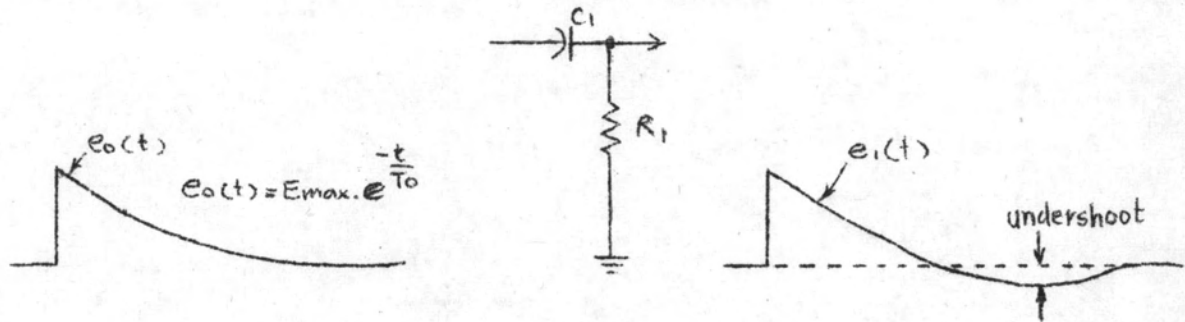
Fig. 9.1 Clipping in an Amplifier Without

Pole-Zero Cancellation.

Charge loop output X First clipping network

= Clipped pulse with undershoot.

Equations :

$$Emax \cdot e^{\frac{-t}{T_o}} \quad X \quad G(t) \quad = \quad e_1(t)$$

Laplace Transform :

$$Emax \cdot \frac{1}{s + \frac{1}{T_o}} \quad X \quad \frac{s}{s + \frac{1}{R_1 C_1}}$$

$$= \quad E_1(s)$$

$$\frac{Emax}{T_o - T_1}\left[T_o \, e^{\frac{-t}{T_1}} - T_1 \, e^{\frac{-t}{T_o}} \right] = \quad e_1(t)$$

where $\qquad T_1 \quad = \quad R_1 C_1$

$0 \leq k \leq 1$

$e_0(t) = E_{max}. e^{\frac{-t}{T_0}}$

C_1

R_2
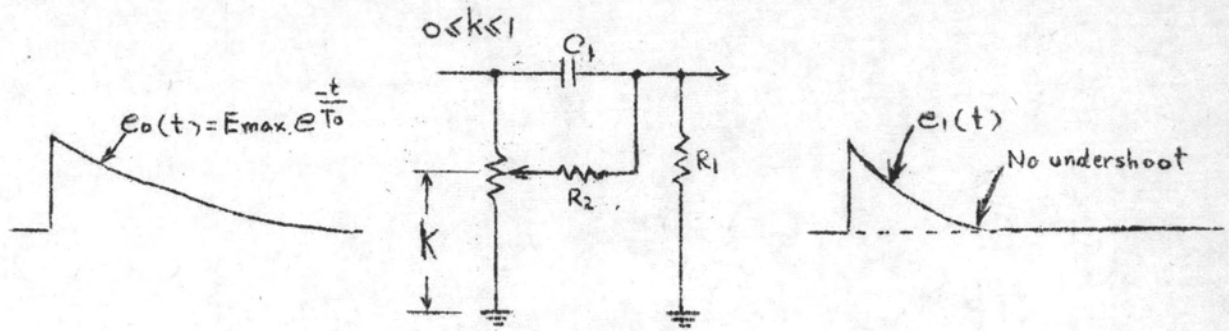
R_1

K

$e_1(t)$

No undershoot

Fig. 9.2 Differentiation (Clipping) in a Pole-Zero-Cancelled

Amplifier.

Charge loop output X **pole**-zero cancelled clipping

network = Clipped pulse without undershoot.

$$E_{max}.e^{\frac{-t}{T_0}} \; X \; G(t) \qquad = \qquad e_1(t)$$

Laplace Transform :

$$E_{max} \; \frac{1}{s + \frac{1}{T_0}} \quad X \quad \frac{s + \frac{k}{R_2 C_1}}{s + \frac{R_1 + R_2}{R_1 R_2 C_1}} \qquad = \quad E_1(s)$$

Pole zero cancel by letting $\quad s + \frac{1}{T_0} \; = \; s + \frac{k}{R_2 C_1}$

or

$$\frac{E_{max}}{s + \frac{R_1 + R_2}{R_1 R_2 C_1}} \qquad = \qquad \frac{E_{max}}{s + \frac{1}{R_p C_1}} \qquad = \; E_1(s)$$

where $R_p = \dfrac{R_1 R_2}{R_1 + R_2}$

$\therefore$ $E_{max}\ e^{\frac{-t}{R_p C_1}} = e_1(t)$

The pole $\left[1/s + (1/T_o) \right]$ due to the preamplifier pulse decay time is cancelled by the zero $\left[s + (k/R_2 C_1) \right]$ of the network. In effect, the d.c. path across the differentiation capacitor adds an attenuated replica of the preamplifier pulse to just cancel the negative undershoot of the clipping network.

Total preamplifier-amplifier pole-zero cancellation requires that the preamplifier output pulse decay time be a single exponential decay and matched to the pole-zero concellation network.

Improper matching of the pole-zero cancellation network will degrade the overload performance and cause excessive pileup distortion at medium counting rates. Improper matching causes either an undercompensation (undershoot is not eliminated) or an overcompensation (output after the main pulse does not return to the baseline and decays to the baseline with the preamplifier time constant).

9.2 UP/DOWN Portable Scaler Circuits Analysis and Synthesis

9.2.1 Preamplifier-Amplifier & Discriminator (See Fig. 3.1)

9.2.1.1 Preamplifier

Choose the supply voltage of 5 V

Let V_{E2} = 2.4 V

and $I_{E2} \cong I_{C2}$ = 1.4 mA

If R18 = 100 Ω, voltage drop across R18 is about

$$V_{R18} \cong 1.4 \times 10^{-3} \times 100$$

$$= 0.14 \text{ V}$$

Voltage drop across R6

$$V_{R6} = 5 - 0.14 - 2.4$$

$$= 2.46 \text{ V}$$

$$\therefore R6 = \frac{2.46}{1.4 \times 10^{-3}}$$

$$= 1.76 \text{ k}\Omega$$

Use R6 = 1.8 kΩ

$$\therefore V_{BE2} \cong 0.6 \text{ V}$$

$$\therefore V_{B2} = 2.4 - 0.6$$

$$= 1.8 \text{ V}$$

If R5 = 100 kΩ

$$\therefore I_{R5} = \frac{0.6}{100 \times 10^{3}}$$

$$= 6 \text{ }\mu\text{A}$$

which is very small compared with emitter current of Q2

$$\therefore \quad V_{BE1} \cong 0.6 \quad V$$

$$\therefore \quad V_{B1} = 1.8 - 0.6$$

$$= 1.2 \quad V$$

Use Transistors 2N 3906 which have $h_{FE} = 100$

$$\therefore \quad I_{B2} = \frac{1.4 \times 10^{-3}}{100}$$

$$= 14 \quad \mu A$$

$$\therefore \quad I_{E1} = I_{B2} + I_{R5}$$

$$= 14 + 6$$

$$= 20 \quad \mu A$$

$$I_{B1} = \frac{20 \times 10^{-6}}{100}$$

$$= 0.2 \quad \mu A$$

Let V_{R4} be 1.18 V

$$\therefore \quad R3 = \frac{1.2 - 1.18}{0.2 \times 10^{-6}}$$

$$= 100 \quad k\Omega$$

If R4 = 18 kΩ,

$$\therefore \quad \frac{R2}{R4} = \frac{5 - 0.14 - 1.18}{1.18}$$

$$\therefore \quad R2 = \frac{3.68 \times 18}{1.18} \quad k\Omega$$

$$= 56.2 \quad k\Omega$$

Use $\quad R2 = 56 \quad k\Omega$

9.2.1.2 <u>Amplifier</u>

For first stage fixed gain amplifier, the closed loop gain is calculated by using (1.14)

$$A_F \cong -\frac{R_F}{R_1} \qquad (1.14)$$

$$\therefore A_{F1} \cong -\frac{R14}{R10}$$

$$= -\frac{5.1 \times 10^3}{255}$$

$$= -20$$

For the other stage variable gain amplifier, the maximum gain is achieved from 162 Ω input resistor.

$$\therefore A_{F2} (max) \cong -\frac{R24}{162}$$

$$= -\frac{5.1 \times 10^3}{162}$$

$$= -31.5$$

$\therefore$ The maximum total gain of the main amplifier

$$= A_{F1} \cdot A_{F2} (max)$$

$$= -20 \times -31.5$$

$$= 630$$

9.2.2 <u>Timer & Gate</u> (see Fig 3.2)

Two 4-bit binary counters are used to scale down the period of the clock pulse.

$$\therefore \text{Scaling factor} = 2^8$$

$$= 256$$

For 0.1 min interval of pulses applied to the gate and thumb-wheel switch, the pulses generated by the relaxation oscillator must have period

$$T = \frac{6}{256}$$

$$= 23.43 \quad ms$$

∴ The period of pulses generated by the relaxation oscillator is calculated from the RC time constant

$$T \cong R_1.C_1. \ln \frac{1}{1-\eta}$$

For Unijunction Transistor 2N 1674 A

$$\eta = 0.5 \quad (average)$$

If we choose C_1 to be 10 μf

$$\therefore 23.43 \times 10^{-3} \cong (R_1 \times 10 \times 10^{-6}) \ln \frac{1}{1-0.5}$$

$$R_1 \cong \frac{23.43 \times 10^{-3}}{(10 \times 10^{-6}) \ln 2}$$

$$= 3.38 \quad k\Omega$$

Choose 5kΩ ten-turns trimmer resistor for the purpose that clock rate can be adjusted.

9.2.3 H.V. Supply & 5V regulated power supply (See Fig. 3.4)

9.2.3.1 5V regulated power supply

Transistor Q3 2N 1484 is used as the series regulator type to supply 5V regulated output.

∴ The voltage drop between base and emitter of transistor Q3 is about 0.6 V

∴ Use 1N 4734 A Zener diode which has reference voltage of 5.6 V and maximum power dissipation of 1W.

$$V_{out} = V_z (D4) + V_{EB} (Q3)$$
$$= 5.6 - 0.6$$
$$= 5 \ V$$

∴ Maximum current rating of D4

$$= \frac{1}{5.6}$$
$$= 0.18 \ A$$

At no load, let the current passing through R5 be

$$I_{R5} = 0.9 \ X \ 0.18$$
$$= 0.162 \ A$$
$$\therefore R5 = \frac{12 - 5.6}{0.162}$$
$$= 39.5 \ \Omega$$

Use 40 Ω

∴ maximum power dissipation in R5

$$= \frac{(12 - 5.6)^2}{40}$$
$$= \frac{(6.4)^2}{40}$$
$$= 1.025 \ W$$

$\therefore$ Use 40 Ω 2W resistor as R5

If sustaining current of zener diode voltage = 0.1 maximum current

$\therefore$ sustaining current $= 0.1 \times 0.18$

$= 0.018$ A

$\therefore$ maximum current I_E (max) that the regulator can supply to the load,

$= I_B \times h_{FE}$(average) of Q3

$= (0.162 - 0.018) \times 20$

$= 2.88$ A