3 CIRCUIT OPERATION

3.1 Preamplifier, Main Amplifier and Discriminator (Fig. 3.1)

General : The function of the preamplifier is to match the high output impedance of the detector to the low impedance of the main amplifier. The amplifier and discriminator circuit provides signal amplification and discrimination for the timer and gate circuit.

Operation

3.1.1 The preamplifier circuit : The preamplifier, which has a gain of unity, consists of two transistors Q1 and Q2 connected in compound emitter follower. Signal input pulse from detector is fed through C1 to the base of input transistor Q1 where the input impedance is approximately equal to 100 kΩ. The output signal which has a decay time constant of 100 μs is taken from the emitter of Q2. The signal is then coupled to the main amplifier through the differentiator with pole-zero cancellation network to reduce overshoot which may be sufficiently large to saturate the amplifier during a considerable portion of the overshoot, causing excessive dead time.

3.1.2 The main amplifier circuit : The amplifier consists of two parts, a fixed gain section (approximately 20) followed by a section with selectable gain in binary steps. Both gain sections employ the basic three transistors transimpedance feedback amplifier. The total maximum amplifier gain is approximately 640.

The following description is applied to the first fixed gain section, where the same principle can be applied to the other as well. Because of the inherent low input impedance, a common base configuration Q3 is used as the input stage. Gain is obtained from output stage Q4 and Q5. Load resistor R16 of Q4 is bootstrapped to the emitter of Q5 to increase the gain of Q4. This provision causes a very high open loop transimpedance of approximately 1.3×10^6 ohms. A d.c. negative feedback through R14 is utilized to stabilize both overall gain and bias level. The voltage gain of the section is very near to the ratio of R14 and R10. With supply voltage of 12 volts, a linear range of output voltage over 5 volts is achieved.

3.1.3 <u>The discriminator circuit</u> : The discriminator section is a simple tunnel diode discriminator comprising R28, D2 and Q9. Negative pulses with amplitude exceeding 1.1 volt from the amplifier output will trigger D2 to the high state and turns Q9 on. An output pulse with 5V amplitude will be generated across R29. In quiescent state only leakage current flow through D2 and collector of Q9 is almost at ground potential. The output pulse from the discriminator will pass through the gate circuit described in section 3.2 before they are counted in the scaling section.

3.2 <u>Timer and Gate</u> (Fig. 3.2)

<u>General</u> : This circuit module provides internal control of the counting time in the scaling channel.

Operation

3.2.1 The timer circuit : The timer circuit consists of Q1 operating as a relaxation oscillator with R1 and C1 establishing the time constant. A positive pulse with pulse rate 42.67 pulse/sec is developed at base 1 and is coupled to Q2.

When the instrument is counting, Q2 is driven to saturation with each pulse, said pulse is then coupled to the monostable multivibrator with a period of 70 μs. The pulse from monostable multivibrator is then coupled to the IC binary count down and the non-indicating decade counters.

When the instrument is not counting (count complete or hold condition), the base of Q2 is shorted to ground by the output Q of IC 6 flip-flop, blocking the pulses to the count down circuit.

The clock rate of Q1 may be calibrated by adjusting R1. Q1 is temperature compensated by setting R2. R2 will not normally require adjustment unless Q 1 is changed.

3.2.1.1 Clock rate calibration

To calibrate the clock frequency :

1. Attach a frequency meter lead to the collector of Q5.
2. Adjust R1 for the proper frequency of 42.67 Hz.
3. Heat Q1 with the point of a small soldering iron for approximately 10 seconds.
4. Observe any shift in frequency.
5. If a shift occurs, allow the transistor to cool until the frequency has returned to the starting position.

6. Adjust R2 to move the frequency in the direction of the high temperature shift. Adjust for approximately 75 % of change in frequency.

7. Repeat heating cycle for finer adjustment. Allow a cooling period of at least 20 times the heating period in this adjustment.

3.2.2 The gate circuit : The gate circuit (Q8) is a parallel gate which is connected across the input of the scaling circuit (Fig. 3.3).

In the stop-state (START-STOP switch is at the STOP position or the clock circuit is held by timing pulse), the collector of Q7 rises to 5 volts and Q8 is forward biased. Any positive signals appearing at the collector of Q8 will be bypassed to ground through the low collector-emitter impedance of saturated Q8 and no signal enters the input of the scaling circuit.

In the counting interval, Q7 is saturated, clamping the base of Q8 at approximately ground potential. Q8 is cut-off. The gate is opened, allowing signals appearing at its collector to pass to the input of the scaling unit through capacitor C6 and attenuator R22 and R23. Diode D12 is used to by-pass the negative overshoot of the incoming signal that may impair the proper function of the decade counter in the scaling unit.

3.3 Scaling and Display (Fig. 3.3)

General : This module is to scale and display the digits of the total counts of the incoming signal during the preset time interval.

Operation

3.3.1 The scaling circuit and display : The scaling circuit comprises of two modules of three UP/DOWN decade counters IC4, IC5 and IC 6. The first decade counter receives the signal pulses from the gate circuit in Fig. 3.2, scales the signals by a factor of ten and sends the output pulse to the next decade counter. The decade counters count in the BCD 1-2-4-8 code and their BCD outputs are used to drive the BCD to decimal decoder drivers IC1, IC2 and IC3. The ten mutually exclusive outputs of the decoder drivers control directly the operation of the readout tube V1, V2 and V3 which will indicate in decimal digits the number of input pulses which actually pass through the gate circuit.

3.4 H.V. Supply (Fig. 3.4)

General : The high voltage supply module is used to provide the high voltage (ranging from 700 to 1,600 V) for the nuclear radiation detectors and a power supply for gas readout tubes.

Operation

3.4.1 The high voltage supply circuit : The high voltage supply circuit employs a DC-DC push pull converter comprising of transistors Q1, Q2 and transformer T1. The converter draws the power directly from 12V Battery Power Supply. The output pulse at the secondary windings of the transformer T1 is a square wave with frequency around 5kHz. The output voltage at the winding designated by N_3 is rectified by diode D1 and filtered by capacitor C3 to provide a 200V at 6 mA supply to the readout tubes. Boosted by N3 the winding

N4 provides high voltage for nuclear radiation detector. Diodes D2, D3 and capacitors C4, C5 form a voltage doubler circuit providing high voltage which is further regulated by resistor R4 and regulator tube V1. Depending on the types of detector used, the regulated high voltage may be varied by using proper regulator tubes and proper dimensioning of N4 and R4. Fig. 3.4 shows a schematic diagram for high voltage of 1100 volts.

3.4.2 <u>5V Regulated supply circuit</u> : The 5V regulated supply is used to provide regulated power supply for the integrated circuits used in the timer and scaler units. In addition, it provides regulated power supply for the preamplifier unit and discriminator unit given in Fig. 3.1. Zener diode D4 is used to provide a reference voltage of 5.6V for Q3 which is connected in series regulator type. The drop in voltage between base and emitter of Q3 about 0.6V caused output voltage to be 5V. The circuit can provide 5V regulated output at 2.88A.