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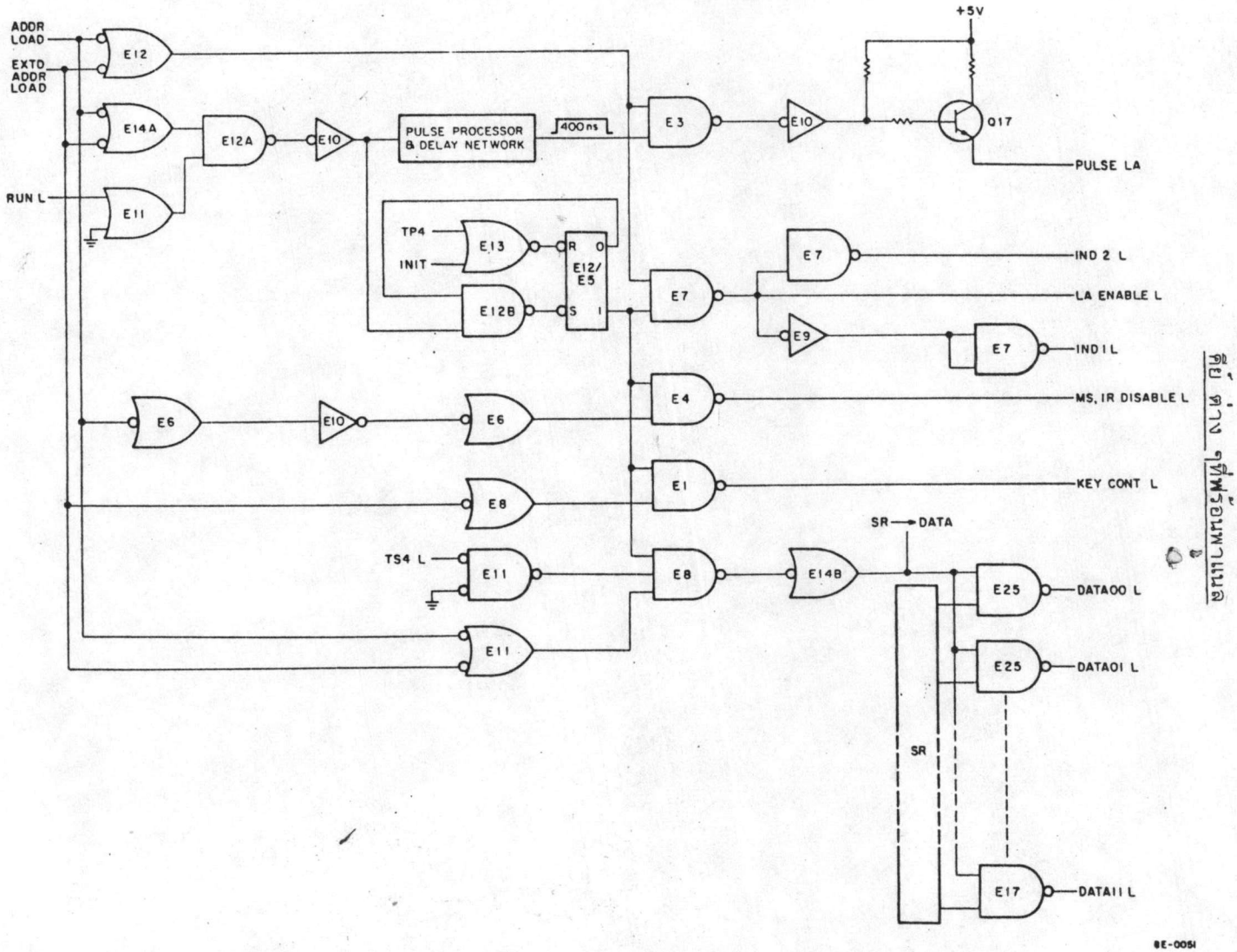
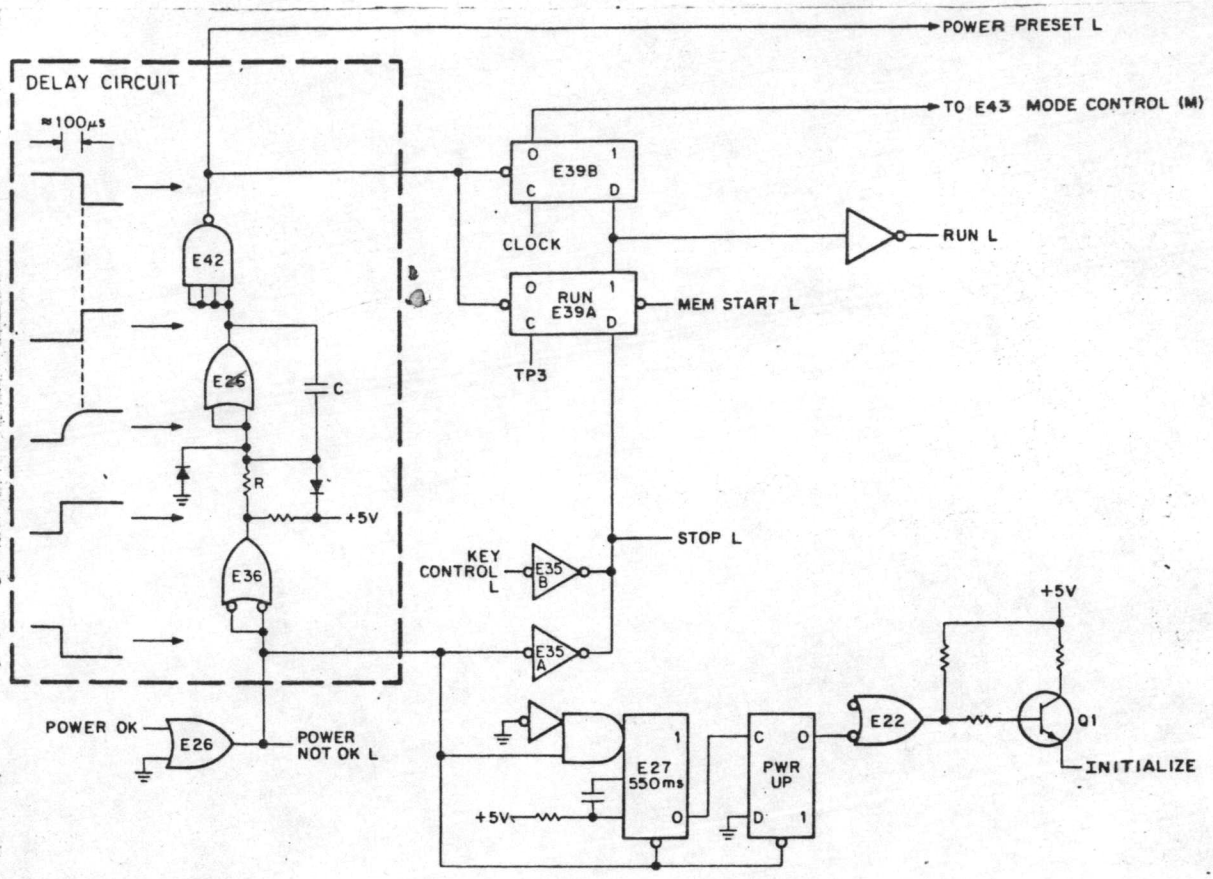
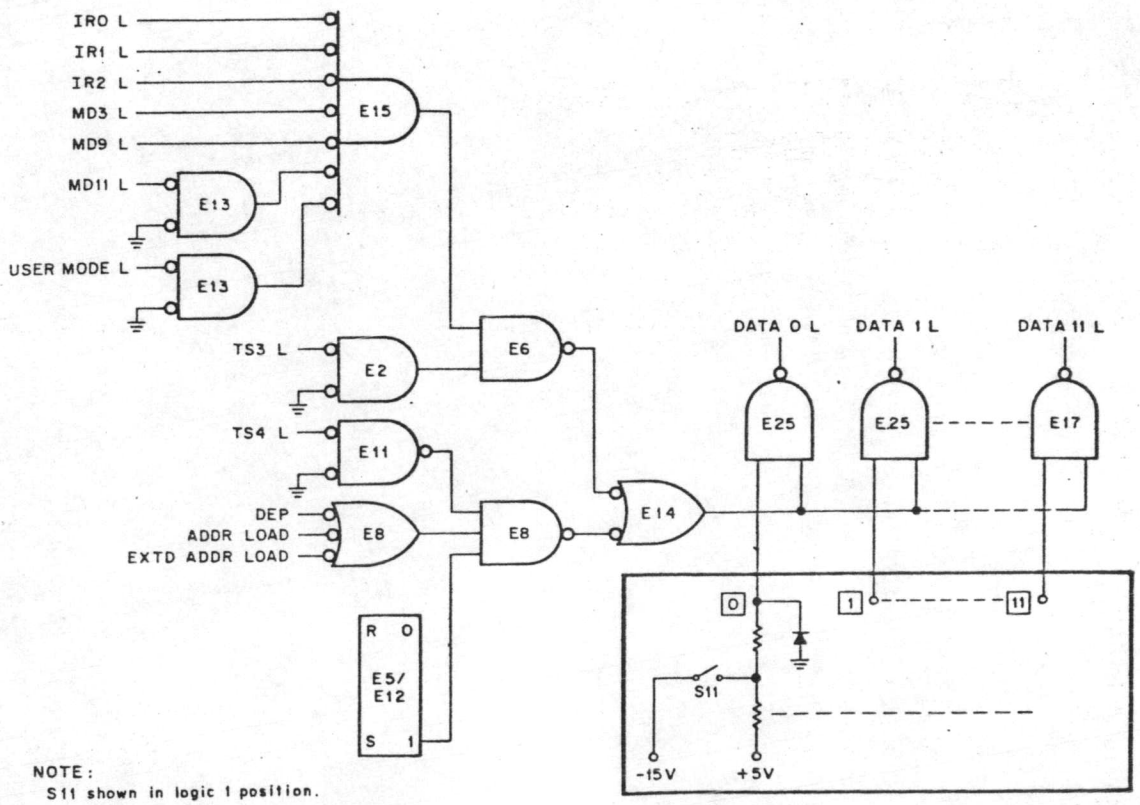


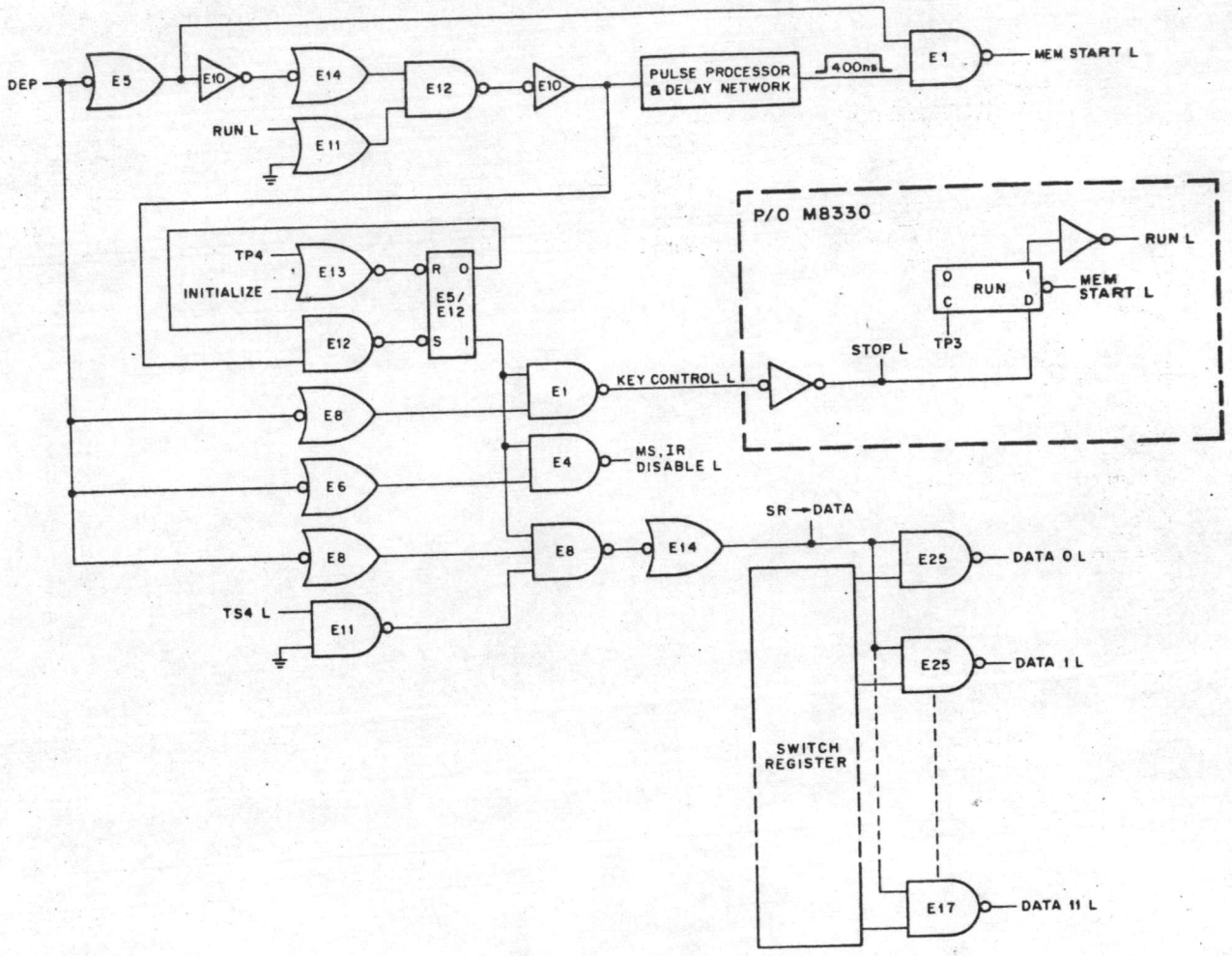
LOAD and EXTD LOAD Keys



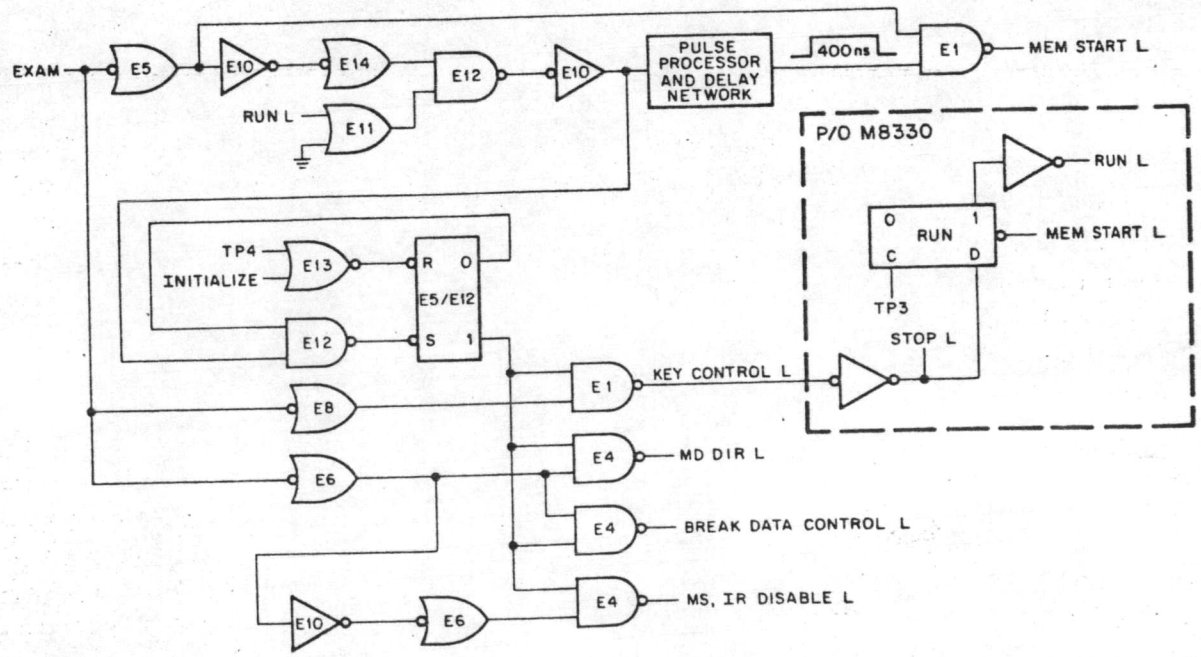
Power-On Preset Control Logic



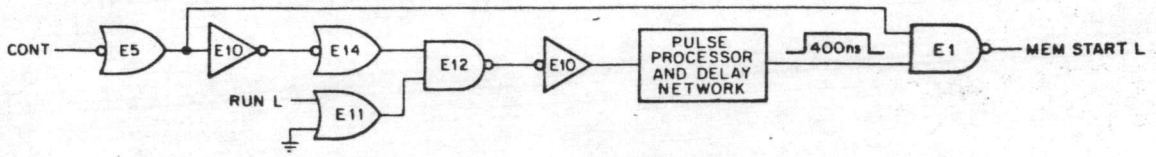
Switch Register Control Logic



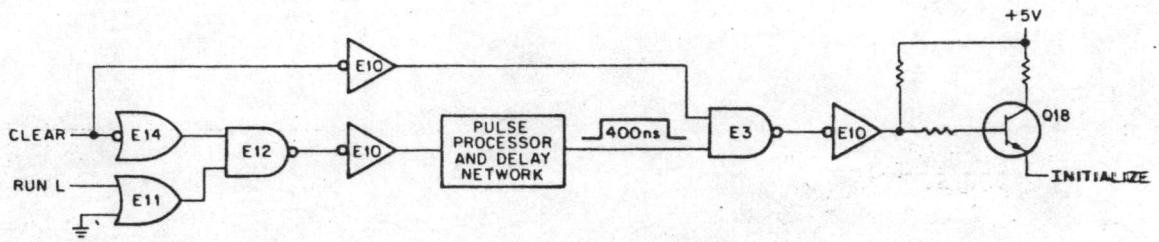
DEP Key Logic



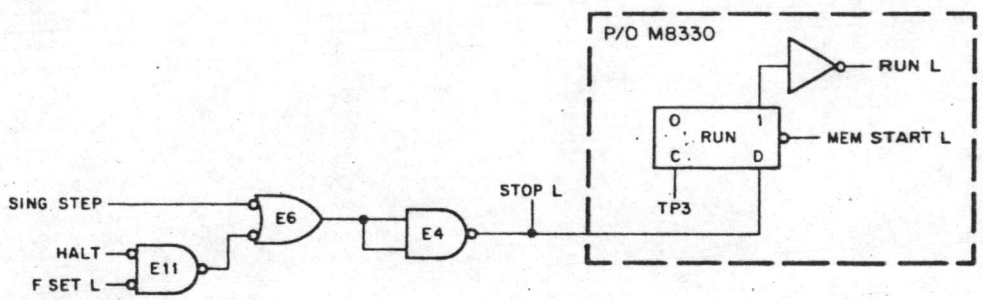
EXAM Key Logic



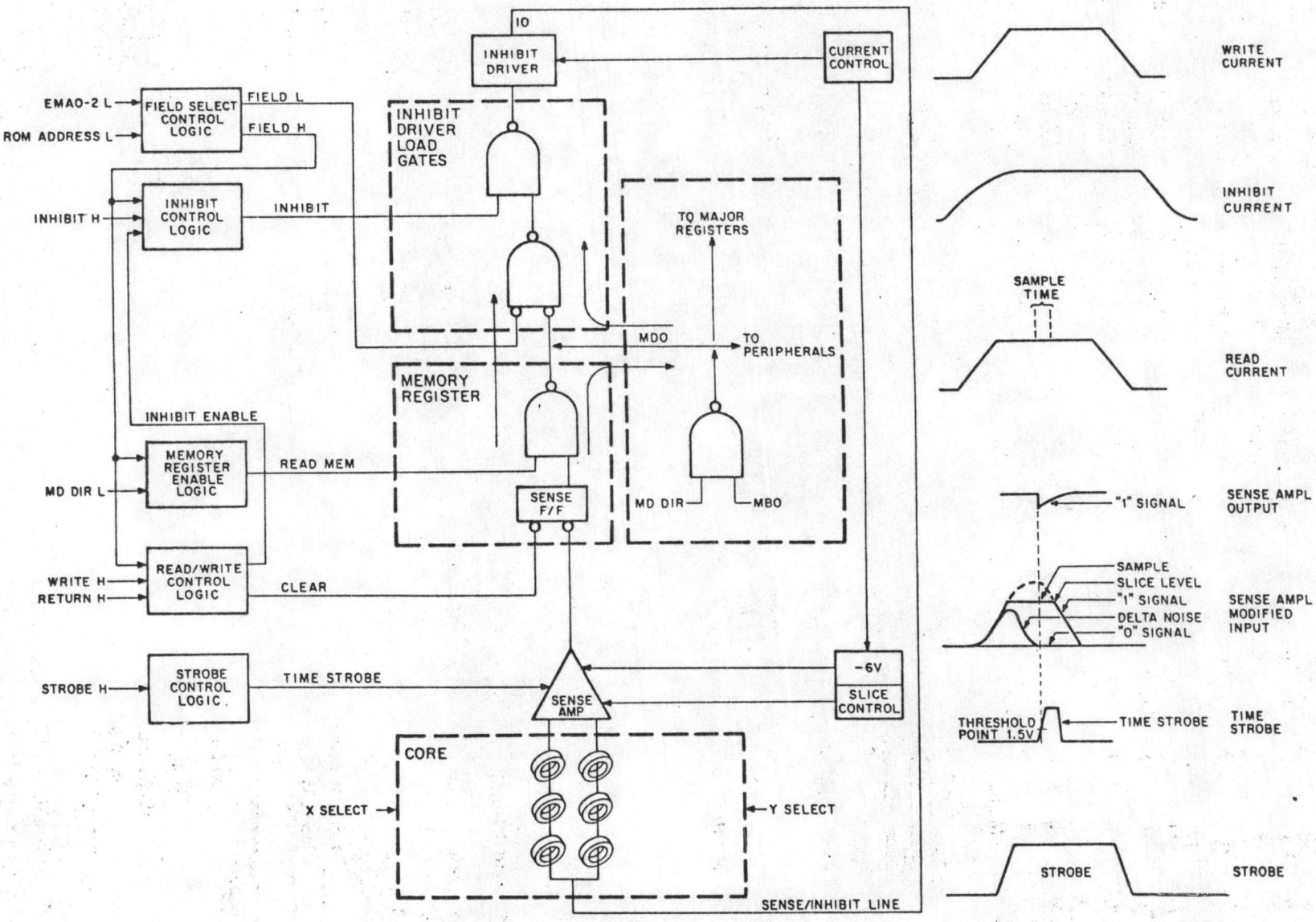
CONT Key Logic



CLEAR Key Logic



SING STEP and HALT Switch Logic



READ/WRITE Operation, Simplified Diagram (Bit 0)

ภาคผนวก ข.

IC เบอร์ที่ใช้งาน

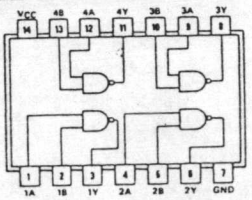
54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

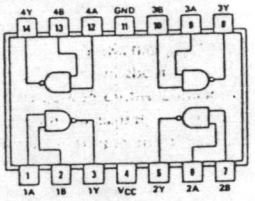
PIN ASSIGNMENTS (TOP VIEWS)

QUADRUPLE 2-INPUT
POSITIVE-NAND GATES

00

positive logic:
$Y = \overline{AB}$





SN5400 (J)
SN54H00 (J)
SN54L00 (J)
SN54LS00 (J, W)
SN54S00 (J, W)

SN7400 (J, N)
SN74H00 (J, N)
SN74L00 (J, N)
SN74LS00 (J, N)
SN74S00 (J, N)

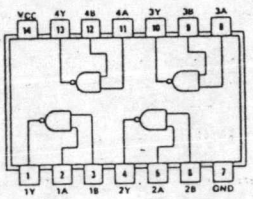
SN5400 (W)
SN54H00 (W)
SN54L00 (T)

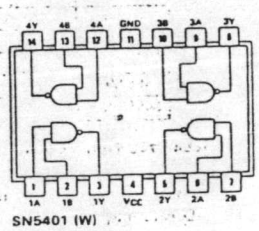
See page 6-2

QUADRUPLE 2-INPUT
POSITIVE-NAND GATES
WITH OPEN-COLLECTOR OUTPUTS

01 8881

positive logic:
$Y = \overline{AB}$

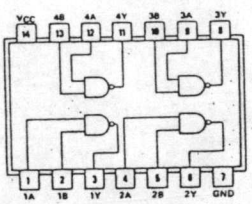




SN5401 (J)
SN54LS01 (J, W)

SN7401 (J, N)
SN74LS01 (J, N)

SN5401 (W)
SN54H01 (W)
SN54L01 (T)



SN54H01 (J)

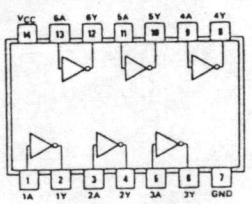
SN74H01 (J, N)

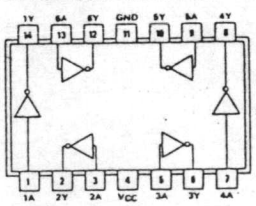
See page 6-4

HEX INVERTERS

04

positive logic:
$Y = \overline{A}$





SN5404 (J)
SN54H04 (J)
SN54L04 (J)
SN54LS04 (J, W)
SN54S04 (J, W)

SN7404 (J, N)
SN74H04 (J, N)
SN74L04 (J, N)
SN74LS04 (J, N)
SN74S04 (J, N)

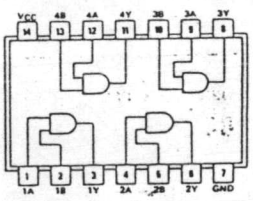
SN5404 (W)
SN54H04 (W)
SN54L04 (T)

See page 6-2

QUADRUPLE 2-INPUT
POSITIVE-AND GATES

08

positive logic:
$Y = AB$



SN5408 (J, W)
SN54LS08 (J, W)
SN54S08 (J, W)

SN7408 (J, N)
SN74LS08 (J, N)
SN74S08 (J, N)

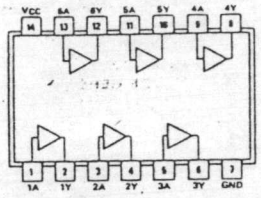
See page 6-10

HEX BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

17

positive logic:
Y = A

See page 6-24



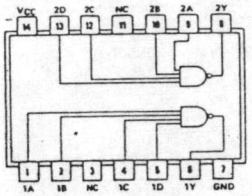
SN5417 (J, W) SN7417 (J, N)

DUAL 4-INPUT
POSITIVE-NAND GATES

20

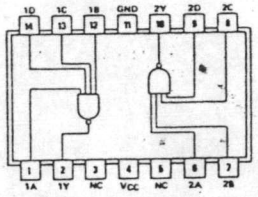
positive logic:
$Y = \overline{ABCD}$

See page 6-2



SN5420 (J)
SN54H20 (J)
SN54L20 (J)
SN54LS20 (J, W)
SN54S20 (J, W)

SN7420 (J, N)
SN74H20 (J, N)
SN74L20 (J, N)
SN74LS20 (J, N)
SN74S20 (J, N)



SN5420 (W)
SN54H20 (W)
SN54L20 (T)

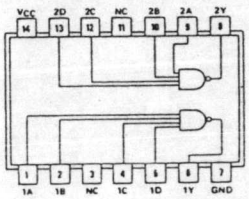
NC—No internal connection

DUAL 4-INPUT
POSITIVE-NAND BUFFERS

40

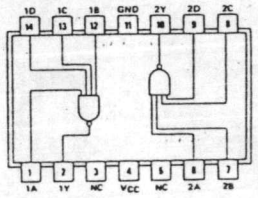
positive logic:
$Y = \overline{ABCD}$

See page 6-20



SN5440 (J)
SN54H40 (J)
SN54LS40 (J,W)
SN54S40 (J, W)

SN7440 (J, N)
SN74H40 (J, N)
SN74LS40 (J, N)
SN74S40 (J, N)



SN5440 (W)
SN54H40 (W)

NC—No internal connection

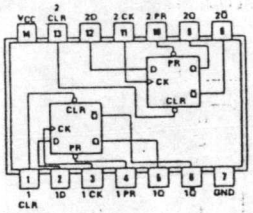
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

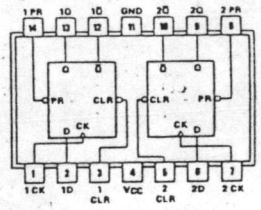
74

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\bar{Q}$
L	H	X	X	L	H
H	L	X	X	H	L
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

See pages 6-46, 6-50, 6-54, and 6-56





SN5474 (J)
SN54H74 (J)
SN54L74 (J)
SN54LS74A (J, W)
SN54S74 (J, W)

SN7474 (J, N)
SN74H74 (J, N)
SN74L74 (J, N)
SN74LS74A (J, N)
SN74S74 (J, N)

SN5474 (W)
SN54H74 (W)
SN54L74 (T)

See explanation of function tables on page 3-8.
* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

4-BIT BISTABLE LATCHES

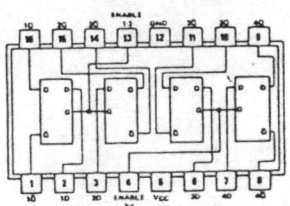
75

FUNCTION TABLE
(Each Latch)

INPUTS		OUTPUTS	
D	G	Q	$\bar{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\bar{Q}_0$

H = high level, L = low level, X = irrelevant
Q_0 = the level of Q before the high-to-low transition of G

See page 7-35

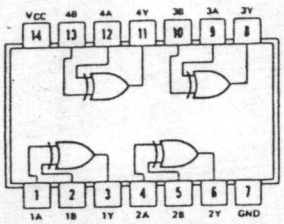


SN5475 (J, W)
SN54L75 (J)
SN54LS75 (J, W)

SN7475 (J, N)
SN74L75 (J, N)
SN74LS75 (J, N)

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

86 $Y = A \oplus B = \bar{A}B + A\bar{B}$

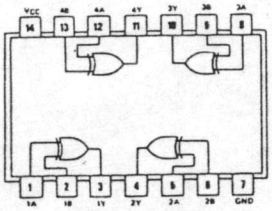


SN5486 (J, W) SN7486 (J, N)
SN54LS86 (J, W) SN74LS86 (J, N)
SN54S86 (J, W) SN74S86 (J, N)

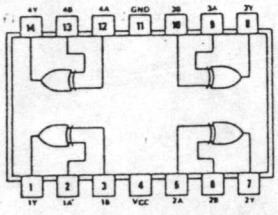
FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level



SN54L86 (J) SN74L86 (J, N)



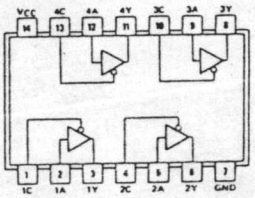
SN54L86 (T)

See page 7-65

QUADRUPLE BUS BUFFER GATES WITH THREE-STATE OUTPUTS

125

positive logic:
Y = A
Output is off (disabled) when C is high.

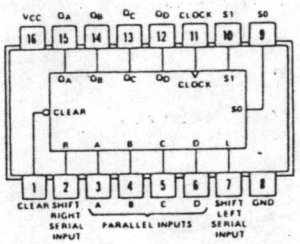


SN54125 (J, W) SN74125 (J, N)
SN54LS125 (J, W) SN74LS125 (J, N)

See page 6-33

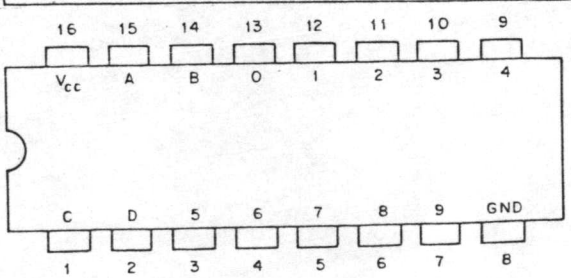
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

194

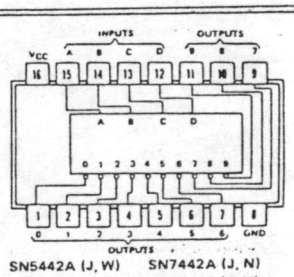


SN54194 (J, W) SN74194 (J, N)
SN54LS194A (J, W) SN74LS194A (J, N)
SN54S194 (J, W) SN74S194 (J, N)

See page 7-316



PIN LOCATOR
(TOP VIEW OF IC)



SN5442A (J, W) SN7442A (J, N)
SN54L42 (J) SN74L42 (J, N)
SN54LS42 (J, W) SN74LS42 (J, N)
SN5443A (J, W) SN7443A (J, N)
SN54L43 (J) SN74L43 (J, N)
SN5444A (J, W) SN7444A (J, N)
SN54L44 (J) SN74L44 (J, N)

DEC 8251 IC Illustration

FEATURES

- Low Power - typ $<5.0\mu W$ standby
- Excellent Speed Operation
- TTL or CMOS Compatible On Inputs and Outputs
- 4V–11V V_{CC} Operation
- Static Operation
- On-Chip Address Register

CMOS RAM 1024 BIT IM6508/IM6518 IM6508A/IM6518A

GENERAL DESCRIPTION

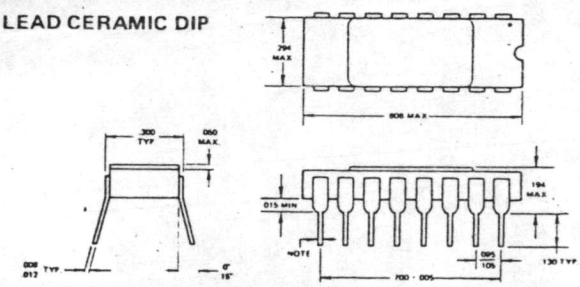
The IM6508/18 are high speed, low power, silicon gate CMOS 1024 bit static RAM's organized 1024 words by 1 bit. In all static states these RAM's exhibit the microwatt power requirements typical of CMOS. Inputs and three state output are TTL compatible. The basic part operates at 4 to 7 volts with a 5V, 25°C access time of 350 ns and supply current of 100μA. Faster access times and lower supply currents are offered in a DASH-1 version. Higher operating voltages are offered in an "A" version. Data retention is guaranteed to 2.2 volts on all parts.

Write Enable and Chip Select functions are active in the low state. These functions are specified for easy interface to common I/O data busses. On chip address registers (clocked by the falling edge of STR) can often improve system performance and reduce package count. The two additional chip selects available on the IM6518 allow faster system design and reduced interconnect by multiplexing addresses, data in and data out on the same lines.

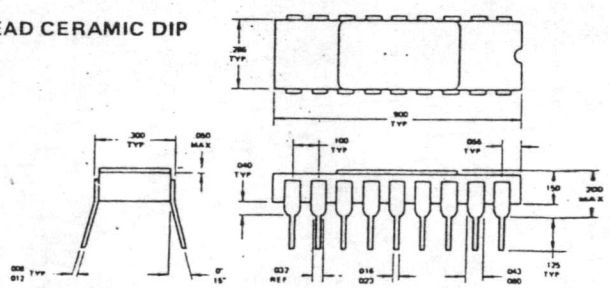
These devices are ideally suited for memory systems requiring low operating power, high performance or non-volatility (battery backup).

PACKAGE DIMENSIONS

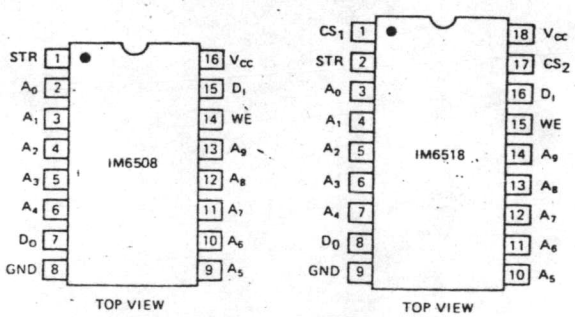
16 LEAD CERAMIC DIP



18 LEAD CERAMIC DIP



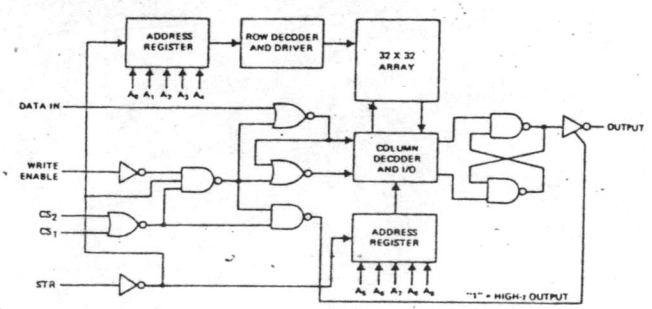
CONNECTION DIAGRAMS



Pin 1 is designated either by a dot or a notch.

FUNCTIONAL DIAGRAM IM6518

The IM6508 functions as if CS_1, CS_2, and STR were tied together.



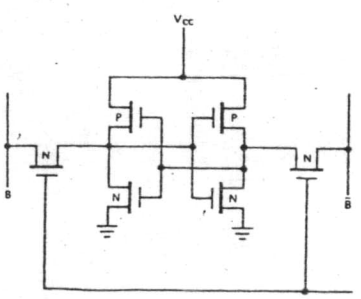
ORDERING INFORMATION

MEMORY CIRCUIT MARKING AND PRODUCT CODE EXPLANATION:

IM 6 5 08A-1 I DE

- Package
  - DE - Ceramic 16 pin DIP
  - DN - Ceramic 18 pin DIP
- Temperature Range
  - I - Industrial (-40°C to +85°C)
  - M - Military (-55°C to +125°C)
- Specific Type
- General Type
  - Random Access Memory (RAM)

CELL



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND −0.5V to V_{CC}+0.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Industrial	−40°C to +85°C
Military	−55°C to +125°C

DC CHARACTERISTICS V_{CC} = 4V to 11V, T_A = Industrial or Military

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		70% V_{CC}			V
Logical "0" Input Voltage	V_{IL}				20% V_{CC}	V
Input Leakage	I_{IL}	$0V \leq V_{IN} \leq V_{CC}$	−1.0		1.0	μA
Logical "1" Output Voltage	V_{OH}	$I_{OUT} = 0$	V_{CC} − 0.01			V
Logical "0" Output Voltage	V_{OL}	$I_{OUT} = 0$			GND + 0.01	V
Output Leakage	I_O	$0V \leq V_o \leq V_{CC}$	−1.0		1.0	μA
Supply Current IM6508A/18A	I_{CC}	$V_{IN} = V_{CC}$		5.0	500	μA
	I_{CC}	V_{CC} = STR = 3.0V		0.1	10	μA
IM6508A-1/18A-1	I_{CC}	$V_{IN} = V_{CC}$		1.0	100	μA
	I_{CC}	V_{CC} = STR = 3.0V		0.01	1.0	μA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_O			6.0	10.0	pF

AC CHARACTERISTICS V_{CC} = 5.0V, 10V C_L = 50 pF, T_A = 25°C

PARAMETER	SYMBOL	V_{CC}	IM6508A-1/18A-1		IM6508A/18A		UNITS
			MIN	MAX	MIN	MAX	
Access Time From STR	t_{AC}	5		200		350	ns
		10		95		150	ns
Output Enable Time	t_{EN}	5		120		210	ns
		10		55		90	ns
Output Disable Time	t_{DIS}	5		120		210	ns
		10		55		90	ns
STR Pulse Width (Positive)	t_{STR}	5	135		235		ns
		10	65		95		ns
STR Pulse Width (Negative)	$t_{\overline{STR}}$	5	200		350		ns
		10	95		150		ns
Write Pulse Width (Negative)	t_{WP}	5	135		235		ns
		10	65		95		ns
Address Setup Time	t_{ADDS}	5	5		10		ns
		10	5		10		ns
Address Hold Time	t_{ADDH}	5	60		105		ns
		10	30		45		ns
Date Setup Time	t_{DS}	5	135		235		ns
		10	65		95		ns
Data Hold Time	t_{DH}	5	0		0		ns
		10	0		0		ns

CMOS TO TTL

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Supplied	GND −0.5V to V_{CC}+0.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Industrial	−40°C to +85°C
Military	−55°C to +125°C

DC CHARACTERISTICS V_{CC} = 5.0V ±10% T_A = Industrial or Military

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		V_{CC} − 2.0			V
Logical "0" Input Voltage	V_{IL}				0.8	V
Input Leakage	I_{IL}	$0V \leq V_{IN} \leq V_{CC}$	−1.0		1.0	μA
Logical "1" Output Voltage	V_{OH2}	I_{OUT} = 0	V_{CC} − 0.01			V
Logical "1" Output Voltage	V_{OH1}	I_{OH} = −0.2 mA	2.4			V
Logical "0" Output Voltage	V_{OL2}	I_{OUT} = 0			GND + 0.01	V
Logical "0" Output Voltage	V_{OL1}	I_{OL} = 2.0 mA			0.45	V
Output Leakage	I_O	$0 V \leq V_o \leq V_{CC}$	−1.0		1.0	μA
Supply Current IM6508/18	I_{CC}	$V_{IN} = V_{CC}$		1.0	100	μA
	I_{CC}	V_{CC} = STR = 3.0V		0.1	10	μA
IM6508-1/18-1	I_{CC}	$V_{IN} = V_{CC}$		0.1	10	μA
	I_{CC}	V_{CC} = STR = 3.0V		0.01	1.0	μA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_O			6.0	10.0	pF

AC CHARACTERISTICS V_{CC} = 5.0V ±10%, C_L = 50 pF (One TTL Load), T_A = Industrial or Military

PARAMETER	SYMBOL	IM6508-1/18-1		IM6508/18		UNITS
		MIN	MAX	MIN	MAX	
Access Time From STR	t_{AC}		300		460	ns
Output Enable Time	t_{EN}		180		285	ns
Output Disable Time	t_{DIS}		180		285	ns
STR Pulse Width (Positive)	t_{STR}	200		300		ns
STR Pulse Width (Negative)	$t_{\overline{STR}}$	300		460		ns
Write Pulse Width (Negative)	t_{WP}	200		300		ns
Address Setup Time	t_{ADDS}	7		15		ns
Address Hold Time	t_{ADDH}	90		130		ns
Data Setup Time	t_{DS}	200		300		ns
Data Hold Time	t_{DH}	0		0		ns

SWITCHING WAVEFORMS AND SWITCHING TIME LOAD

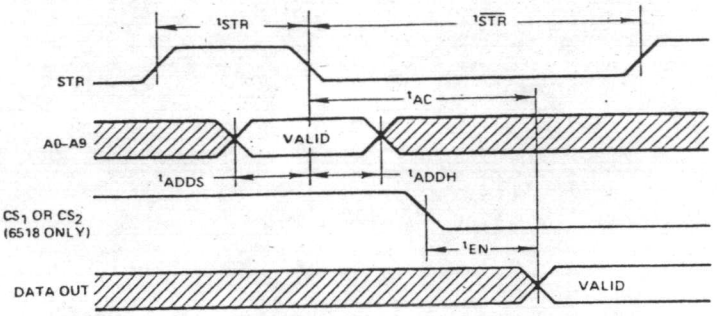


FIGURE 1. READ CYCLE

The IM6508 output is active when STR is low. The IM6518 output data latch retains the data when STR returns high.

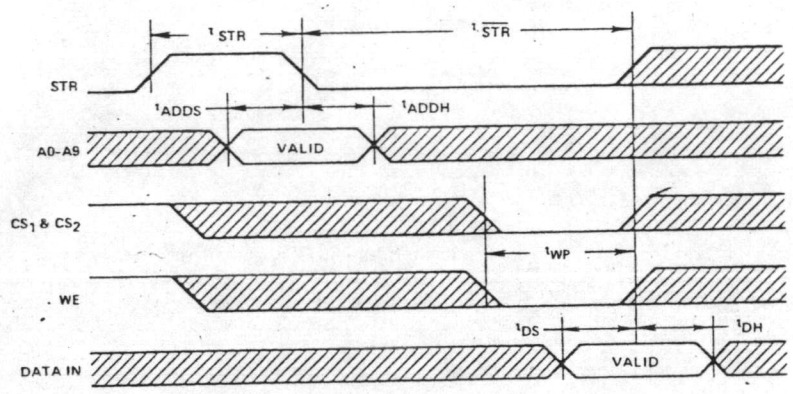


FIGURE 2. WRITE CYCLE

The IM6508 performs a write operation when STR = WE = 0. The IM6518 performs a write operation when STR = CS_1 = CS_2 = WE = 0. The write operation is terminated on any positive edge from STR or CS_1 or CS_2 or WE.

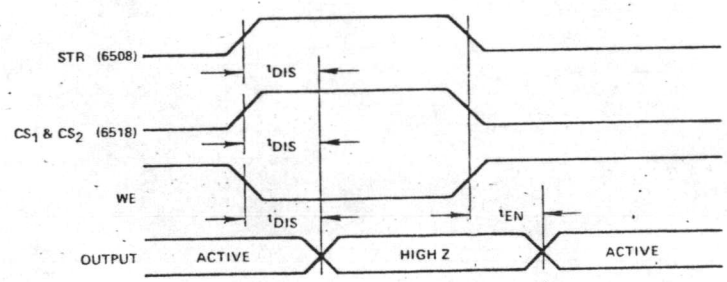


FIGURE 3. OUTPUT ENABLE

The IM6508 output is high impedance when STR = 1 or WE = 0. The IM6518 output is high impedance when CS_1 or CS_2 = 1 or WE = 0.

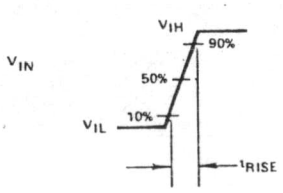
IM6508

STR	WE	OPERATION	OUTPUT
0	0	Write	High Resistance
0*	1	Read	Memory Data
1	X	Hold	High Resistance

* Addresses are loaded on chip by the falling edge of STROBE.

IM6518

STR	CS1	CS2	WE	OPERATION	OUTPUT
0	0	0	0	Write	High Resistance
0*	0	0	1	Read	Memory Data
1	0	0	1	Read	Memory Data
X	0	1	X	Hold	High Resistance
X	1	0	X	Hold	High Resistance



$t_{rise} = t_{fall} = 20$ ns

DELAY TIMES ARE MEASURED FROM 50% TO 50%

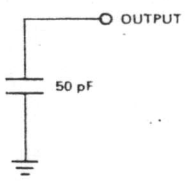
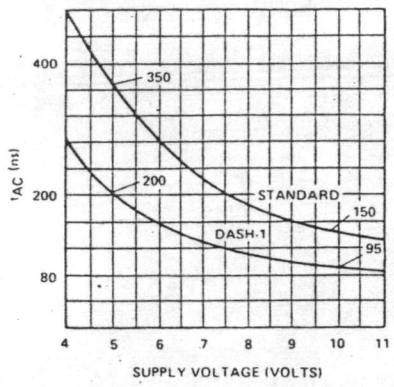


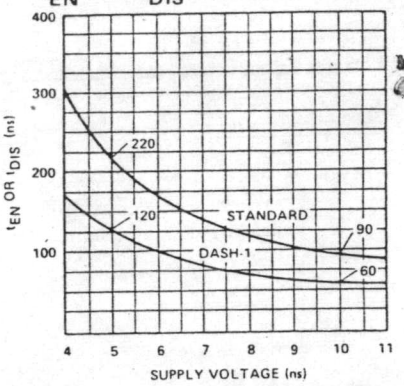
FIGURE 4. SWITCHING TIME WAVEFORMS AND LOAD

GUARANTEED AC CHARACTERISTICS

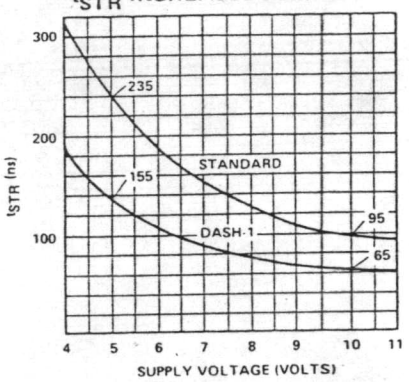
ACCESS TIME FROM STR
t_{AC} INCREASES 0.3%/°C



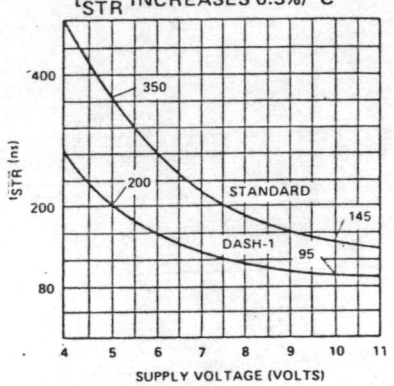
OUTPUT ENABLE TIME
OUTPUT DISABLE TIME
t_{EN} AND t_{DIS} INCREASE 0.3%/°C



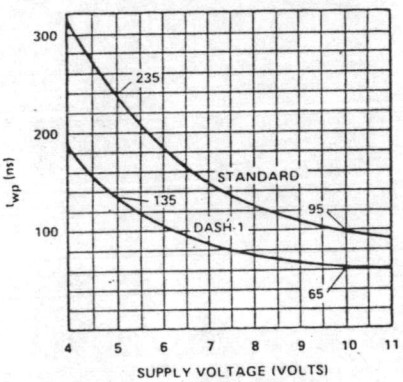
MINIMUM STR PULSE
WIDTH (POSITIVE)
t_{STR} INCREASES 0.3%/°C



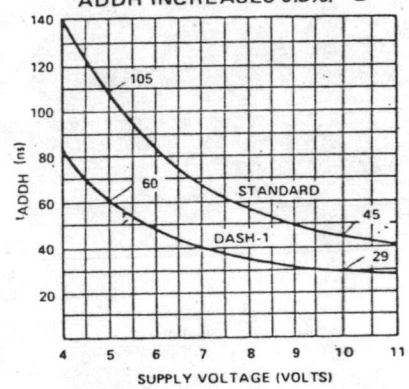
MINIMUM STR PULSE WIDTH (NEGATIVE)
$t_{\overline{STR}}$ INCREASES 0.3%/°C



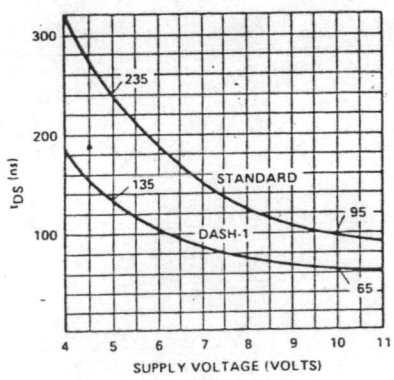
WRITE PULSE WIDTH
twp INCREASES 0.3%/°C



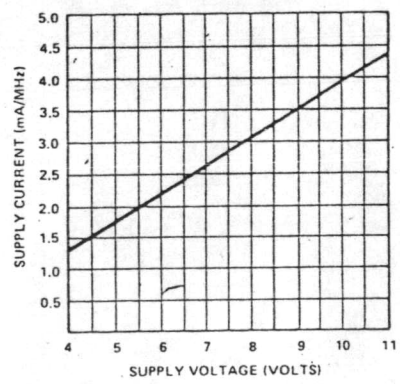
ADDRESS HOLD TIME
t_{ADDH} INCREASES 0.3%/°C



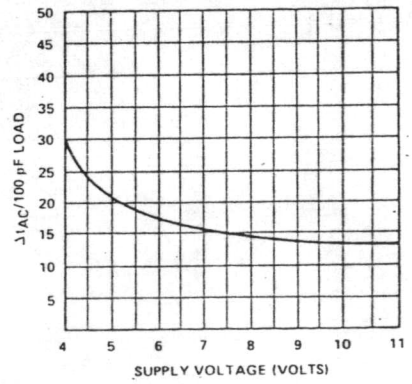
INPUT DATA SETUP TIME
t_{DS} INCREASES 0.3%/°C



DYNAMIC POWER REQUIREMENTS
AT 1 MHz I_{DYN} = (CURVE VALUE)
(OPERATING FREQUENCY)/ (1 MHz)

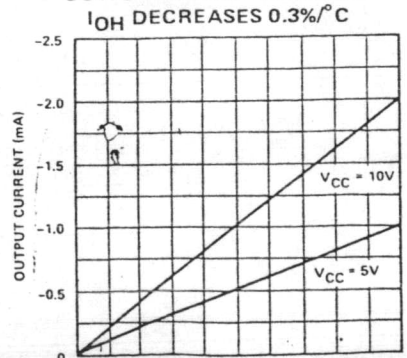


DELTA ACCESS TIME
PER 100 pF LOAD CAPACITANCE
Δt_{AC} INCREASES 0.3%/°C

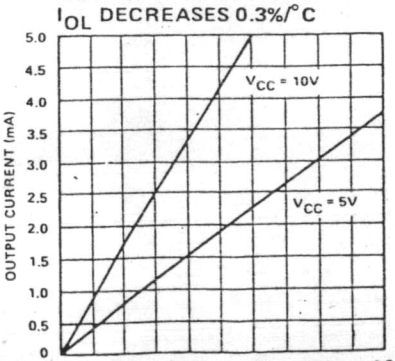


GUARANTEED DC CHARACTERISTICS

OUTPUT SOURCE CURRENT
I_{OH} DECREASES 0.3%/°C



OUTPUT SINK CURRENT
I_{OL} DECREASES 0.3%/°C



ภาคผนวก ค.

PDP-8/E Key Function Signal

KEY LA

KEY LA	H	Qualification for MA LOAD
MS DISABLE	L	Disables MAJOR STATES and IR
MD DIR	L	No use for KEY LA
BK DATA CONTROL	L	No use for KEY LA
SR BUS	H	Enables SR to the DATA BUS

KEY EXAM

KEY CONTROL	L	Allows one timing cycle only
MS DISABLE	L	Disables MAJOR STATES and IR
MD DIR	L	Enables MEM ⟶ MD LINES
BK DATA CONTROL	L	Enables MD ⟶ MB
SR BUS	L	Disabes SR ⟶ BUS

KEY DEP

KEY CONTROL	L	Allows one timing cycle only
MS DISABLE	L	Disables MAJOR STATES and IR
MD DIR	H	Disables MEM ⟶ MD LINES
BK DATA CONTROL	H	Disables MD ⟶ MB
SR BUS	H	Enables SR ⟶ BUS

ภาคผนวก ง.

Specification ของแผ่นโมดูล CMOS

ชื่อ	:ส่วนความจำแบบ CMOS 4K words
ความจุ	:ขนาด 12/4096 bit-words ต่อแผ่นโมดูล
จุดประสงค์	:ใช้กับเครื่องคอมพิวเตอร์ขนาดเล็ก ของ DEC
	PDP-8/E
	PDP-8/M
	PDP-8/F
ขนาด	:ความกว้าง เท่ากับ 8.5 นิ้ว
	ความยาว เท่ากับ 10.5 นิ้ว
	ความหนา เท่ากับ 0.5 นิ้ว
การทำงาน	:วัฏจักรการอ่าน 150 nSec
	วัฏจักรการเขียน 650 nSec
การอินเตอร์เฟทI/O	:ต่อกับ TTL แบบ Open Collector ได้
DC Power	: +5 v $\pm$ 10 %
	กระแสใช้งาน ไม่เกิน 500 MA /โมดูล
	กระแสใช้งานเมื่อเก็บข้อมูล 536.2 μA /โมดูล
อุณหภูมิ	:0°c ถึง +50°c ขณะทำงาน
ความชื้นสัมพัทธ์	:สูงถึง 90 %
การรักษาข้อมูล	:สามารถเก็บข้อมูลไว้ได้นาน 39 วัน ขณะปิดเครื่อง

ข้อดี

ก. ราคาถูกกว่าส่วนความจำวงแหวนแม่เหล็ก ๓๐๐%

ข. เชื่อถือได้ ๙๐%

ค. สามารถขยายแผ่นโมดูลเพิ่มขึ้นได้ ถึง 32 K-words

ง. แผ่นโมดูลสามารถสลับเปลี่ยนที่กันได้

จ. วัฏจักรการทำงานได้เร็วเท่ากับ ส่วนความจำแบบวงแหวนแม่เหล็ก

ฉ. สูญเสียพลังงานการแผ่กระจายต่ำ

ช. สามารถทำงานร่วมกับส่วนความจำแบบวงแหวนแม่เหล็ก

ซ. มี Address Register อยู่ในตัวเอง

ฌ. เป็นระบบส่วนความจำแผ่นเดียว ขนาดกระทัดรัด

ญ. สามารถเก็บรักษาข้อมูลไว้ได้นานถึง ๓๙ วัน ขณะที่เครื่องไม่ทำงาน

ฎ. การบำรุงรักษาทำได้ง่าย

ภาคผนวก จ.

IDENTIFICATION A.

PRODUCT CODE	:	MAINDEC -8E -D 1 FB -D
PRODUCT NAME	:	PDP -8E EXTENDED MEMORY ADDRESS TEST (EA 8 E)
DATE	:	JUNE 14, 1971
MAINTAINER	:	DIAGNOSTIC GROUP
AUTHOR	:	VERNON FREY

ABSTRACT

The PDP-8/E Extended Memory Address Test is designed to detect any location that cannot be uniquely addressed. This is performed by a senes of four test routines which will test Systems equipped with from 8 K to 32 K words of core memory. Automatic program relocation is provided in order to test all memory fields from latch memory field. Teletype print-outs are provided for error identification, and the operator is given a degree of control over the program by various SR settings.

REQUIRMENTS

1. Equipment A PDP-8/E computer equipped with a minimum of 8 K words of core memory.

2. Storage The program occupies core locations ØØØØ to 3777.

3. Prelininary Programs The Binary Loader must be in memory. Also, all diagnostics for a basic 4K PDP8/E must hare been previously run successfully.

IDENTIFICATION B.

PRODUCT CODE	:	MAINDEC - Ø8-DHKMA - A - D
PRODUCT NAME	:	PDP -8E EXTENDED MEMORY DATA & CHECKERBOARD TEST
DATE CREATED	:	10 APRIL 1972
MAINTAINER	:	DIAGNOSTIC GROUP
AUTHOR	:	VERNON FREY
NOTE	:	REPLACES MAINDEC -8E-D 1 BC-D

ABSTRACT The PDP-8/E Extended Memory Data & Checkerboard Test is designed to detect memory failure due to sense-line noise under worst case conditions. The four worst case patterns provided will generate worst case noise conditions in all standard and specially purchased PDP-8E core stacks, and will test systems equipped with from 8K to 32K words of core memory. The All Ø's and All 1's patterns are provided to identify Basic memory failures. Automatic program relocation is provided in order to test all memory fields from each memory field. Teletype printouts are provided for error identification, and the operator is given a degree of control oven the program by various switch register settings.

REQUIREMENT

1. Equipment A PDP-8E Computer equipped with at least 8K of core memory

2. Storage The program occupies core location ØØØØ to 4777 and 6ØØØ to 7177 of the present field

3. Preliminary Program The Binary loader must be in memory. Also, all diagnostics for a basic 4K PDP-8E must have been previously run successfully.

ประวัติ

นายสุนทร เพชรรัชตะชาติ เกิดเมื่อวันที่ ๔ มิถุนายน พ.ศ. ๒๔๙๕ ที่อำเภอเมือง จังหวัด ตรัง สำเร็จการศึกษาปริญญาวิศวกรรมศาสตร์บัณฑิต สาขาวิศวกรรมไฟฟ้า ปีการศึกษา ๒๕๑๗ จากสถาบันเทคโนโลยีพระจอมเกล้า วิทยาเขตลาดกระบัง ปี ๒๕๑๗ ได้รับทุนผู้เชี่ยวชาญญี่ปุ่น เข้ารับราชการเป็นอาจารย์สถาบันเดียวกันนี้ แผนกวิชาวิศวกรรมคอมพิวเตอร์และระบบอัตโนมัติในปี ๒๕๑๘ และปีเดียวกันนี้ได้เข้าศึกษาต่อในแผนกวิศวกรรมคอมพิวเตอร์ บัณฑิตวิทยาลัย จุฬาลงกรณมหาวิทยาลัย ปี ๒๕๑๙ ได้รับทุนโคลัมโบ จากรัฐบาลญี่ปุ่น ไปฝึกงานด้านสื่อสารข้อมูลผ่านดาวเทียม (Data Communication) ที่มหาวิทยาลัย Electro Communication กรุงโตเกียว และที่มหาวิทยาลัยโตโฮกุ เมืองเซนได และฝึกงานด้าน Hardware เครื่อง HITAC 10 ที่บริษัทฮิตาชิ จำกัด ดูงานด้านศูนย์คอมพิวเตอร์ที่มหาวิทยาลัยโตเกียว มหาวิทยาลัยเกียวโต และดูงานการสร้างประกอบเครื่องคอมพิวเตอร์ที่บริษัท NEC

ปัจจุบันเป็นวิศวกร เครื่องฝึกบิน แบบ Air Bus A-300(Flight Simulator A-300) แผนก Flight Simulator ศูนย์ฝึกบิน บริษัทการบินไทย จำกัด