

REFERENCES

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Operational Amplifiers

LM318 operational amplifier

general description

The LM318 is a precision high speed operational amplifier designed for applications requiring wide bandwidth and high slew rate. It features a factor of ten increase in speed over general purpose devices without sacrificing DC performance.

features

- 15 MHz small signal bandwidth
- Guaranteed 50V/µs slew rate
- Maximum bias current of 500 nA
- Operates from supplies of ±5V to ±20V
- Internal frequency compensation
- Input and output overload protected
- Pin compatible with general purpose op amps

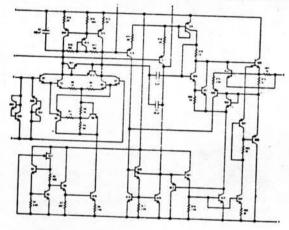
The LM318 has internal unity gain frequency compensation. This considerably simplifies its application since no external components are necessary

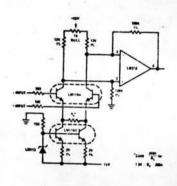
for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feedforward compensation will boost the slew rate to over $150V/\mu s$ and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under 1 μ s.

The high speed and fast settling time of these op amps make them useful in A/D converters, oscillators, active filters, sample and hold circuits, or general purpose amplifiers. These devices are easy to apply and offer an order of magnitude better AC performance than industry standards such as

The LM318 is specified for operation over 0°C

schematic diagram and typical application

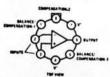




Instrumentation Amplifier

connection diagrams

Metal Can Package*

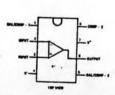


Pin connections shown on schematic diagram and typical applications are for

Order Number LM318H See Package 11

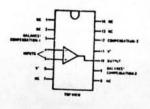
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Dual-In-Line Package



Order Number LM318N See Package 20

Dual-In-Line Package



Order Number LM318D See Package 1

2-141



absolute maximum ratings

Supply Voltage
Power Dissipation (Note 1)
Differential Input Current (Note 2)
Input Voltage (Note 3)
Output Short-Circuit Duration
Operating Temperature Range
Storage Temperature Range
Lead Temperature (Soldering, 10 sec)

±20V 500 mW ±10 mA ±15V Indefinite 0°C to 70°C -65°C to 150°C 300°C

electrical characteristics (Note 4)

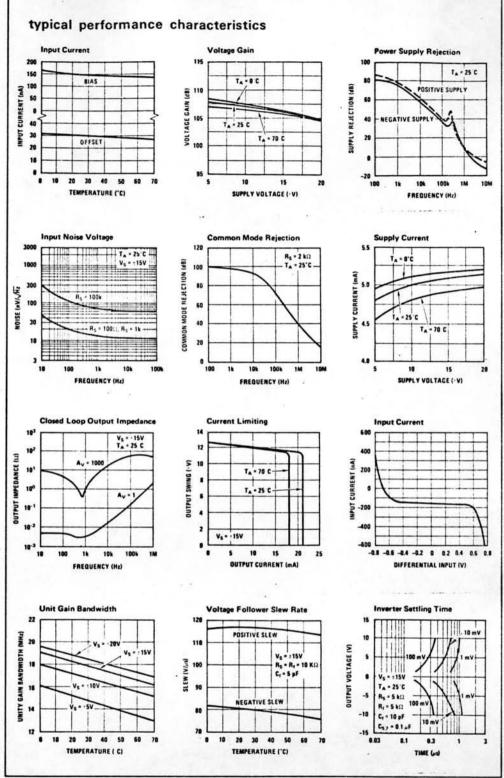
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	T _A = 25°C		4	10	m∨
Input Offset Current	T _A = 25°C		30	200	nA
Input Bias Current	T _A = 25°C		150	500	nA
Input Resistance	T _A = 25°C	0.5	3		MΩ
Supply Current	T _A = 25°C		5	10	mA
Large Signal Voltage Gain	$T_A = 25^{\circ}C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \ge 2 \text{ k}\Omega$	25	200	-8	V/mV
Slew Rate	T _A = 25°C, V _S = ±15V, A _V = 1	50	70		V/µs
Small Signal Bandwidth	T _A = 25°C, V _S = ±15V		15		MHz
Input Offset Voltage				15	mV
Input Offset Current				300	nA
Input Bias Current				750	nA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \ge 2 k\Omega$	20	į.		V/mV
Output Voltage Swing	· V _S = ±15V, R _L = 2 kΩ	±12	±13		V
Input Voltage Range	V _S = ±15V	±11.5			V
Common Mode Rejection Ratio		70	100		dB
Supply Voltage Rejection Ratio		65	80		dB

Note 1: The maximum junction temperature of the LM318 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

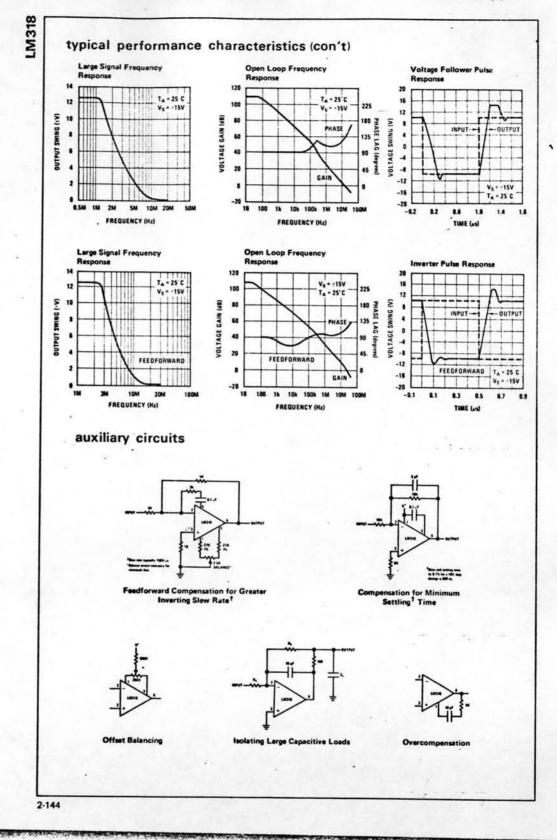
Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $\pm 5V \le V_S \le \pm 20V$ and $0^{\circ}C \le T_A \le 70^{\circ}C$, unless otherwise specified. For proper operation, the power supplies must be bypassed with 0.1 μF disc capacitors.



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Fast Summing Amplifer with Low Input Current



Wein Bridge Sine Wave Notalliator

Operational Amplifiers

LM741/LM741C operational amplifier

general description

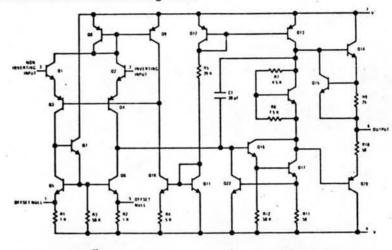
The LM741 and LM741C are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

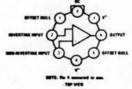
The offset voltage and offset current are guaranteed over the entire common mode range. The amplifiers also offer many features which make

their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

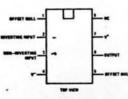
The LM741C is identical to the LM741 except that the LM741C has its performance guaranteed over a 0°C to 70°C temperature range, instead of -55°C to 125°C.

schematic and connection diagrams

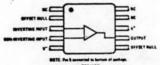




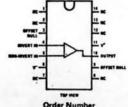
Order Number LM741H or LM741CH



Order Number LM741CN See Package 20



Order Number LM741F See Package 3



LM741CD or LM741CN-14 See Package 1 See Package 22

2-173

absolute maximum ratings

electrical characteristics (Note 3)

	PARAMETER	CONDITIONS	1	LM741			LM7410		STEET TO STEET OF THE	
	2000/2007/2007	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	
	Input Offset Voltage	TA = 25°C, R ₅ ≤ 10 kΩ		1.0	5.0		1.0	6.0	mV	
	Input Offset Current	TA - 25°C		30	200		30	200	nA	
	Input Bias Current	TA - 25°C		200	500		200	500	nA	
	Input Resistance	TA - 25°C	0.3	1.0	2	0.3	1.0	200	мΩ	
-	Supply Current	TA - 25°C, Vs - ±15V		1.7	2.8	S7403	1.7	2.8	mA.	
	Large Signal Voltage Gain	TA - 25°C, V5 - ±15V				nega i				
	100 - 2000 Val	$V_{OUT} = ±10V, R_L \ge 2 k\Omega$	50	160		25	160		V/mV	
	Input Offset Voltage	$R_S \le 10 k\Omega$			6.0			7.5	mV	
	Input Offset Current				500		1 6	300	nA	
	Input Bias Current				1.5			0.8	μΑ	
	Large Signal Voltage Gain	$V_{S} = ±15V, V_{OUT} = ±10V$ $R_{L} \ge 2 k\Omega$	25	-		15			1.5.4	
	Output Voltage Swins		(CE: 1			- 175 A.A.			V/mV	
		V _S = ±15V, R _L = 10 kΩ R _L = 2 kΩ	±12 ±10	±14 ±13		±12 ±10	±14 ±13		Ÿ	
	Input Voltage Range	Vs - ±15V	±12			:12		- 3	Ţ	
	Common Mode	colora de Cont	-20002							
	Rejection Ratio	$R_S \le 10 \text{ k}\Omega$	70	90		70	90		dB	
	Supply Voltage	R ₅ < 10 kΩ								
	Rejection Ratio		77	96	- 1	77	96	- 1	dB	

Note 1: The maximum junction temperature of the LM741 is 150°C, while that of the LM741C is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to case.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for V_S = ±15V and -55°C \leq T_A \leq 125°C, unless otherwise specified. With the LM741C, however, all specifications are limited to 0°C \leq T_A \leq 70°C and V_S =±15V.



Interface Circuits

LM710C voltage comparator

general description

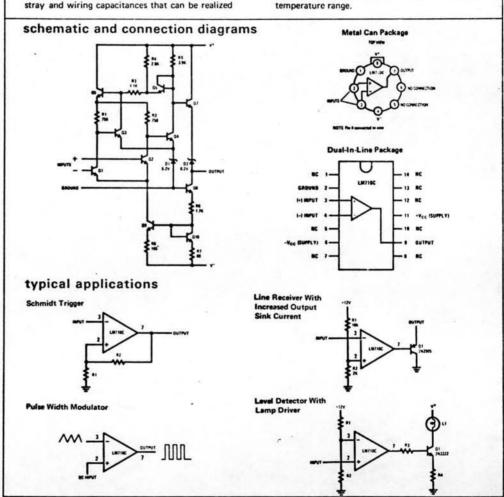
The LM710C is a high-speed voltage comparator intended for use as an accurate, low-level digital level sensor or as a replacement for operational amplifiers in comparator applications where speed is of prime importance. The circuit has a differential input and a single-ended output, with saturated output levels compatible with practically all types of integrated logic.

The device is built on a single silicon chip which insures low offset and thermal drift. The use of a minimum number of stages along with minority-carrier lifetime control (gold doping) makes the circuit much faster than operational amplifiers in saturating comparator applications. In fact, the low stray and wiring capacitances that can be realized

with monolithic construction make the device difficult to duplicate with discrete components operating at equivalent power levels.

The LM710C is useful as a pulse height discriminator, a voltage comparator in high-speed A/D converters or a go, no-go detector in automatic test equipment. It also has applications in digital systems as an adjustable-threshold line receiver or an interface between logic types. In addition, the low cost of the unit suggests it for applications replacing relatively simple discrete component circuitry.

The LM710C is the commercial/industrial version of the LM710. It is identical to the LM710 except that operation is specified over a 0°C to 70°C temperature range.



absolute maximum ratings

14.0V Positive Supply Voltage -7.0V Negative Supply Voltage ±5.0V Differential Input Voltage Input Voltage ±7.0V 300 mW Power Dissipation (Note 1) **Output Short Circuit Duration** 10 sec 0°C to 70°C Operating Temperature Range -65°C to +150°C Storage Temperature Range 300°C Lead Temperature (Soldering, 10 sec)

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	T _A = 25°C, R _S <200Ω V _{OUT} = 1.4V		1.6	5.0	mV ·
Input Offset Current	TA = 25°C, Vout = 1.4V		1.8	5.0	μΑ
Input Bias Current	TA - 25°C		16	25	μА
Voltage Gain	TA = 25°C	1000	1500		
Output Resistance	TA = 25°C		200		Ω
Output Sink Current	T _A = 25°C, ΔV _{IN} ≥5 mV V _{OUT} = 0	1.7	2.5		mA
Response Time			40		ns
(Note 3)					
Input Offset Voltage	R ₅ ≤200Ω			6.5	mV
Average Temperature	0°C≤T_4≤70°C	3			
Coefficient of Input	R _s ≤50Ω		5.0	20	µV/
Offset Voltage					
Input Offset Current				7.5	μА
Average Temperature	25°C≤T _A ≤70°C		15	50	nA/°
Coefficient of Input	0°C≤T _A ≤25°C		24	100	na/
Offset Current					
Common Mode Rejection Ratio	R _S ≤ 200Ω	70	98		
Input Bias Current	TA = 0°C		25	40	μA
Input Voltage Range	V" = -7.0V	±5.0			٧
Differential Input Voltage Range .		±5.0			٧
Voltage Gain		800			
Positive Output Level	V _{IN} ≥ 5 mV, 0 ≤ l _{OUT} ≤ −5 mA	2.5	3.2	4.0	٧
Negative Output Level	V _{IN} ≤-10 mV	-1.0	-0.5	0	v
Output Sink Current	$V_{IN} \leq -10 \text{ mV}, V_{OUT} = 0$	0.5	200		mA
Positive Supply Current	V _{IN} ≤-10 mV		5.2	9	mA
Negative Supply Current			4.6	7.0	mA
Power Consumption				150	mW

Note 1: Ratings apply for ambient temperatures to 70°C . Note 2: These specifications apply for $V'=12.0V,\ V'=6.0V,\ 0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ and for a logic threshold voltage of 1.5V at 0°C , 1.4V at 25°C and 1.2V at 70°C unless otherwise specified.

Note 3: The response time specified (see definitions) is for a 100 mV input step with



Series 54/74

DM54121/DM74121(SN54121/SN74121) monostable multivibrator

general description

The DM54121/DM74121 TTL monostable multivibrator features DC triggering from positive or gated negative-going inputs with inhibit facility. Both positive and negative-going output pulses are provided with full fan-out to 10 normalized loads.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry for the B input allows jitter-free triggering from inputs with transition times as slow as 1V per second, providing the circuit with an excellent noise immunity of typically 1.2V. A high immunity to V_{CC} noise of typically 1.5V is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions on the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse lengths may be varied from 30 ns to 40 seconds by choosing appropriate timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} range for more than six decades of timing capacitance (10 pF to 10 μ F) and more than one decade of timing resistance

(2 k Ω to 40 k Ω). Throughout these ranges, pulse width is defined by the relationship $t_{p(OUT)} = C_T R_T \log_e 2$.

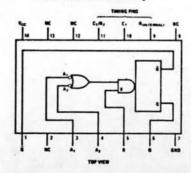
Duty cycles as high as 90% are achieved when using $R_{\rm T}$ = 40 $k\Omega.$ Higher duty cycles are achievable if a certain amount of pulse width jitter is allowed.

features

- Series 54/74 compatibility
- DC triggering
- Schmitt trigger inputs
- Positive-going or negative-going triggering
- Pulse width variation from 30 ns to 40 sec
- Pulse width virtually independent of V_{CC} and temperature
- Typical power dissipation
 90 mW (50% duty cycle)
 65 mW (Quiescent state)
- Output pulse width independent of input pulse width

connection diagram

Dual-In-Line and Flat Package



truth table

4	t INPUT			1 INP	UT	
Aı	A ₂	В	A	Az	8	OUTPUT
1	1	0	1	1	1	Inhibit
0	×	1	0	X	0	Inhibit
×	0	1	×	0	0	Inhibit
0	×	0	0	×	1	One Shot
×	0	0	X	0	1	One Shot
1	1	1	×	0	1	On Shot
1	1	1	0	×	1	One Shot
×	0	0	X	. 1	0	Inhibit
0	×	0	1	×	0	Inhibit
×	0	1	1	1	1	Inhibit
0	X	1	1	1	1	Inhibit
1	1	0	X	0	0	Inhibit
1	1	0	0	X	0	Inhibit

NOTES:

La * Time before input transition

La 1 * Time after input transition

1.75

absolute maximum ratings (Note 1)

 Vcc
 7.0v

 Input Voltage
 5.5v

 Operating Temperature Range
 DM54121
 -55°C to +125°C

 DM74121
 0°C to >75°C

 Storage Temperature Range
 -85°C to +150°C

 Lead Temperature (Soldering, 10 sec)
 300°C

electrical characteristics (Note 2)

PARAMETER				1	LIMITS (No	te 2)	h. Koxes
FAILAMETER		CUN	DITIONS	MIN	TYP	MAX	UNITS
Positive-Going Threshold Voltage at	DM54121	V _{CC} = 4.5V		_		+	1
A Input, V _T .	DM74121	Vcc = 4.75V		1	1.4	2	٧
Negative Going Threshold Voltage at	DM54121	Vcc = 4.5V		10000	1000		
A Input, V _T _	DM74121	Vcc = 4.75V		0.8	- 1.4		v
Positive-Going Threshold Voltage at	DM54121	Vcc = 4.5V				4	
B Input, V _{T+}	DM74121	V _{CC} = 4.75V			1.55	2	v
Negative-Going Threshold Voltage at	DM54121	Vcc = 4.5V			10000		
B Input, V _T _	DM74121	V _{CC} = 4.75V		0.8	1.35		٧
Logical "0" Output Voltage, Vou Troi	DM54121	V _{CC} = 4.5V	ALL THE OWN STATE WAS		10000000		
cogical o output voltage, voution	DM74121	V _{CC} = 4.75V	ISINK = 16 mA	1	0.23	0.4	٧
Logical "1" Output Voltage, Vout(1)	DM54121	Vcc = 4.5V					
Coupat Voltage, Vout(1)	DM74121	Vcc = 4.75V	ILOAD = -400 μA	2.4	3.3	1	٧
Logical "0" Level Input Current at	DM54121	Vcc = 5.5V	744 5372 513			Tarata V	- 00
A1 or A2, I _{IN(0)}	DM74121	V _{CC} = 5.25V	VIN - 0.4V		-1	-1.6	mA
Logical "0" Level Input Current	DM54121	V _{CC} = 5.5V					
at B, I _{IN(0)}	DM74121	V _{CC} = 5.25V	VIN - 0.4V		-2	-3.2	mA
Logical "1" Level Input Current at	DM54121	Vcc = 5.5V	VIN = 2.4V		1.5	40	
A1 or A2, I _{IN(1)}	DM74121	V _{CC} = 5.25V	VIN = 5.5V		0.02	1 40	μA mA
Logical "1" Level Input Current	DM54121	V _{cc} = 5.5V	V _{IN} = 2.4V		3	80	μΑ
et B, I _{IN(1)}	DM74121	V _{CC} = 5.25V	VIN = 5.5V		0.05	1	mA.
Short Circuit Output Current at Q or	DM54121	Vcc = 5.5V		-20	\$11WEE22	-55	mA
D, l _{OS} (Note 3)	DM74121	V _{cc} = 5.25V		-18		-55	mA
Power Supply Current in Quiescent	DM54121	Vcc * 5.5V					
(Unfired) State, I _{CC}	DM74121	Vcc = 5.25V			13	25	mA
Power Supply Current in	DM54121	Vcc = 55V			local c		
Fired State, I _{CC}	DM74121	V _{CC} = 5.25V			23	40	mA

	C _L = 15 pF, C _T = 80 pF, R _T = Internal	15	25	55	ns	
	C _L = 15 pF, C _T = 80 pF, R _T = Internal	25	34	70	ns	
	C _L = 15 pF, C _T = 80 pF	20	32	65	ns	
	C _L = 15 pF, C _T = 80 pF	30	39	80	ns	
	C _L = 15 pF, C _T = 80 pF, R _T = Open, Pin 9 to V _{CC}	70	110	150	ns	
	C _L = 15 pF, C _T = 0, R _T = Open, Pin 9 to V _{CC}	17	23	50	ns	
	C _L = 15 pF, C _T = 100 pF, R _T = 10 kΩ, Pin 9 Open	600	700	800	ns	
	C _L = 15 pF, C _T = 1 μF, R _T = 10 kΩ, Pin 9 Open	6	7	8	ms	
mum Duration of Trigger Pulse, tHOLD	C _L = 15 pF, C _T = 80 pF, R _T = Open, Pin 9 to V _{CC}		22	50	ns	
	pagation Delay Time to Logical "1" Level in 8 Input to Q Output, t _{pot1} pagation Delay Time to Logical "1" Level in A1/A2 Inputs to Q Output, t _{pot1} pagation Delay Time to Logical "0" Level in 8 Input to Q Output, t _{pot0} in 8 Input to Q Output, t _{pot0} pagation Delay Time to Logical "0" Level in A1/A2 Inputs to Q Output, t _{pot0} pagation Delay Time to Logical "0" Level in A1/A2 Inputs to Q Output, t _{pot0} pagation Delay Time to Logical "0" Level in A1/A2 Inputs to Q Output, t _{pot0} pagation Delay Time to Logical "0" Level in A1/A2 Inputs to Q Output, t _{pot0} pagation Delay Time to Logical "0" Level in A1/A2 Inputs to Q Output, t _{pot0} pagation Pagat	n 8 Input to Q Output, t _{pot1} Pagation Delay Time to Logical "1" Level n A1/A2 Inputs to Q Output, t _{pot1} R _T = Internal C _L = 15 pF, C _T = 80 pF, R _T = Internal C _L = 15 pF, C _T = 80 pF R _T = Internal C _L = 15 pF, C _T = 80 pF C _L = 15 pF, C _T = 80 pF C _L = 15 pF, C _T = 80 pF C _L = 15 pF, C _T = 80 pF C _L = 15 pF, C _T = 80 pF C _L = 15 pF, C _T = 80 pF C _L = 15 pF, C _T = 80 pF C _L = 15 pF, C _T = 80 pF C _L = 15 pF, C _T = 80 pF C _L = 15 pF, C _T = 80 pF R _T = Open, Pin 9 to V _{CC} C _L = 15 pF, C _T = 0, R _T Open, Pin 9 to V _{CC} C _L = 15 pF, C _T = 0 R _T = 10 kΩ, Pin 9 Open C _L = 15 pF, C _T = 10 pF, R _T = 10 kΩ, Pin 9 Open C _L = 15 pF, C _T = 10 pF R _T = 10 kΩ, Pin 9 Open C _L = 15 pF, C _T = 1 μF, R _T = 10 kΩ, Pin 9 Open C _L = 15 pF, C _T = 80 pF C _L = 15 pF, C _T = 10 pF, R _T = 10 kΩ, Pin 9 Open C _L = 15 pF, C _T = 1 μF, R _T = 10 kΩ, Pin 9 Open C _L = 15 pF, C _T = 80 pF	n 8 Input to Q Output, t _{po1} segation Delay Time to Logical "1" Level n A1/A2 Inputs to Q Output, t _{po1} segation Delay Time to Logical "0" Level n B Input to Q Output, t _{po1} segation Delay Time to Logical "0" Level n A1/A2 Inputs to Q Output, t _{po0} segation Delay Time to Logical "0" Level n A1/A2 Inputs to Q Output, t _{po0} segation Delay Time to Logical "0" Level n A1/A2 Inputs to Q Output, t _{po0} segation Delay Time to Logical "0" Level n A1/A2 Inputs to Q Output, t _{po0} segation Delay Time to Logical "0" Level n A1/A2 Inputs to Q Output, t _{po0} segation Delay Time to Logical "0" Level n A1/A2 Inputs to Q Output, t _{po0} segation Delay Time to Logical "0" Level n A1/A2 Inputs to Q Output, t _{po0} segation Delay Time to Logical "0" Level n A1/A2 Inputs to Q Output, t _{po0} Ct = 15 pF, Ct = 80 pF To Qpen, Pin 9 to V _{CC} Ct = 15 pF, Ct = 100 pF, Rt = 10 kΩ, Pin 9 Open Ct = 15 pF, Ct = 1 μF, Rt = 10 kΩ, Pin 9 Open Ct = 15 pF, Ct = 80 pF, To Qpen, Pin 9 Open Ct = 15 pF, Ct = 1 μF, Rt = 10 kΩ, Pin 9 Open Ct = 15 pF, Ct = 80 pF, Ct = 15 pF,	n 8 Input to Q Output, t _{pd1} Pagation Delay Time to Logical "1" Level of A1/A2 Inputs to Q Output, t _{pd1} Regation Delay Time to Logical "0" Level of B Input to Q Output, t _{pd1} Regation Delay Time to Logical "0" Level of B Input to Q Output, t _{pd2} Regation Delay Time to Logical "0" Level of B Input to Q Output, t _{pd2} Regation Delay Time to Logical "0" Level of A1/A2 Inputs to Q Output, t _{pd2} Regation Delay Time to Logical "0" Level of A1/A2 Inputs to Q Output, t _{pd2} Regation Delay Time to Logical "0" Level of A1/A2 Inputs to Q Output, t _{pd2} Regation Delay Time to Logical "0" Level of Logical "0" Level of A1/A2 Inputs to Q Output, t _{pd2} Regation Delay Time to Logical "0" Level of Logical "0" Level	A line of the policy of the po	AT = Internal CL = 15 pF, CT = 80 pF, RT = Internal CL = 15 pF, CT = 80 pF, RT = Internal CL = 15 pF, CT = 80 pF AT = Internal CL = 15 pF, CT = 80 pF AT = Internal CL = 15 pF, CT = 80 pF CL = 15 pF, CT = 80 pF AT = Internal CL = 15 pF, CT = 80 pF CL = 15 pF, CT = 80 pF AT = Internal CL = 15 pF, CT = 100 pF AT = Internal CL = 15 pF, CT = 100 pF AT = Internal CL = 15 pF, CT = 100 pF AT = Internal CL = 15 pF, CT = 100 pF AT = Internal CL = 15 pF, CT = 100 pF AT = Internal CL = 15 pF, CT = 100 pF AT = Internal CL = 15 pF, CT = 100 pF AT = Internal CL = 15 pF, CT = 100 pF AT = Internal CL = 15 pF, CT = 100 pF AT = Internal CL = 15 pF, CT = 100 pF AT = Internal CL = 15 pF, CT = 100 pF AT = Internal AT = Internal CL = 15 pF, CT = 100 pF AT = Internal CL = 15 pF, CT = 100 pF AT = Internal CL = 15 pF, CT = 100 pF AT = Internal CL = 15 pF, CT = 100 pF AT = Internal CL = 15 pF, CT = 100 pF AT = Internal CL = 15 pF, CT = 100 pF AT = Internal CL = 15 pF, CT = 100 pF AT = Internal AT = Internal CL = 15 pF, CT = 80 pF AT = Internal AT = Internal CL = 15 pF, CT = 80 p

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannobe guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these immir. The table of "Electrical Characteristics" provides conditions.

Note 2: Unless otherwise specified minimax limits apply across the -55°C to +125°C temperature range for the DM54121 and across the 0°C to 70°C range for the DM74121. All typicals are given for VCC = 5.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted





Series 54/74

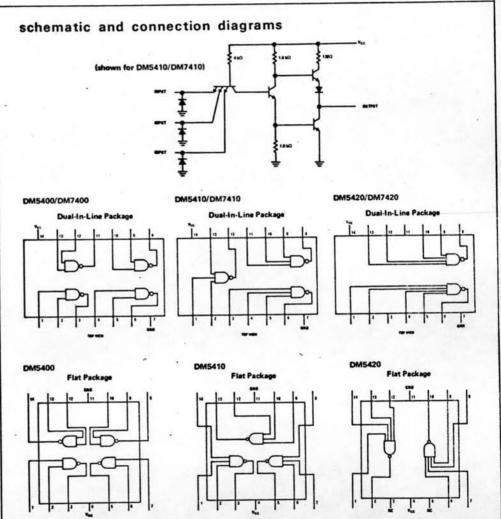
DM5400/DM7400(SN5400/SN7400) quadruple 2-input NAND gate DM5410/DM7410(SN5410/SN7410) triple 3-input NAND gate DM5420/DM7420(SN5420/SN7420) dual 4-input NAND gate general description

Employing TTL (Transistor-Transistor-Logic) to achieve high speed at moderate power dissipation, these gates provide the basic functions used in the implementation of digital integrated circuit systems. Characteristics of the circuits include high noise immunity, low output impedance, good capacitive drive capability, and minimal variation in switching times with temperature. The gates are compatible with and interchangeable with Series 54/74 equivalent.

features

- Typical Noise Immunity 17 400 mV Guaranteed Noise Immunity 10
- Fan Out
- 13 ns Average Propagation Delay

10 mW per gate Average Power Dissipation



absolute maximum ra	tings	operating cor	ndition	S	
			MIN	MAX	UNITS
Van	7.0V	Supply Voltage (VCC)			
VCC Input Voltage	5.5V	DM54XX	4.5	5.5	V
Storage Temperature Range	-65°C to +150°C	DM74XX	4.75	5.25	V
Fan-Out .	10	Temperature (TA)			
Lead Temperature (Soldering, 10 sec)	300°C	DM54XX	-55	+125	°c
		DM74XX	0	70	°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Diode Clamp Voltage	V _{CC} = 5.0V, T _A = 25°C, I _{IN} = -12 mA			-1.5	٧
Logical "1" Input Voltage	V _{CC} = Min	2.0			V.
Logical "0"	V _{CC} = Min			0.8	v
Logical "1" Output Voltage	V _{CC} = Min V _{IN} = 0.8V, I _{OUT} = -400 μA	2.4			v
Logical "0" Output Voltage	V _{CC} = Min V _{IN} = 2.0V, I _{OUT} = 16 mA			0.4	v
Logical "1" Input Current	V _{CC} = Max V _{IN} = 2.4V			40	μА
Logical "1" Input Current	V _{CC} = Max V _{IN} = 5.5V			1	m/A
Logical "0" Input Current	V _{CC} = Max V _{IN} = 0.4V			-1.6	m#
Output Short Circuit Current (Note 2)	V _{CC} = Max V _{IN} = 0V, V ₀ = 0V DM74XX DM54XX	-20 -18		-55 -57	m#
Supply Current— Logical "0" (Note 3)	V _{CC} = Max V _{IN} = 5.0V		3	5.1	m.
Supply Current— Logical "1" (Note 3)	V _{CC} = Max V _{IN} = 0V		1	1.8	m
Propagation Delay Time to Logical "0", tpd0	V _{CC} = 5.0V, T _A = 25°C, C = 50 pF		8	15	ns
Propagation Delay Time to Logical "1", t _{pd 1}	V _{CC} = 5.0V, T _A = 25°C, C = 50 pF		13	25	ns

Note 1: Unless otherwise specified min/max limits apply across the -55°C to +125°C temperature range for the DM54XX and across the 0°C to 70°C range for the DM74XX. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 2: Not more than 1 output should be shorted at a time.

Note 3: Each gate.



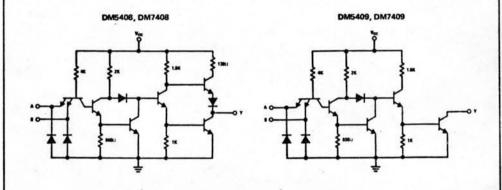
Series 54/74

DM5408/DM7408(SN5408/SN7408) quad 2-input AND gate DM5409/DM7409(SN5409/SN7409) quad 2-input AND gate (open collector)

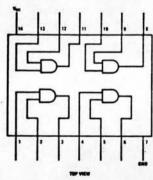
general description

The DM5408/DM7408 and DM5409/DM7409 provide the non-inverting AND function in the popular quad 2-input pin configuration.

schematic and connection diagrams







absolute maximum	ratings (Note 1)	operating cor	nditio	ns	
Supply Voltage	7V		MIN	MAX	UNITS
Input Voltage	5.5V	Supply Voltage(VCC)			
Output Voltage	5.5V	DM5408. DM5409	4.5	5.5	V
Storage Temperature Range Lead Temperature (Soldering, 10 sec)	-65°C to +150°C 300°C	DM7408, DM7409	4.75	5.25	v
crea remperature tooldering, reserv		Temperature (TA)			
		DM5408, DM5409	-55	+125	‡C
		DM7408, DM7409	0	70	°C

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V _{CC} = Min	2			٧
Logical "0" Input Voltage	V _{CC} = Min			0.8	v
Logical "1" Output DM5408 Voltage DM7408	V_{CC} = Min, V_{IN} = 2V, I_{OUT} = -800 μ A	2.4			v
Logical "1" Output DM5409 DM7409	V _{CC} = Min, V _{OUT} = 5.5V, V _{IN} = 2.0V			250	μА
Logical "0" Output Voltage	V _{CC} = Min, V _{IN} = 0.8V, I _{OUT} = 16 mA			0.4	V
Logical "1" Input Current	V _{CC} = Max, V _{IN} = 2.4V			40	μА
	V _{CC} = Max, V _{IN} = 5.5V			1	mA
Logical "0" Input Current	V _{CC} = Max, V _{IN} = 0.4V			-1.6	mA
Output Short Circuit Current (Note 3)	V _{CC} = Max DM5408 DM7408	-20 -18		-55 -55	mA
Supply Current — Logical "1" (each device)	V _{CC} = Max, V _{IN} = 5V		11	21	mA
Logical "O"	V _{CC} = Max, V _{IN} = 0V	-	20	33	mA
Input Clamp Voltage	$V_{CC} = 5.0V$, $T_A = 25^{\circ}C$, $I_{IN} = -12 \text{ mA}$		-1.0	-1.5	V
Propagation Delay to a Logical "0" from DM5408/DM7408 Any Input to Output, t _{pd0}	V _{CC} = 5.0V T _A = 25°C		14	19	ns
Propagation Delay to a Logical "0" from DM5409/DM7409 Any Input to Output, t _{pd0}	V _{CC} = 5.0V T _A = 25°C	4.8	15	24	ns
Propagation Delay to a Logical "1" from DM5408/DM7408 Any Input to Output, t _{pd1}	V _{CC} = 5.0V T _A = 25°C		13	27	ns
Propagation Delay to a Logical "1" From DM5409/DM7409 Any Input to Output, t _{pd1}	V _{CC} = 5.0V T _A = 25°C		17	32	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the -55°C to +125°C temperature range for the DM5408, DM5409 and across the 0°C to 70°C range for the DM7408, DM7409. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Only one output at a time should be shorted.

YITA

Mr. Suphon Phoihiran attended the college of Engineering, Chulalongkorn University in 1963 where he received his Bachelor of Engineering (Electrical Communication Engineering) in 1968. After graduation he was appointed as the 1 class Electronic Engineer at the Communication Division, the Electricity Generating Authority of Thailand. From June 1972 to March 1977, he was admitted to take the "Nuclear Science and Technology" course at the Chulalongkorn University. Now he is working as the Electrical Engineer at The Siam Kraft Paper Co., Ltd.