CHAPTER II

CIRCUIT OPERATION

2.1 PREAMPLIFIER

The function of the preamplifier is used to match the high output impedance of the detector to the low impedance of the main amplifier. Input signal pulse from detector is fed through C_1 of Figure 2.1 to non-inverting input terminal of IC-1, that is connected as non-inverting amplifier which has a gain of unity. The output signal has a decay time constant of 50 μs. determined by the value of R_3 and C_3.

2.11 TEST PULSE

A voltage pulse can be inserted at the test input connector. A one volt input signal at the Test Pulse Connector produces an output pulse of approximately 135 mV. The shape of the voltage test pulse should have a fast rise time (less than 10^{-8} sec.) followed by a slow exponential decay back to baseline (2 to 4×10^{-4} sec.).

2.2 AMPLIFIER

The main amplifier is the multistage amplifier which consists of five parts the circuits of which are shown in Fig. 2.2 to Fig. 2.6. This amplifier accepts either positive or negative input pulses to a maximum of 10 V. into 1000 ohms input impedance. IC-2 (Fig. 2.2) is the inverting

amplifier which inverts the negative to positive pulse. IC-3 (Fig. 2.3) a fixed gain (x 4) amplifier, with adjustable pole-zero cancellation accepts the signal from the inverting amplifier or positive input pulse from input connector mounted on the front panel. The rear panel Pos/Neg switch must be set to match the polarity of the input signals, while the output signal is always positive.

With 0.5 μs. or 2 μs. time constants the input pulses are shaped for a near optimum semi-Gaussian shape by active filter circuit shown in Fig. 2.5. Gain is continuously adjustable from x 12 to x 640 by the second stage amplifier Fig. 2.4. A switch mounted on the rear panel of the module selects either a positive unipolar output or a bipolar output with a positive leading portion. Fig. 2.6 is the power amplifier with gain about 3 and the output impedance is about 10 Ohms. This amplifier output is connected internally into the SCA and is also available through a front panel BNC connector.

2.3 SINGLE-CHANNEL ANALYZER

The amplifier output is internally connected to the SCA input, where it is buffered by IC-7 in Fig. 2.7. The output signal of IC-7 is dc-coupled to the lower level and window discriminators, IC-12 and IC-13 of Fig. 2.10, however this signal is dc-restored by BLR circuitry(Fig.2.7) consisting of comparator IC-8, Q5 and Q6. The lower-level reference voltage can be set either internally by the lower level control or externally from an external source by the switch mounted on the printed circuit and accessible through the left side panel of the module. The external lower level

can be furnished through a BNC connector marked EXT LTD at the rear panel. Window width is set by the front-panel 10-turn control for the full linear range of 0 to 1 volt or 0 to 10 volts above the lower level bias. The choice of window ranges is made with a slide switch mounted directly on the printed circuit.

The lower level bias is present at the non-inverting input of both the lower level and window discriminators. IC-12 and IC-13 are high again differential voltage comparators that function as discriminators operating in a biased amplifier mode. The non-inverting input is biased negative with respect to the inverting input. When an input pulse exceeds the bias threshold, the IC acts as a very high gain direct-coupled amplifier that generates an output for any input that just exceeds the bias threshold by a few millivolts. The inverting input of the lower level discriminator IC-12 is referenced to ground by the output of IC-11 so that the lower level discriminator will fire when the input signal exceeds the bias level at its non-inverting input. The inverting input of the window discriminator is referenced to the window control setting so that the window discriminator will trigger when the input signal exceeds the sum of the lower level and window control settings from IC-10.

The peak detection circuitry Fig. 2.9, consisting of Q8, Q9, Q10, Q11 and IC-18, is used to strobe the output of the lower level discriminator and window discriminator Fig. 2.10 when the amplifier output pulse has reached its peak. IC's 14, 15, 16 and 17 represent a logic circuitry used to generate output signal, approximately 0.5 μs. wide with 5 V amplitude rectangular logic pulse. If the amplifier output pulse is less than the

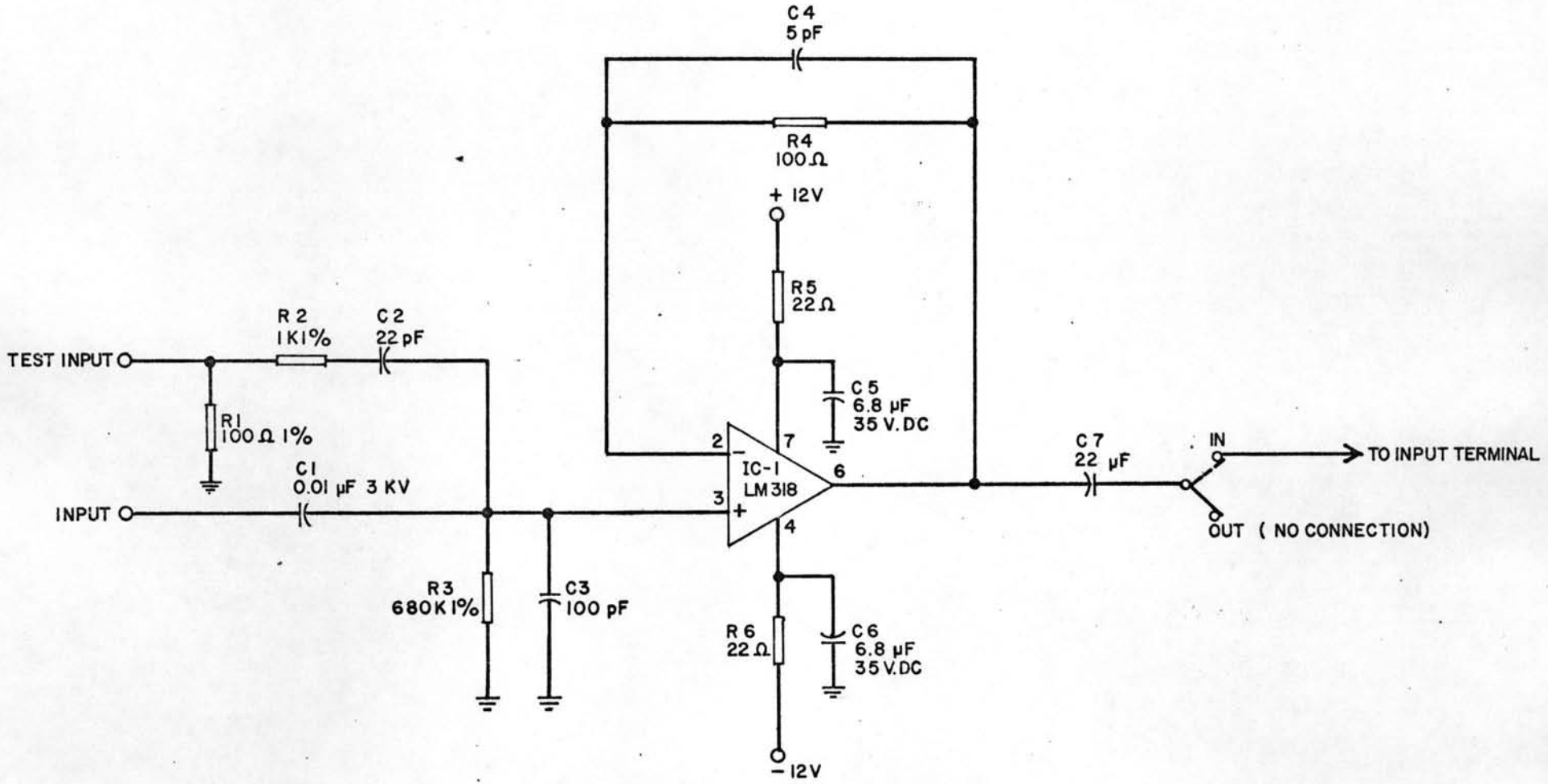
lower level setting, no analyzer output is generated. If the amplifier output pulse exceeds the lower level by an amount greater than the window width, the lower level and the window discriminators are triggered, the negative signal of IC-15 at pin 4 of IC-16 blocks the timing signal from IC-14 at pin 5 so that no analyzer output is generated.

Only if the amplifier output pulse peak falls within the analyzer window does the timing signal at pin 5 of IC-16 pass through the gate by the positive signal of IC-15.

A switch mounted on the rear panel of the module selects either differential or integral discriminator operation. If the switch is in the integral position, +5 V is fed to pin 4 of IC-16, and SCA functions as an integral discriminator.

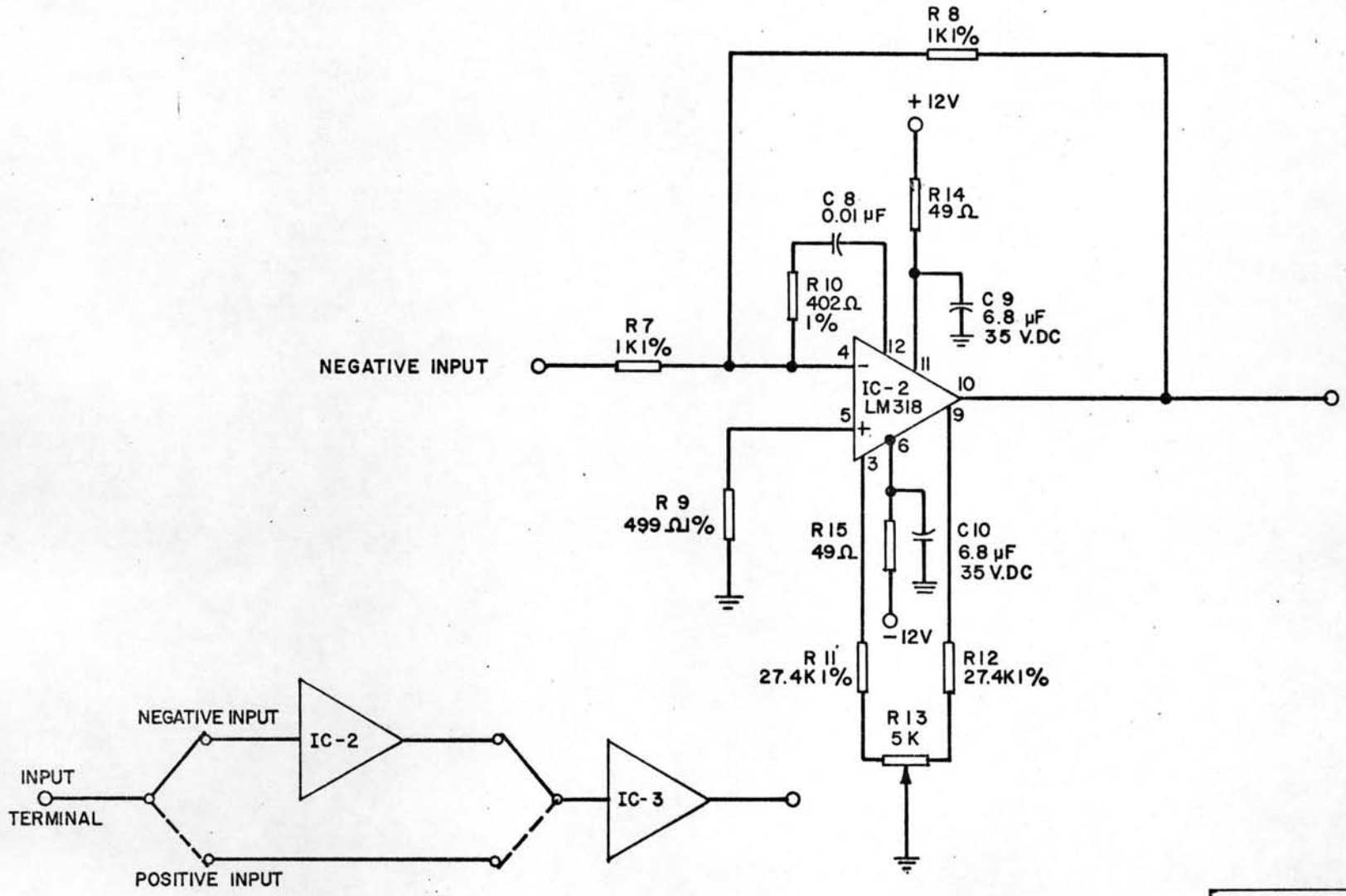
2.4 5V. REGULATED SUPPLY CIRCUIT

The 5V. regulated supply is used to provide regulated power supply for the integrated circuits used in the monostable unit and other digital circuitry.



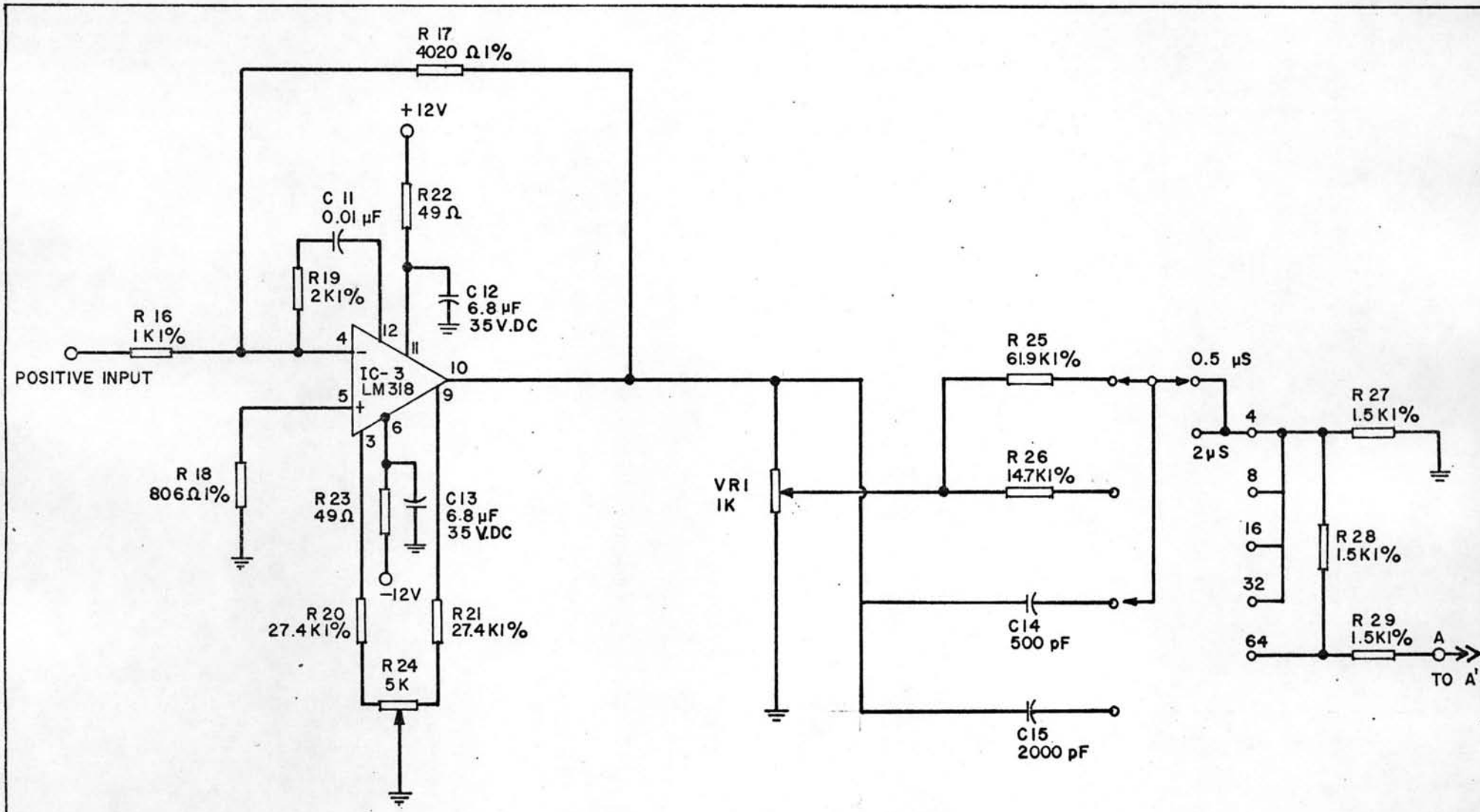
PRE AMPLIFIER CIRCUIT

FIGURE 2.1



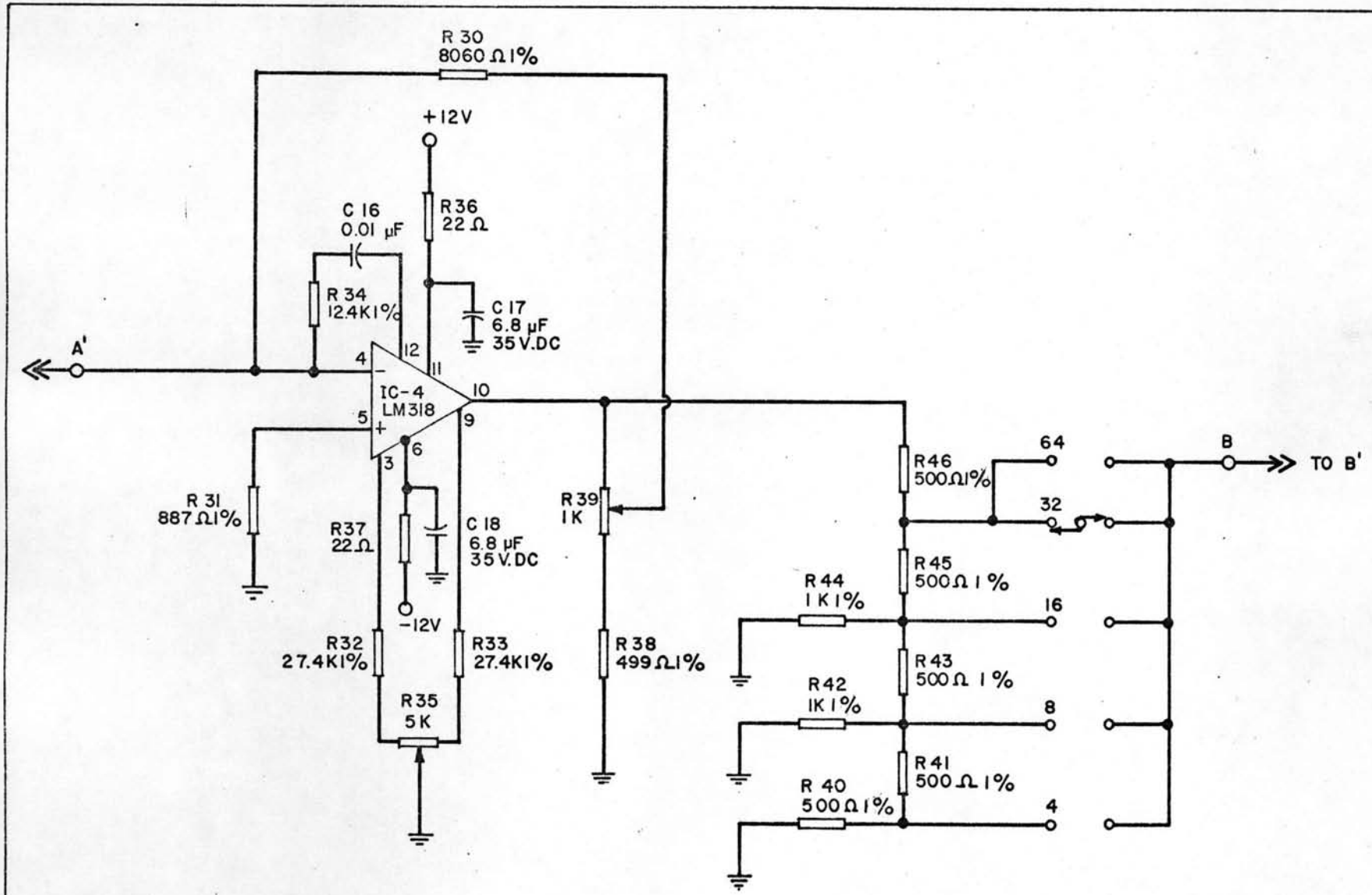
NEGATIVE INPUT CIRCUIT

FIGURE 2-2



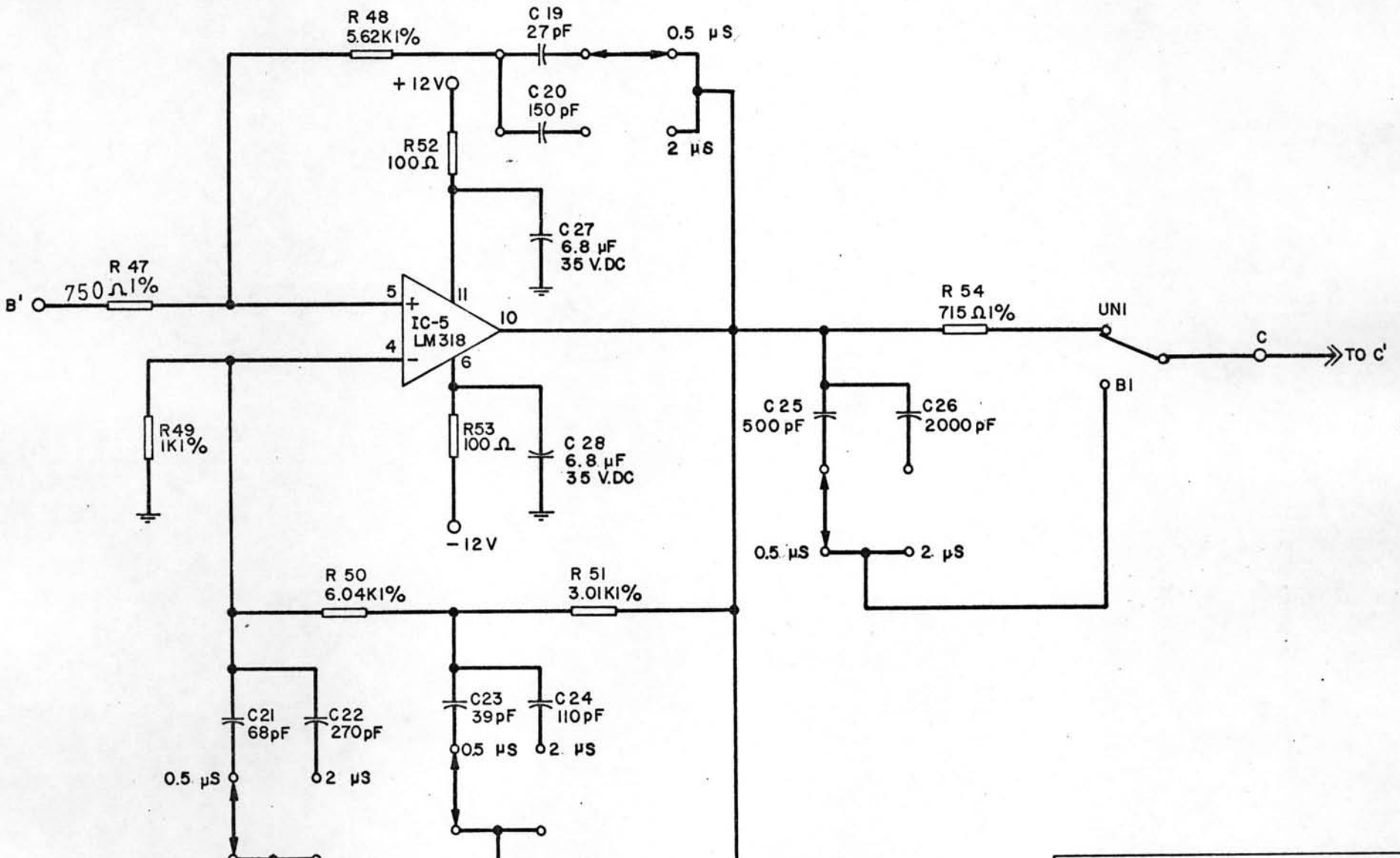
FIRST STAGE AMPLIFIER

FIGURE 2.3



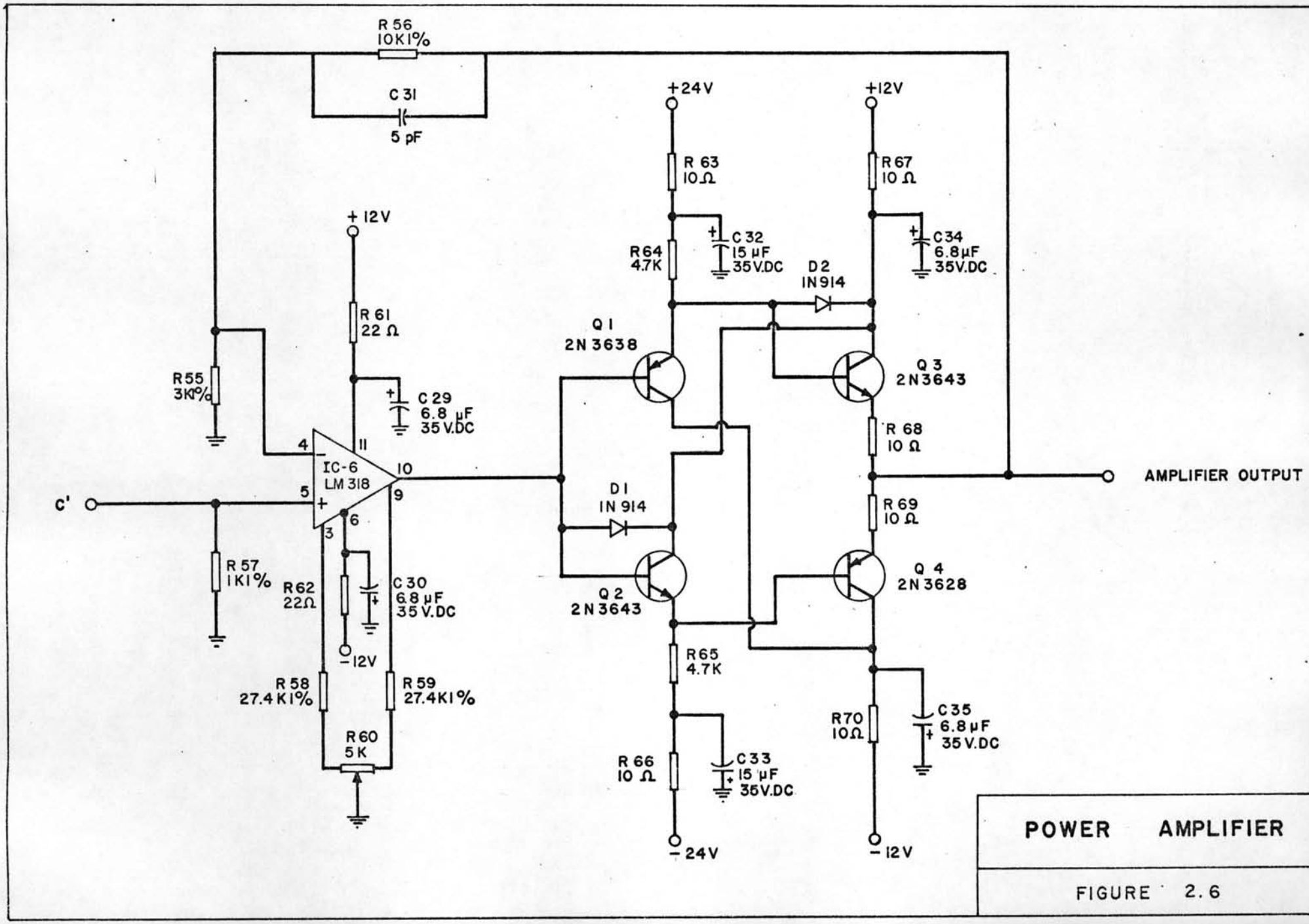
SECOND STAGE AMPLIFIER

FIGURE 2.4



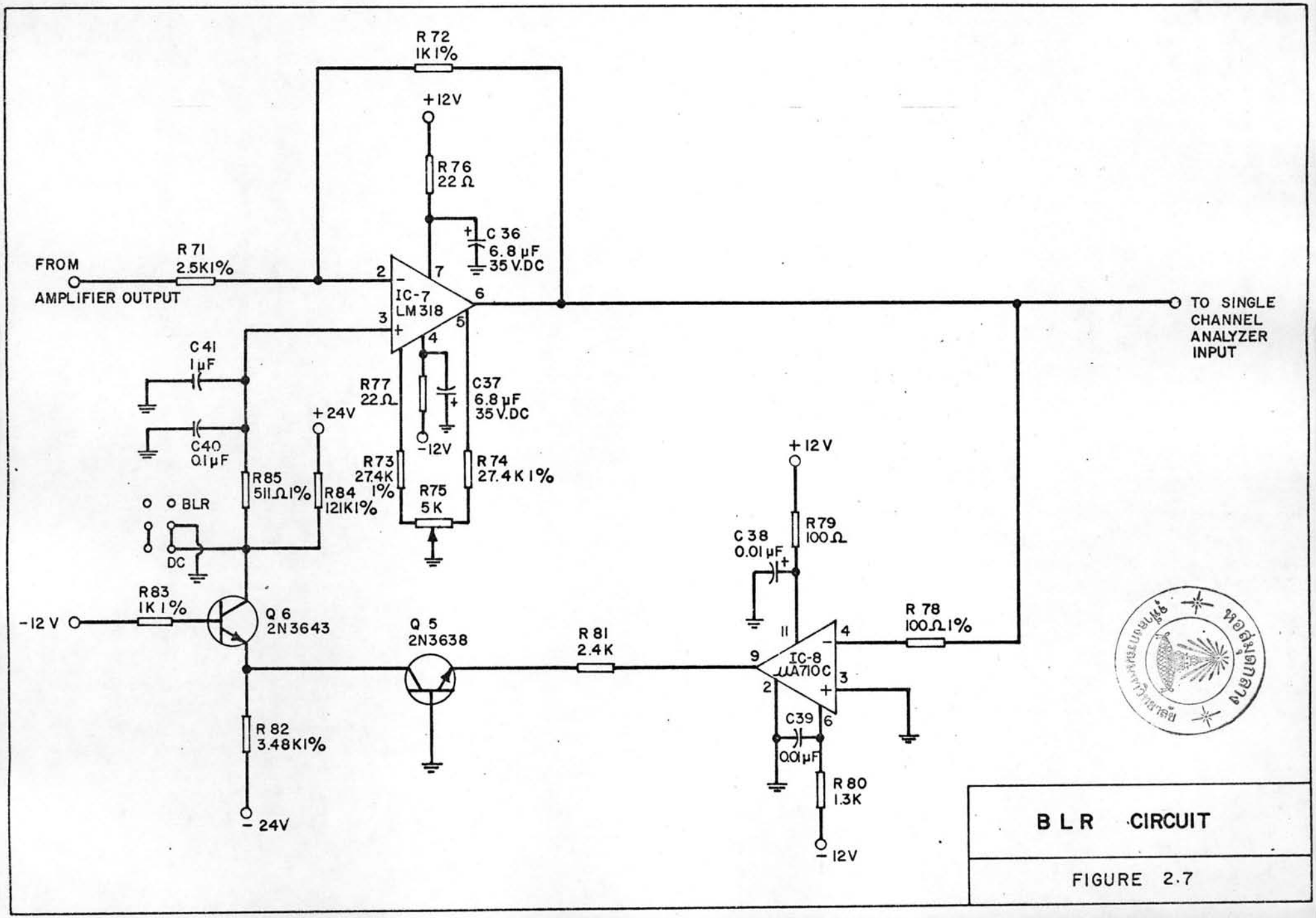
ACTIVE FILTER CIRCUIT

FIGURE 2.5



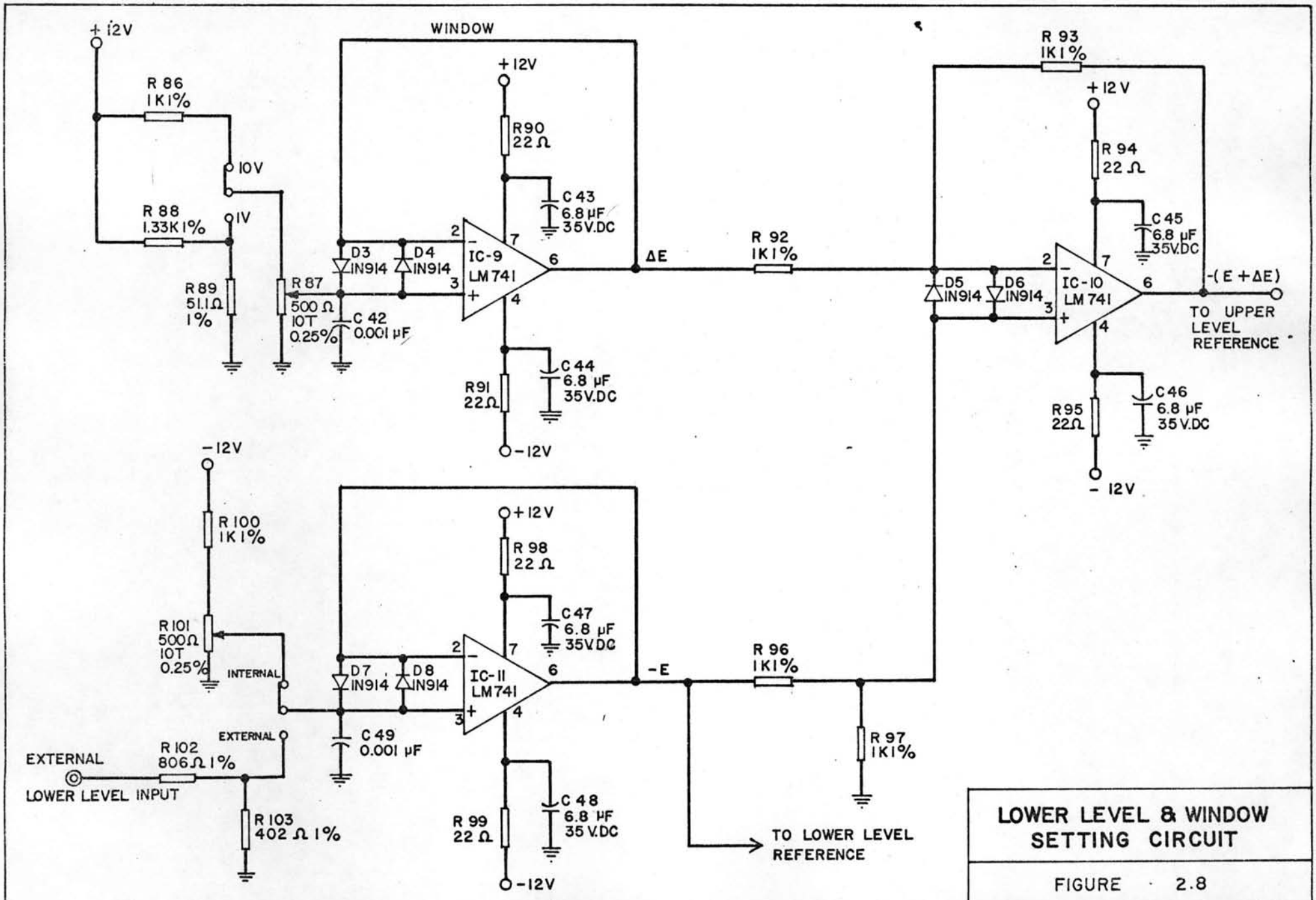
POWER AMPLIFIER

FIGURE 2.6



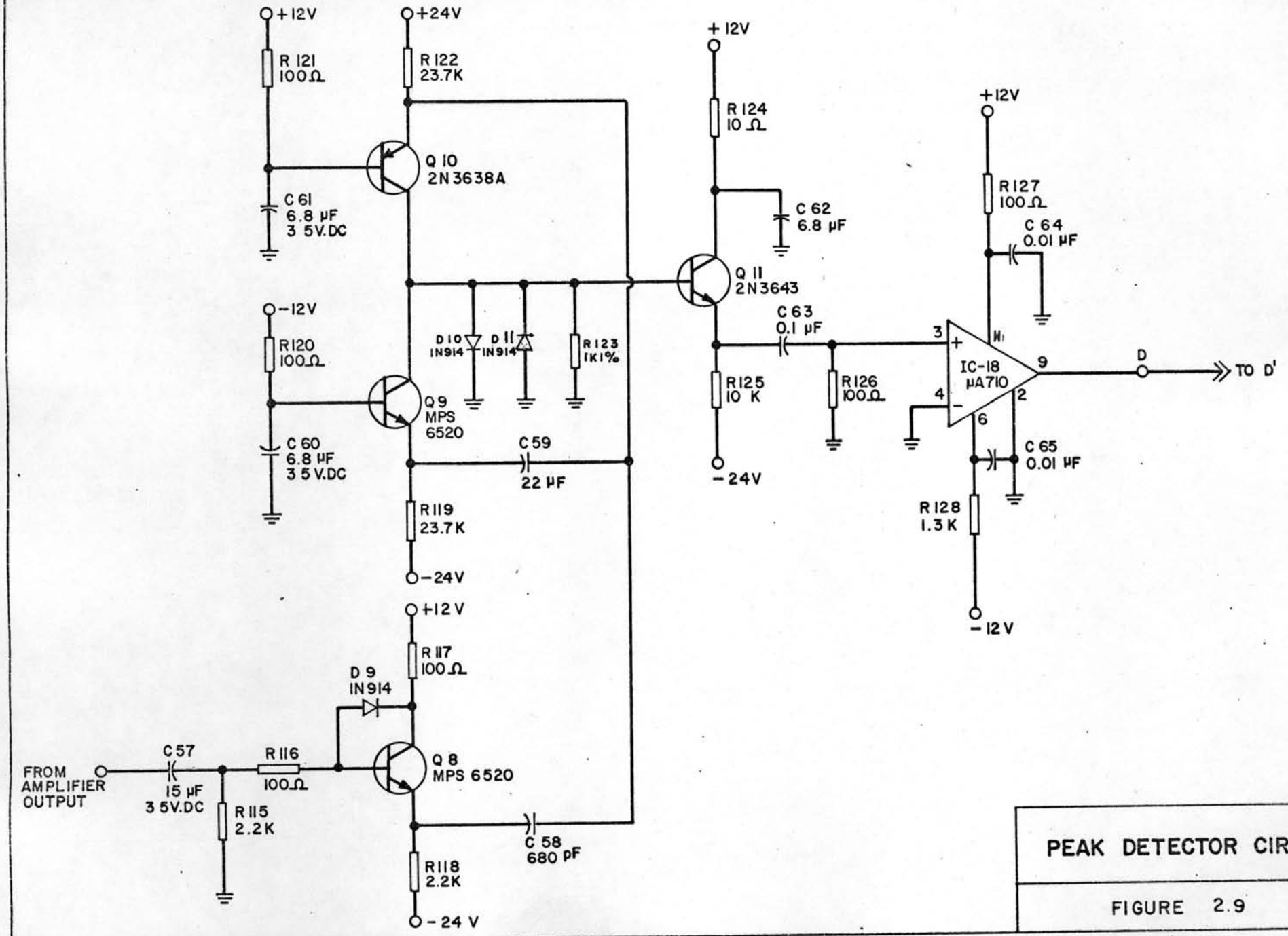
B L R CIRCUIT

FIGURE 2.7



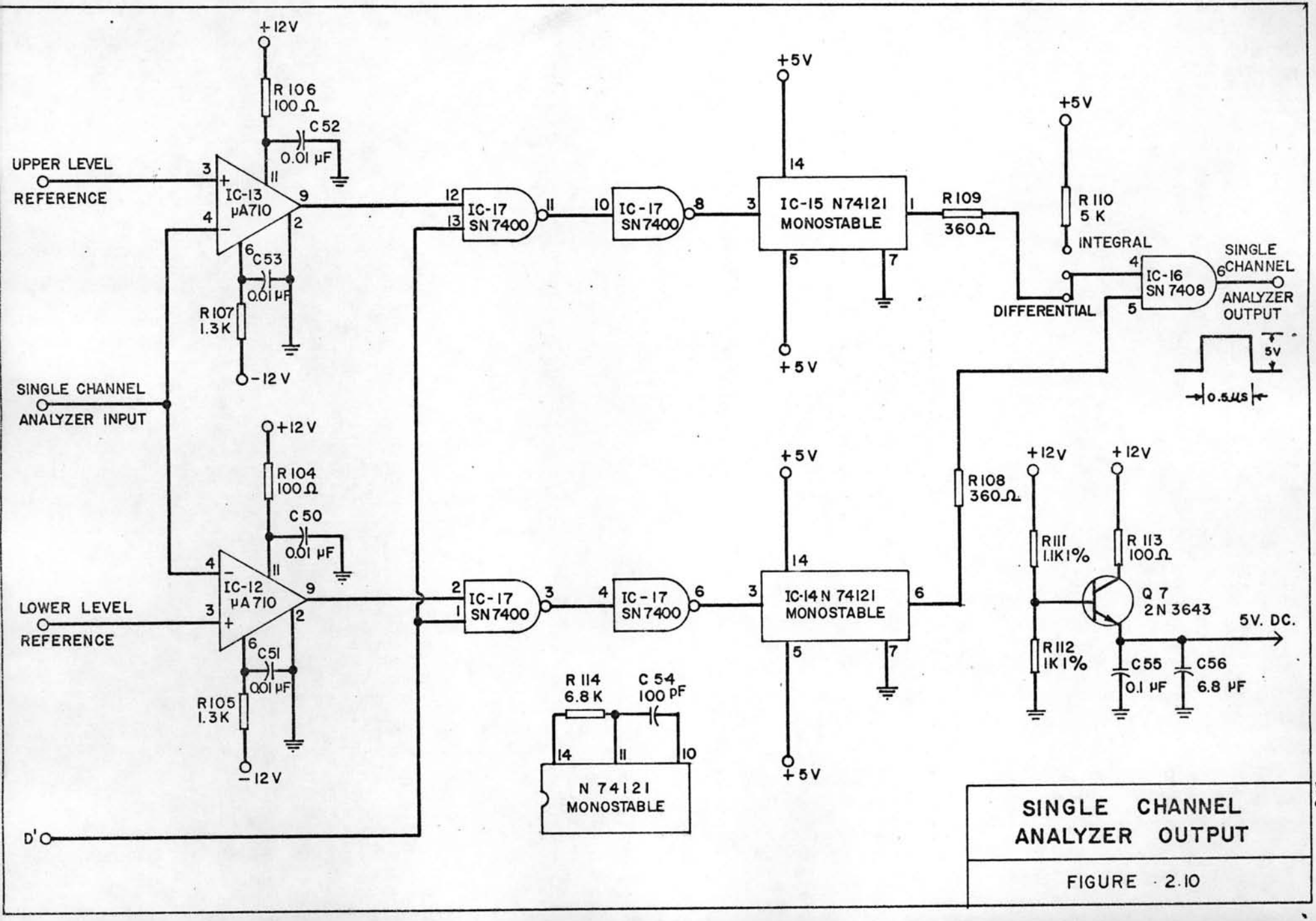
LOWER LEVEL & WINDOW SETTING CIRCUIT

FIGURE 2.8



PEAK DETECTOR CIRCUIT

FIGURE 2.9



SINGLE CHANNEL ANALYZER OUTPUT

FIGURE 2.10