CHAPTER IV

DESIGN AND CONSTRUCTION

4.1 Introduction

This chapter handles the fundamental function and composition of the overall instrument and each component assembly. Design and construction of the instrument will also be described in detail. In section 3.7 and **Fig.** 3-16 we have shown the block diagram and have described the operating principle of a digital AC power meter we are interested in. It is not difficult to design the circuits outlined by the block diagram. But in the construction step all circuit elements must be mounted on plug-in printed circuit cards. Then it is necessary to share some components among the assemblies. In the following sections the explanation will be given on circuit assemblies, shown bounded by hatching and marked by the symbols AS:1, AS:2, etc., in **Fig.** 4-1, and interconnections among the assemblies is shown in the same figure.

4.2 Fundamental Function of the Desired Instrument

Intented for use in power electronic field, the instrument has a function of measuring true RMS voltages and currents of distorted waveform, and single phase power, and displaying them digitally.

4.3 General Desired Specifications

Type of input : Floating

Display : LED display (with $4\frac{1}{2}$ digits)

Sampling rate : Approximately 3 times per second

Maximum reading : 19999 (effective reading maximum = 11000)

Range selection : Manual

Function selection : Manual

Unit marks : V, mA, A, mW, W, and kW

Effective measuring range : 30 to 100% of rated value

Power supply : 220 Vac $\pm$ 10%

MEASURING FUNCTION	VOLTAGE		CURRRENT		WATTAGE	
OPERATING PRINCIPLE	STEEPEST DESCENT METHOD		STEEPEST DESCENT METHOD		FEEDBACK TIME DIVISION	
	RANGE	EFFECTIVE MEASURING	RANGE	EFFECTIVE MEASURING	RANGE	EFFECTIVE MEASURING
MEASURING RANGE	3 V	1.000 ~ 3.300 V	0.1A	30.00 ~ 110.00 mA	30 mW to 18 kW	0 ~ 20kW
	10 V	3.000 ~ 11.000 V	0.3A	100.00 ~ 330.0 mA		
	30 V	10.000 ~ 33.00 V	1 A	300.0 ~ 110.00 mA		
	100 V	30.00 ~ 110.00 V	3 A	1.000 ~ 3.300 A		
	300 V	100.00 ~ 330.0 V	6 A	2.000 ~ 6.600 A		
	600 V	300.0 ~ 660.0 V	10 A	3.000 ~ 11.000 A		
	—	—	30 A	10.000 ~ 33.00 A		
RESOLUTION	1 mV/DIGIT		3 μA/DIGIT		0.3 mW/DIGIT	
FREQ. RANGE	DC,40 to 1,500 Hz		40 Hz to 1,500 Hz		40 Hz to 1,500 Hz	
ACCURACY EXPECTED	$\pm$0.5% OF READING		$\pm$0.5% OF READING		$\pm$0.5% OF READING AT COS ϕ = 1	

Table 4-1 General specifications

4.4 Printed Circuit Assembly and its Descriptions

According to Fig. 4-1, a desired instrument can be divided to 11 printed circuit assemblies which denote by AS:0 to AS:11. An assemblies list are as following.

(1) Measuring voltage divider (AS:0)

(2) Power supply-1 (AS:1) for analog zone

(3) V, A, W selector and alarm (AS:2)

(4) Preamplifier and ranging circuit (AS:3)

(5) Multiplier (AS:4)

(6) Power supply -2 (AS:5) for digital zone

(7) Control signal isolator (AS:6)

(8) A-to-D converter (AS:7)

(9) Point, unit, and ranging encoder -1 (AS:8) conventional type

(10) Point, unit, and ranging encoder -2 (AS:8) EPROM version

(11) Display (AS:9)

(12) Bypass transistors card (AS:10)

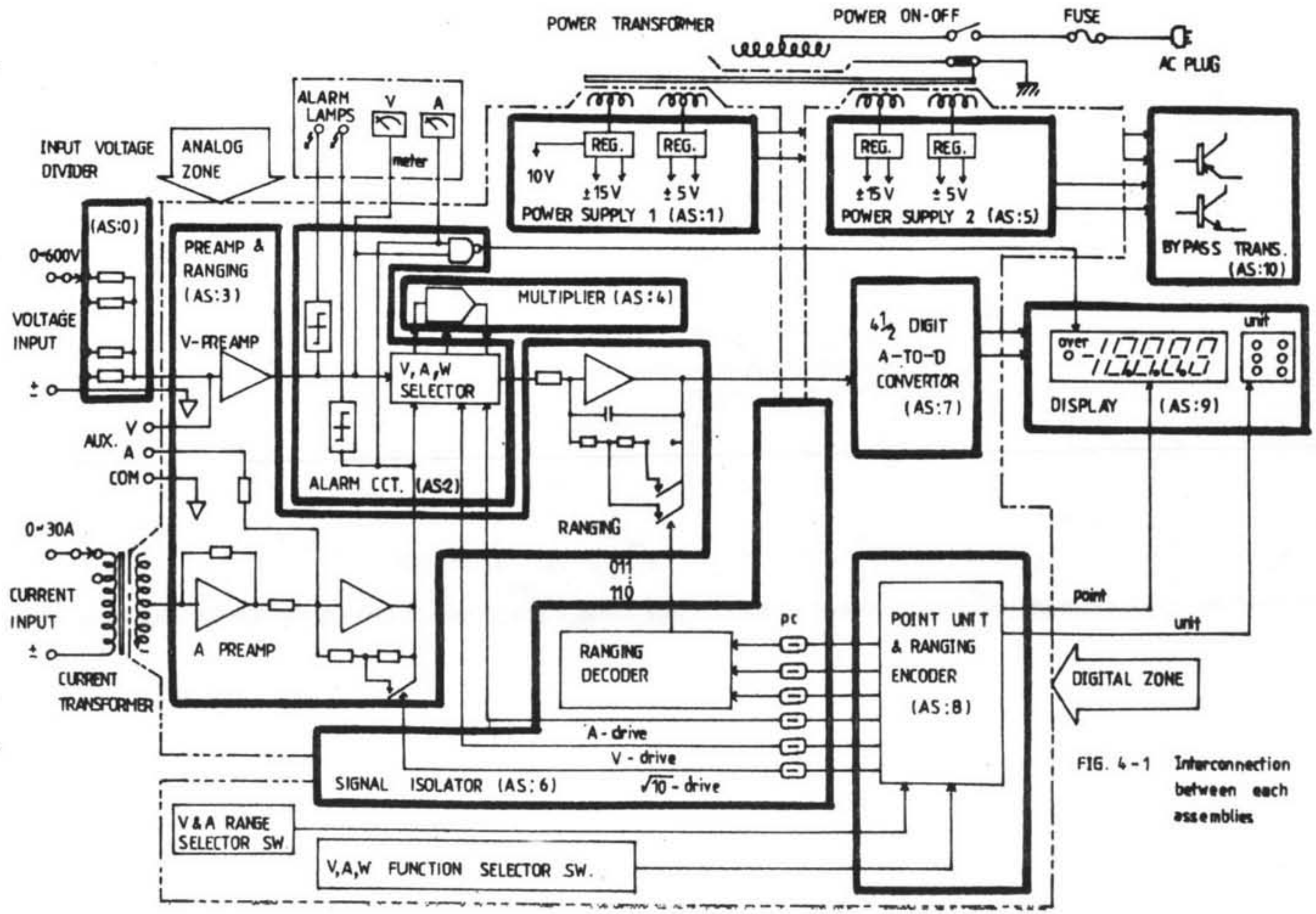


FIG. 4-1 Interconnection between each assemblies

4.4.1 Measuring voltage divider (AS:0)

This assembly, shown in Fig. 4-2, has only precision (less tolerance as possible) resistors to accurately divided input voltage for each measuring ranges. S1 is a voltage selector switch, V is input voltage terminal. Suppose that we select the gain of the V-preamplifier A1 to be 3, which will be discussed later. The calculation to find the divider resistor for 3V, 10V, 30V, 100V, 300V, and 600V full scale ranges can be derived as follows.

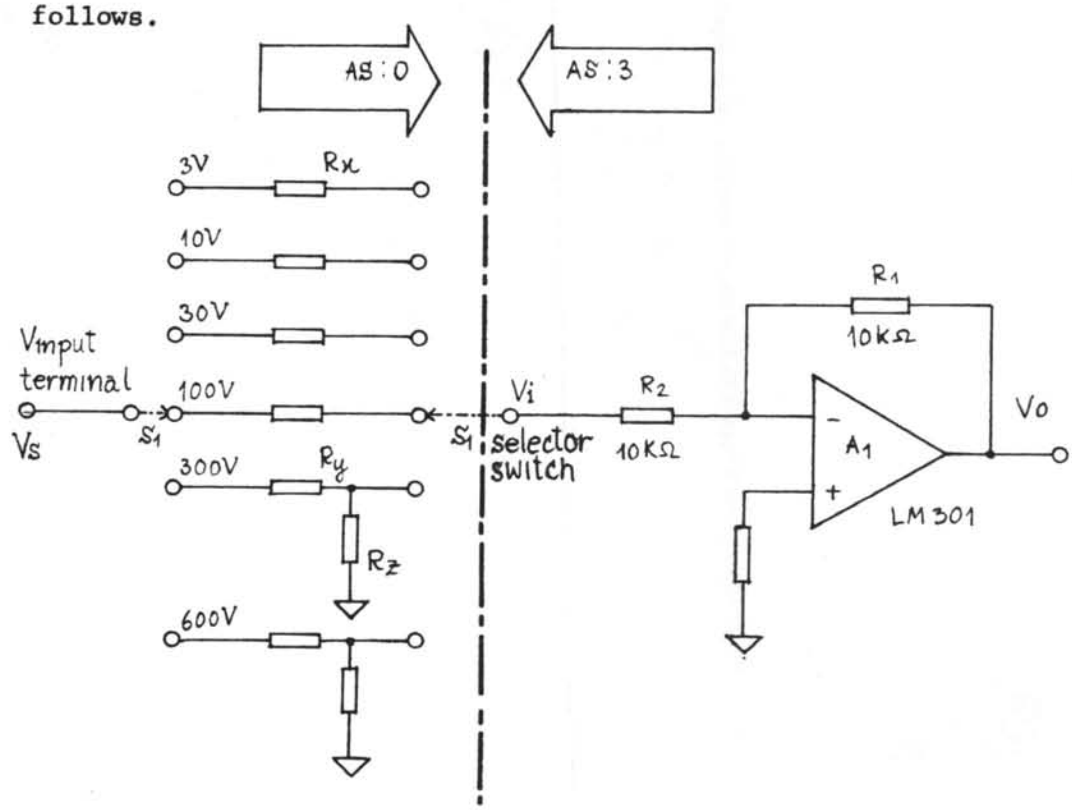


Fig. 4-2 Measuring voltage divider

As described in section 3.7. The designed value Vo of V preamplifier in Fig. 4-2 are separated in two groups (the reasons is shown in sector 4.4.4.3. When voltage range setting is a multiple of 3, the designed Vo is $3\times3/\sqrt{10}$ Vrms full scale and in AC mode

$$\text{gain of A1} = \frac{Vo}{Vi} = \frac{R1}{R2} = 3 \qquad (4\text{-}1)$$

and,

$$Vi = \frac{Vo}{A1}$$

$$= \frac{3 \times 3}{3\times\sqrt{10}} = \frac{3}{\sqrt{10}} \qquad \text{Vrms}$$

In basically

$$\frac{Vs}{Rx + R2} = \frac{Vi}{R2} \qquad (4\text{-}2)$$

Suppose we selected Vs to 3 V range, and R2 = 10kΩ, thus

$$Rx = 21.623 \text{ k}\Omega$$

When the range setting is a multiple of 10, we can use the same solution but substitute every times with Vo = 3V rms. Exception for 300 V and 600 V full scale ranges, the derived value of Rx seem high (more than 3 MΩ) and that value is not easy to keep the tolerance as mentioned. So we have to use another application as shown in Fig. 4-2 and the calculation is

$$Vi \left[(R2//Rz) + Ry\right] = Vs \;.\; R2//Rz \qquad (4\text{-}3)$$

for example ; Vs = 300 V , Vi $\frac{3}{\sqrt{10}}$ V, and R2 = 10 kΩ

then,

$$\frac{Vs}{Vi} = 1 + \frac{Ry}{R2//Rz}$$

$$\frac{300\times\sqrt{10}}{3} = 1 + \frac{Ry}{R2//Rz}$$

$$\frac{Ry}{R2//Rz} = \frac{300\times\sqrt{10}-3}{3}$$

if we select Ry = 1 MΩ

$$\text{we get } R2//Rz = \frac{3\times10^6}{300\sqrt{10}-3} = 3.1723 \text{ k}\Omega$$

When R2 parallel with Rz

$$\frac{1}{R2} + \frac{1}{Rz} = \frac{1}{3.1723}$$

thus, $Rz = 4.6462$ kΩ

A complete diagram of AS:0 shown in Fig. 4-3.

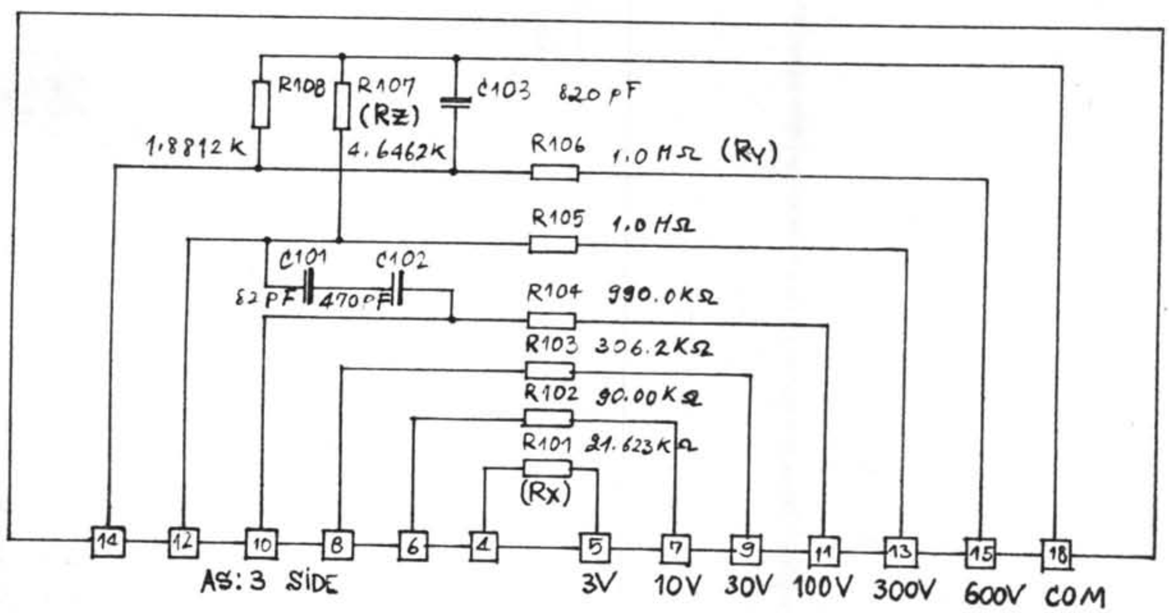


Fig. 4-3 Measuring Voltage divider (AS:0)

4.4.2 Power supply -1 (AS:1) for analog zone

Power supply -1 is a stabilized DC power supply to energize each assembly within an analog potential zone. It is divided into three groups

(1) ±15V/1.5A supplies for op-amps, relays, and indicator lamps

(2) +5V/2.5A supplies for TTL'S

(3) -5V/0.5A and -10V/50 mA supplies only for a multiplier (AS:4)

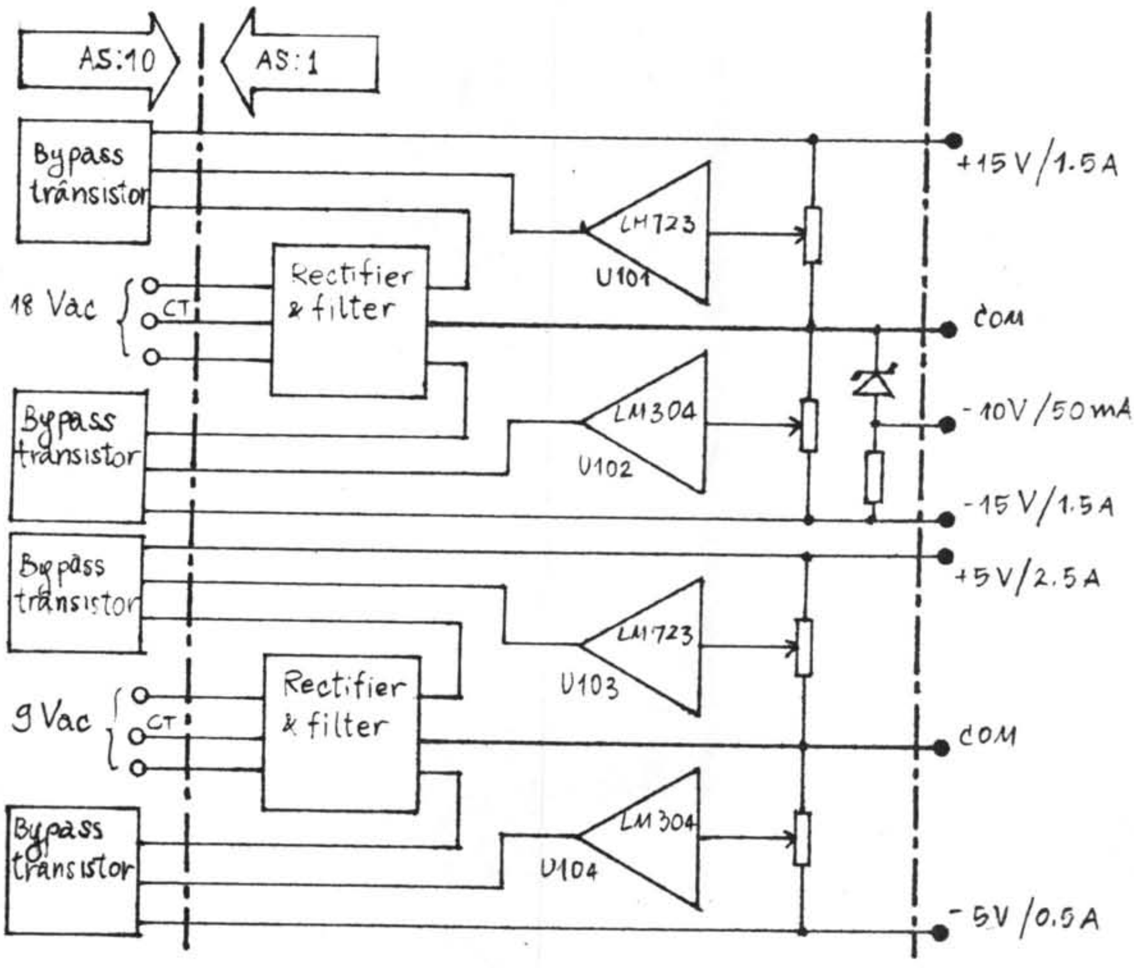


Fig. 4-4 AS:1 Regulated power supply block diagram

All of Regulators are adjustable except for the range -10V. For adjustable positive regulators we use IC No LM 723 and for adjustable negative regulators we use IC No LM 304. Each of the regulators have their own bypass transistor for its output current boosting. These transistors are mounted on bypass transistor card (AS:10). For detail how to select the value of R and C can be finded in "Voltage regulator handbook from National Semiconductor inc". The -10V/50 mA supply is tapped from -15V supply maintained the voltage with zener diode No BZY 93 and series resistor R121 for current limiting. The calculation for R 121 is

$$\text{R current limit} = \left| \frac{\text{V input} - \text{V output}}{\text{desired current}} \right| \qquad (4\text{-}4)$$

in this case, V input = -15 V, V output = -10 V, and desired current = 50 mA substitute in Eq. (4-4)

$$\text{then R121} = \frac{15 - 10}{50 \times 10^{-3}} = 100 \ \Omega$$

The block diagram shown in Fig. 4-4 and the complete drawing shown in Fig. 4-5

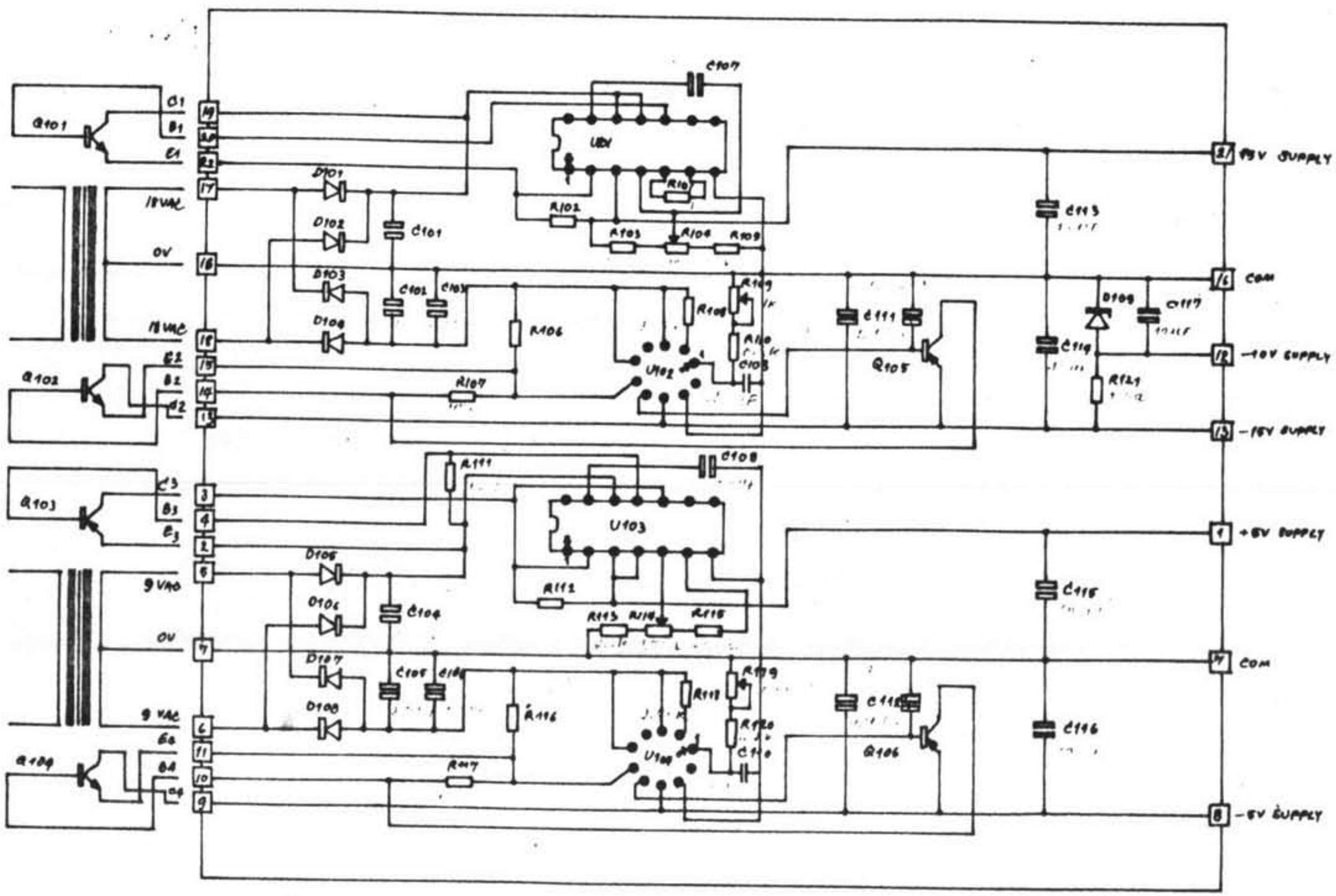


FIG. 4-5 POWER SUPPLY-1 (AS:1)

4.4.3 V,A,W selector and alarm (AS:2)

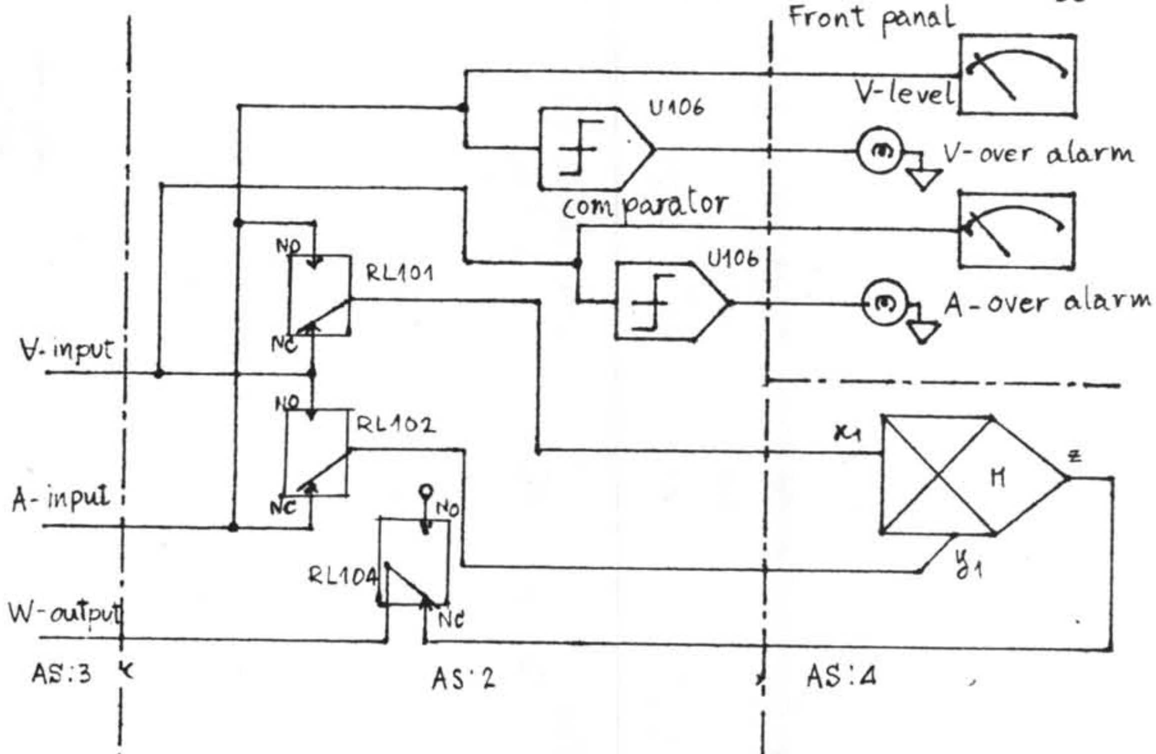


Fig.4-6 Function of AS:2 during power measurement

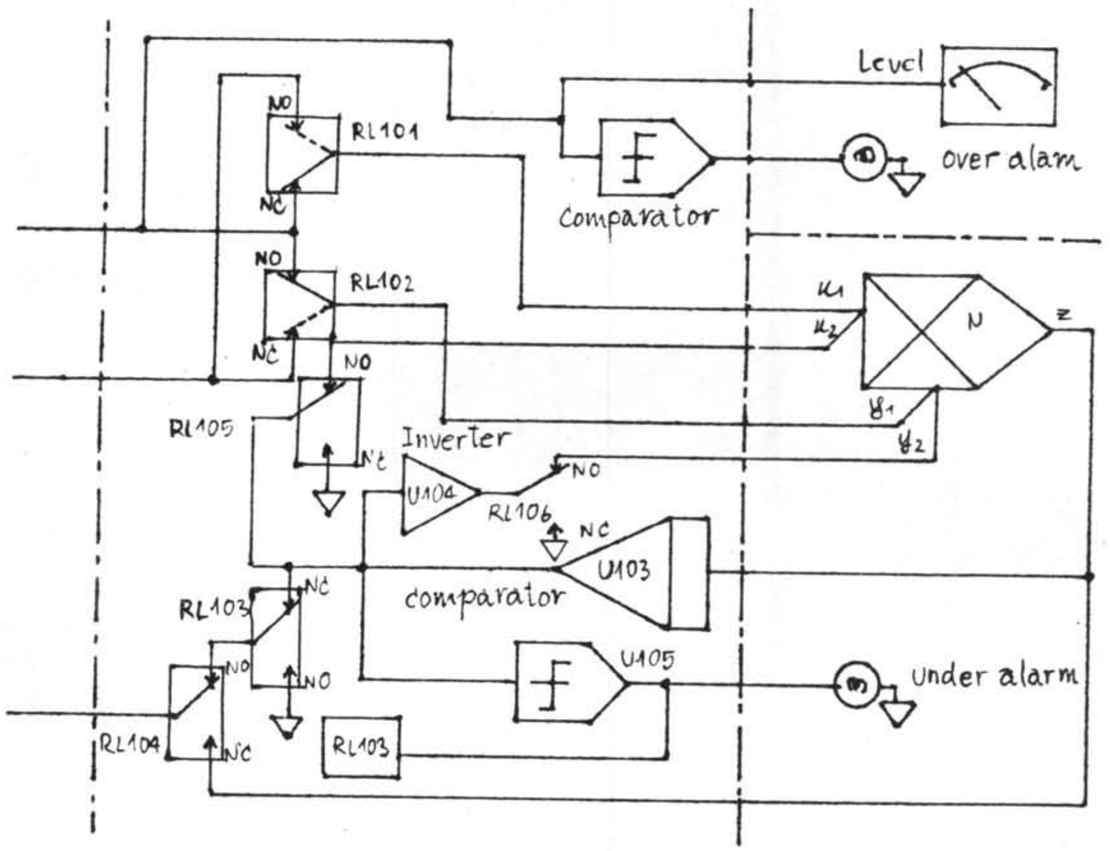


Fig.4-7 Function of AS:2 during Vrms and Arms measurement

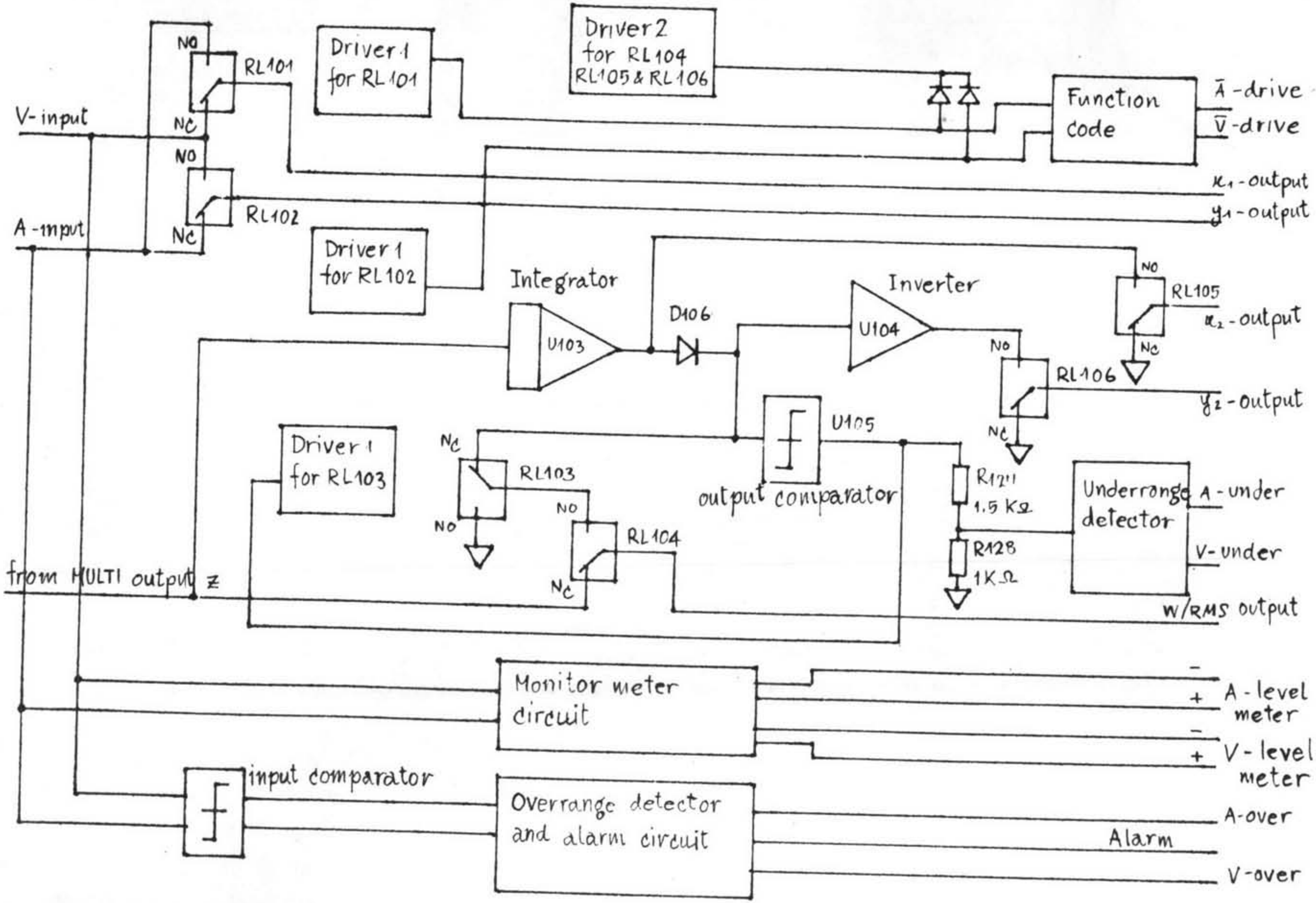


Fig.4-8 AS:2 V,A,W selector and alarm on one-line diagram

Assembly 2 consists of the following four essential circuits.

(1) Switching circuit for the V rms and A rms measuring circuits and the power measuring circuit.

(2) Ghost trap circuit and under range indicator lamp diver circuit.

(3) Monitor meter circuit.

(4) Over range detector circuit and indicator lamp driver circuit.

The function of each of the four circuits is as follows.

4.4.3.1 Switching circuit

A combination of the $\overline{V}$-drive and $\overline{A}$-drive signal actuates relays RL101, 102, 104, 105 and RL106 in figure 4-8, and either the RMS value or power measuring circuit is selected as shown in Figs. 4-6 and 4-7. And the designed to fixing the function in each block shows as follows.

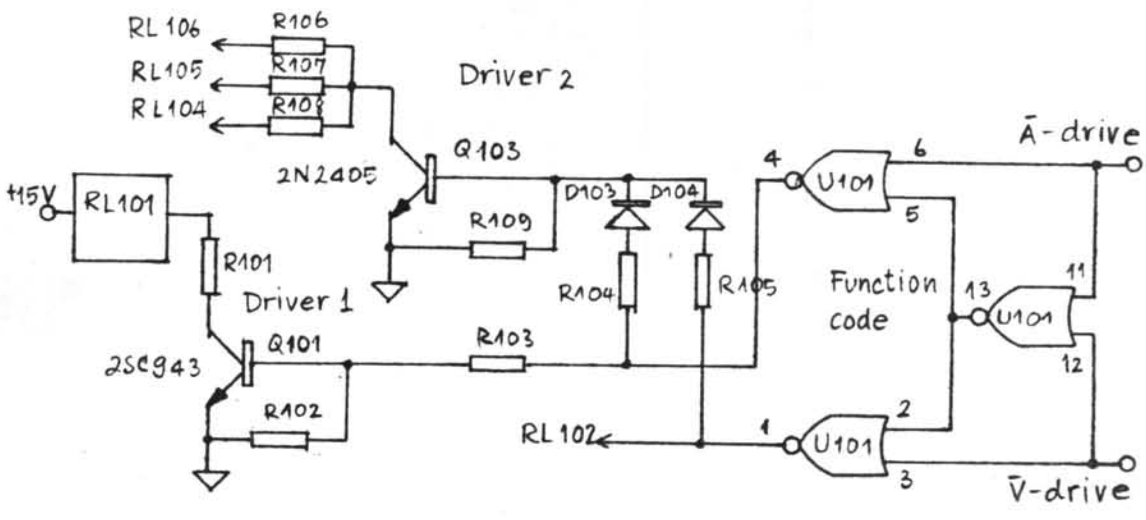


Fig.4-9 Switching Circuit on AS:2

a) Function code circuit

The function code is the combination of logic gates to obtain the output of Driver 1 and Driver 2 from input $\bar{A}$-drive and $\bar{V}$-drive. The input and the desired output truth table is

Function	Input		Output		
	$\bar{A}$-drive	$\bar{V}$-drive	RL101	RL102	RL104, 105, 106
A	0	1	Active	–	Active
V	1	0	–	Active	Active
W	1	1	–	–	–

Table 4-2 Function code signal for AS:2

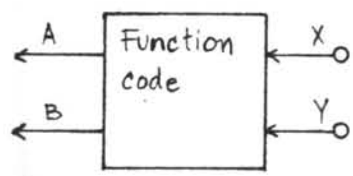
if we given $X = \bar{A}$-drive input

$Y = \bar{V}$-drive input

A = Output to drives RL101

B = Output to drives RL102

C = Output to Driver 2



from truth table above $A = \bar{X} \cdot Y$ (4-5)

$$B = X \cdot \bar{Y} \quad (4\text{-}6)$$

$$C = (\bar{X} \cdot Y)+(X \cdot \bar{Y}) = A+B \quad (4\text{-}7)$$

In this case we must have one Inverter and one AND gate to perform the function A.

applied De Morgen's law to Eq. (4-5)

$$A = \bar{X} \cdot Y \qquad = \bar{X} \cdot Y + X \cdot \bar{X}$$

$$= \bar{X} \cdot (Y+X) \qquad = \overline{\overline{\bar{X} \cdot (Y+X)}}$$

$$= \overline{\bar{\bar{X}} + \overline{(Y+X)}} \qquad = \overline{X+\overline{X+Y}}$$

Then we can used two NOR gate (IC7402) to performed function A and the same solution can be applied to Eq. (4-6). To forming function C we used wire-or technique combined (OR) 2 Signal A and B pass through the diodes D103 and D104.

b) Driver 1 and Driver 2

Because the output (TTL) from function code circuit is not enough to drive the reed relays RL101, 102, 104, 105 or RL106. For this reason we use the driver circuit to boost the current supply for these relays. From Fig. 4-10, the input to the Driver 1 circuit swing from 0V to 5V we must be sure that when the input equal 0V the transistor will cut-off and when the input is 5V the transistor is fully conducted.

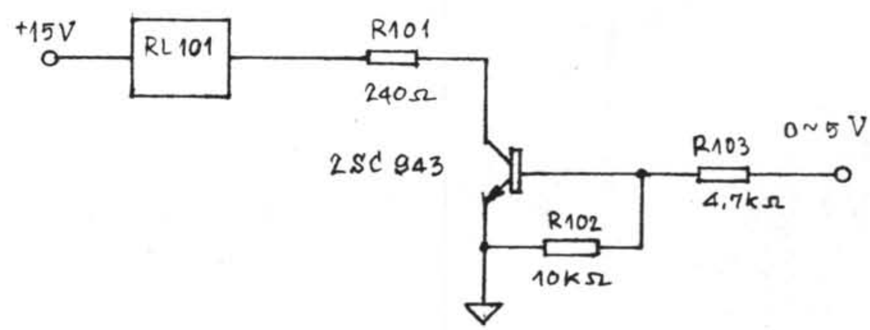


Fig. 4-10 Driver 1 circuit

R102 and R103 are connected as the bias circuit to drive NPN transistor 2SC 943. We selected R102 = 10 kΩ and R103 = 4.7 kΩ to give a full bias when ≃ 5V is applied. RL102 requires+12V supply with current ≃ 10 mA, R101 is used for dropping voltoge supply to the relay, and the value is

$$R101 = \frac{15 - V\ relay - Vce}{Irelay} \quad \Omega \qquad (4-8)$$

$$= \frac{15-12-0.6}{10x10^{-3}} \quad \Omega$$

$$= \frac{2400}{10} \quad = \quad 240 \quad \Omega$$

For Driver 2 the calculation is the same as that of Driver 1, but the transistor current must be maintained at 3 times the relay current.

c.) Integrator circuit

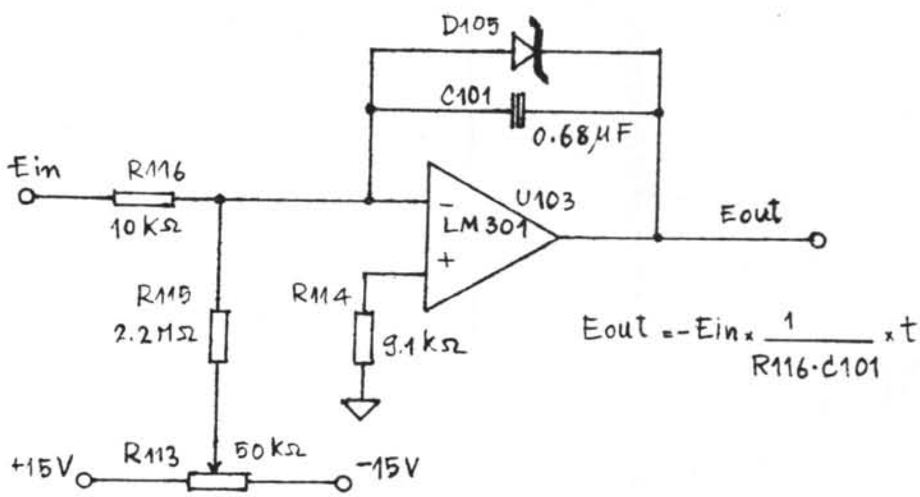


Fig.4-11 Integrator circuit

From Fig. 4-11, diode D105 is intented for preventing Eout from becoming negative. R115 and R113 are connected as the balancing circuit to prevent the drift effects of input offset voltage. As mentioned in section 3.6 the time constant of this integrator must be sufficiently large enough to attenuate the AC component of the input to integrator. For measuring the value of AC from 20 Hz (50 ms) upto 1,500 Hz (667 μs), if we given R116 = 10 kΩ, and from the experiments a suitable value of C101 is 0.68 μF.

d.) Inverting amplifier

This circuit is a normal unity gain inverting amplifier to inverts the output of the integrator and supplies pass through a contact of relay RL106 to multiplier assembly (AS:4) as the Y2-input. IC LM301 is choosed because it is general purpose, cheap, and very popular. From Fig. 4-15, gain of the inverter circuit = -1 and selected value of Rfeedback (R119) and Rinput (R120) are equal to 10 kΩ. In basically R118 is equal to R119 parallel with R120 for minimum error due to input bias current in amplifier circuit, by this way the drift of Vout will be reduced to approximatly 25% of the previous value, (ref. 8, p139) then,

$$R118 \cong R119//R120 \cong 5\ k\Omega$$

4.4.3.2 Ghost trap circuit and under range indicator lamp driver circuit.

The RMS value measuring circuit will not work propery if the signal level is too low. To avoid such inconvenience, we used the ghost trap circuit to detect this phenomenon. First the output of the measured RMS value is fed to the comparator (U105 in Fig. 4-12), which will actuate relay RL103 if the output level of integrator (U103 in Fig.4-7) is lower than approximately 15% of the full-scale value, immediatly the output of the ranging circuit (next state on assembly 3) is stopped, and at the same time the under range lamp is lit by the under range detector circuit. If the under range lamp is lit, the range selector must be set to a range one step lower.

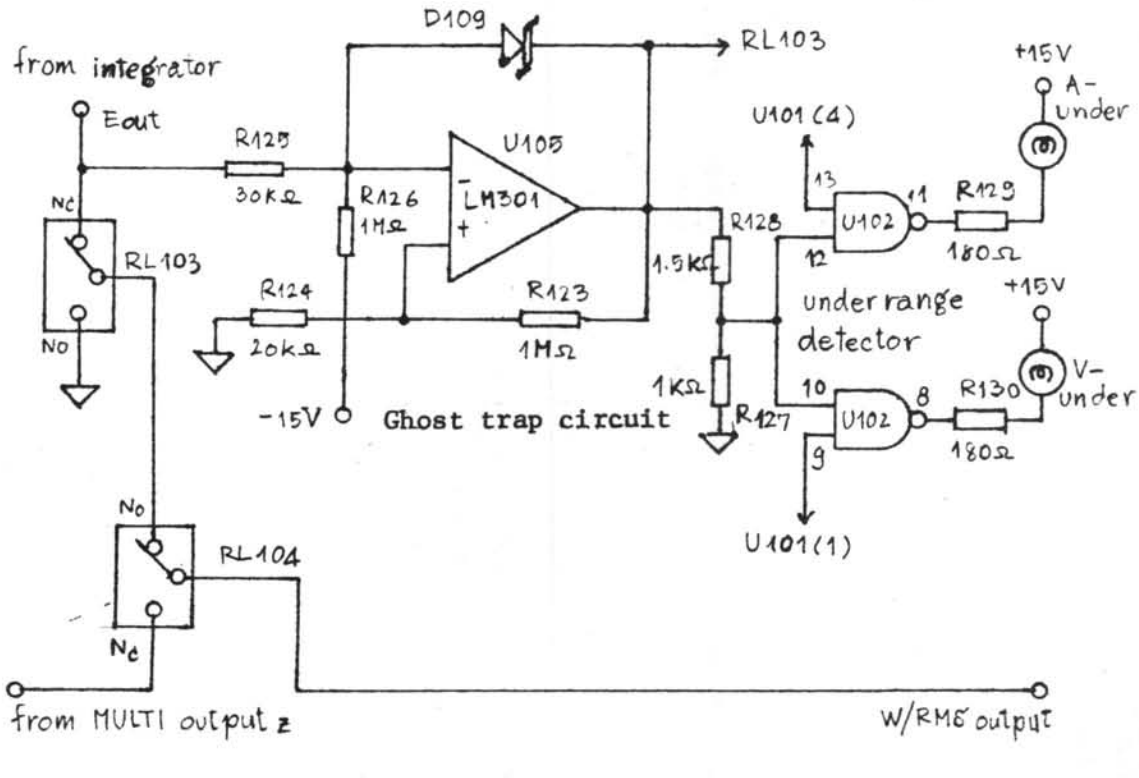


Fig. 4-12 Ghost trap and under range detector circuit

In Fig. 4-12 above U105 works as a positive feedback signal comparator. The equation involved is

$$\text{voltage across R124} = \frac{R124}{R124+R123}\,(+V\ sat) = E\ Out \qquad (4\text{-}9)$$

From an experiment, we find that Eout is -0.3 V rms when the input is 15% of full scale

The setting of the ratio of the comparator is

$$= \frac{E\ out}{+V\ sat} = \frac{0.3}{15} = 0.02$$

from Eq. (4-9) $$\frac{E\ out}{+V\ sat} = \frac{R124}{R124+R123}$$

If we select R124 = 20 kΩ and R123 = 1 MΩ

then, the ratio of $\frac{R124}{R124+R123}$ is also

$$= \frac{20}{20+1{,}000} = 0.0196 \simeq 0.02$$

Every time the measuring input is lower than 15% of full scale the output of comparator U105 equals +15V (+V sat). This voltage is attenuated to 5V or logic "1" by the ratio of R128 and R127. And when gating (NOR) with A-drive (U101 pin 4) or V-drive (U101 pin 1) signal the A-under range lamp or V-under range lamp will give out light. At the same time relay RL103 is energized. The result is that the W/RMS output is shorted to ground and the instrument displays all zeros.

U102 is IC 7401 NAND/buffer gate. R129 and R130 are current limiters for the lamps. If we choose 10 mA lamps the values of R129 and R130 can be 150 to 220 Ω.

4.4.3.3 Monitor meter circuit

The monitors, which are of a rectification type, indicate the input voltage and current in terms of approximate RMS percentage with reference to the full scale. The full scale (100%) corresponds to 3 V rms. The zone between 30% to 110% of meter graduation are green. The green zone includes effective measuring ranges of the instrument.

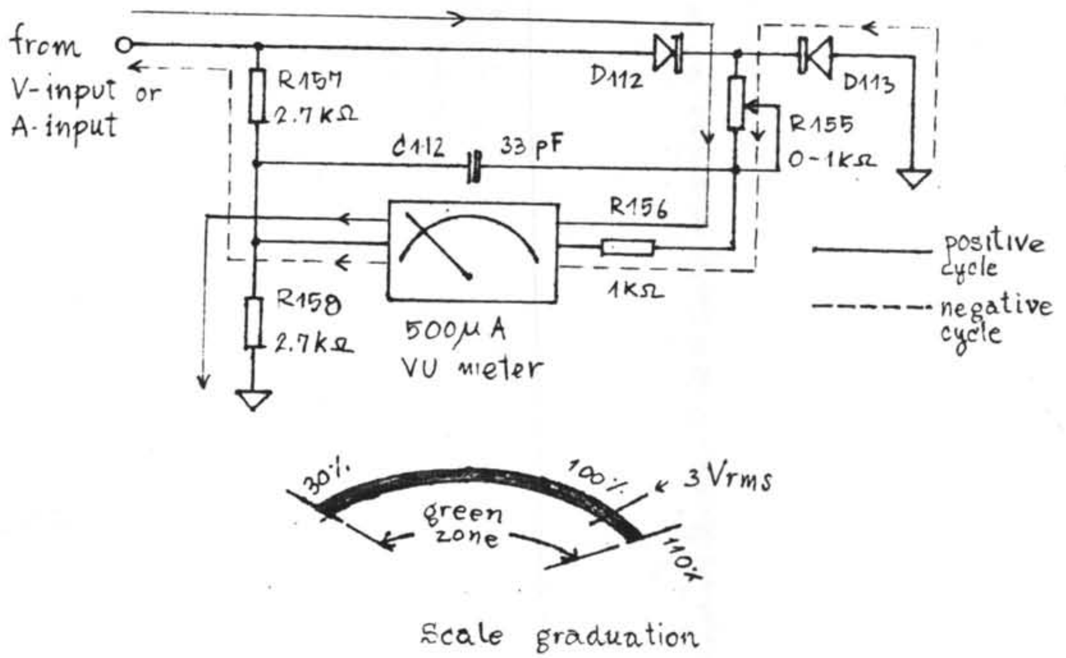


Fig. 4-13 The monitor meter circuit

D112 (1N 4001) is used for rectifying positive cycle of the input signal

D113 (1N 4001) is used for rectifying negative cycle of the input signal.

C112 (33 μF) is used for damping the voltage across the meter.

During the positive cycle most of the current pass through D112, R155, R156,the meter, and R158. If we select the level-meter which requires 500 μA dc to indicate the full scale, then the roughly calculation is

$$R158+R156+R155 \cong \frac{\text{DC voltage of input signal}}{\text{meter current}}$$

$$\cong \frac{3\times 0.707}{500\times 10^{6}} \cong 4.242 \quad k\Omega$$

we can choose many values of R158, K156, and R155 to combines 4.242 kΩ. In this case, we choose R158 = 2.7 kΩ, and R156 = 1 kΩ, whereas R155 can be varied from 0 to 1 kΩ. With the same solution we found that R157 is equal to R158 too.

4.4.3.4 Over range detector circuit and indicator lamp driver circuit

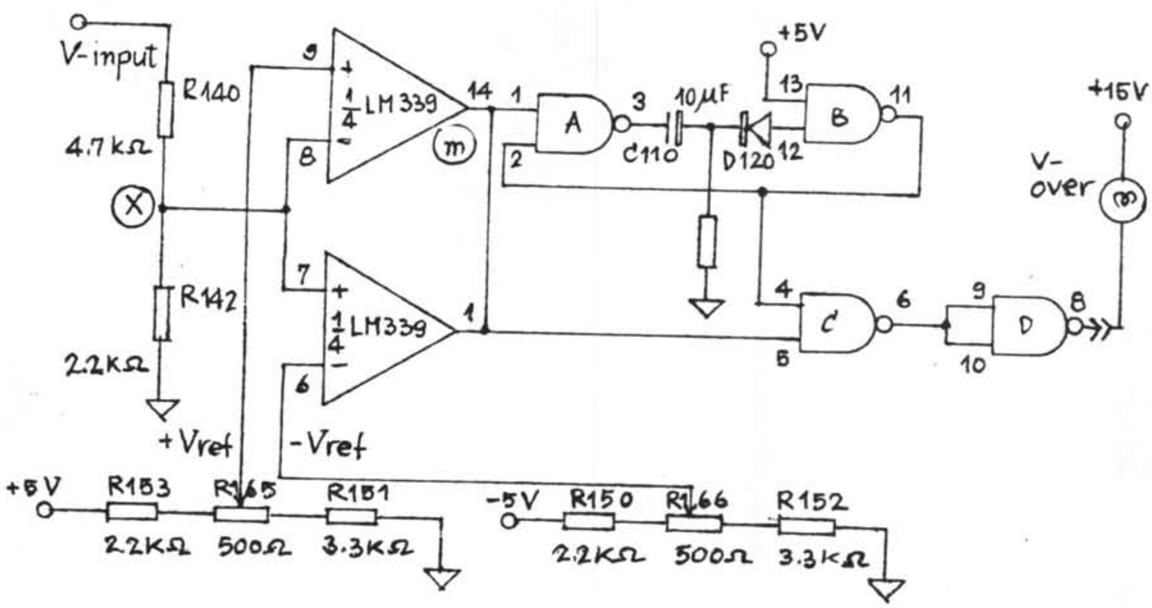


Fig. 4-14 Over range detector circuit

As shown in Fig. 4-14 the V-input and the A-input signal are compared with +Vref and -Vref. The +Vref and the -Vref are set to +3Vdc and -3Vdc by each group of resistors 2.2 kΩ, 500Ω (variable), and 3.3 kΩ. IC LM339 is composed of 4 comparators, one pair at the V-input and the other at the A-input. On V-side, if the peak value of V-input at point X is higher than $\pm$ V ref, the output of the comparator at point m will be equal to -5V (Logic "0"). The four logic NOR gates (A, B, C, D) performs a function to light the V-over range lamp. C110, R148, and D102 are connected to hold the logic "1" at output of gate "A". It can extend the lighting period of indicator lamp during the status change form positive peak to negative peak. D120 is normal signal diode 1N914B, C101 and R148 are 10 μF and 470 Ω respectively. Also this application can be applied to the A-side. The complete circuit diagram of AS:2 is shown in Fig. 4-15.

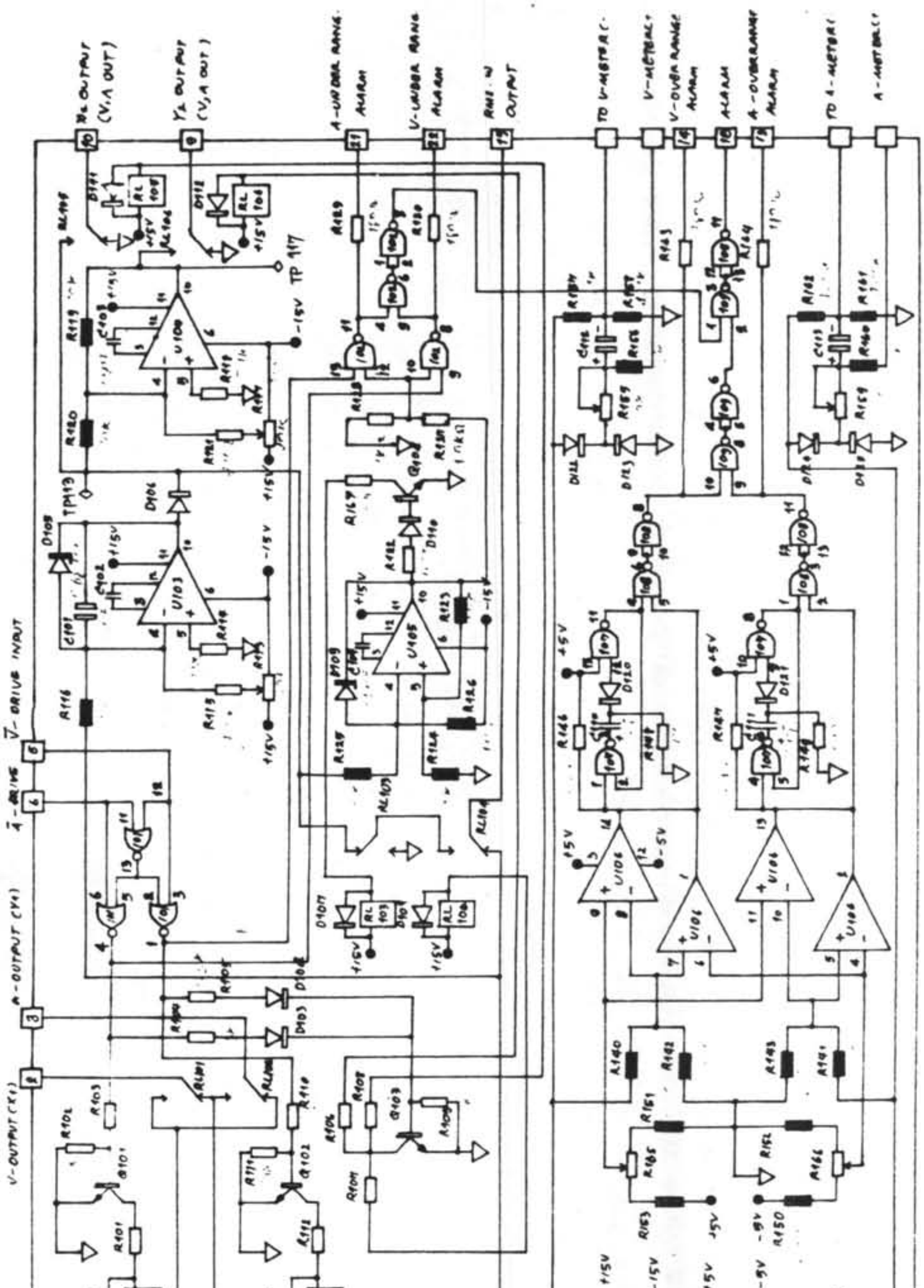


FIG. 4-15 V,A,W SELECTOR & ALARM (AS: 2)

4.4.4 Preamplifier and Ranging Circuit (AS:3)

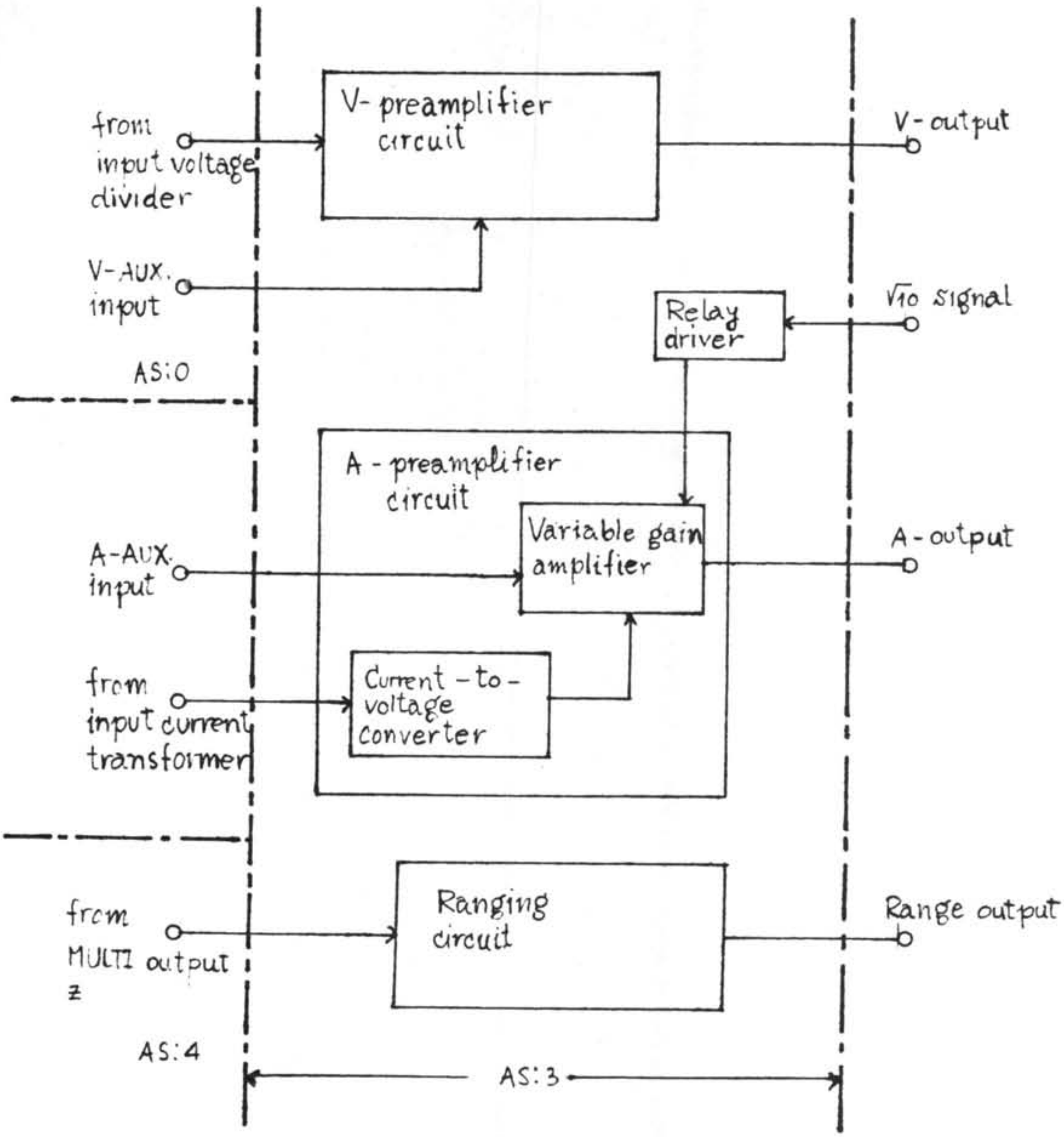


Fig. 4-16 AS:3 Preamplifier and ranging block diagram

Assembly 3 is composes of the following four circuits.

(1) V - preamplifier circuit.

(2) A - preamplifier circuit.

(3) Ranging circuit.

(4) Auxiliary input circuit.

4.4.4.1 V-preamplifier circuit

As described in Section 3.7, the voltage to be measured is divided into 1 V full scale or $3/\sqrt{10}$ V full scale by means of a voltage divider, and that voltage is applied to this amplifier (U101 on AS:3) where the signal is boosted threefold in to -3V full scale or $-3\times3/\sqrt{10}$V full scale.

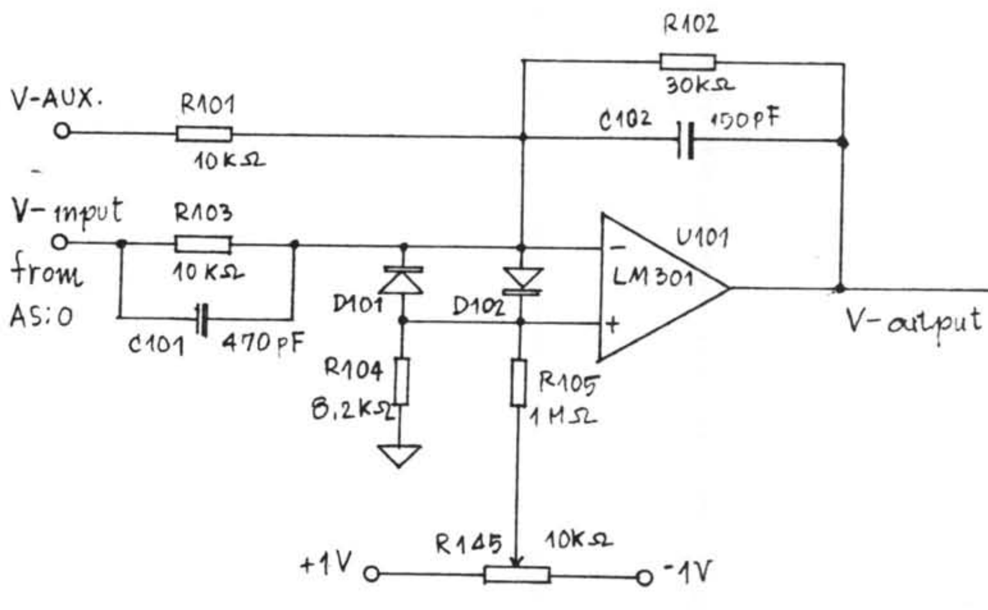


Fig. 4-17 V-preamplifier circuit

In Fig. 4-17 the gain of amplifier U101 $= -\frac{R102}{R103}$ in this case a desired gain $= -\frac{3V}{1V} = -3$ if selected Rin = 10 kΩ, then Rout = − (−3)×10kΩ = 30 kΩ D101 and D102 are the signal diode IN 914B the purpose is to keep the voltage[4] difference between positive and negative input of U101 (LM301). C101 and C102 are used to filter a high frequency interference, a value is 470 PF and 150 PF respectively. R105 and R145 is adjusted to correct a feed-through error of U101.

4.4.4.2 A-preamplifier circuit

As described in section 3.7, the secondary winding of the current transformer, used for adjusting the level of the input current, sends out a current of 10 mA full scale to the initial stage, or the A-to-V converting stage, of the A-preamplifier. Thus the output of 3V full scale is obtained.

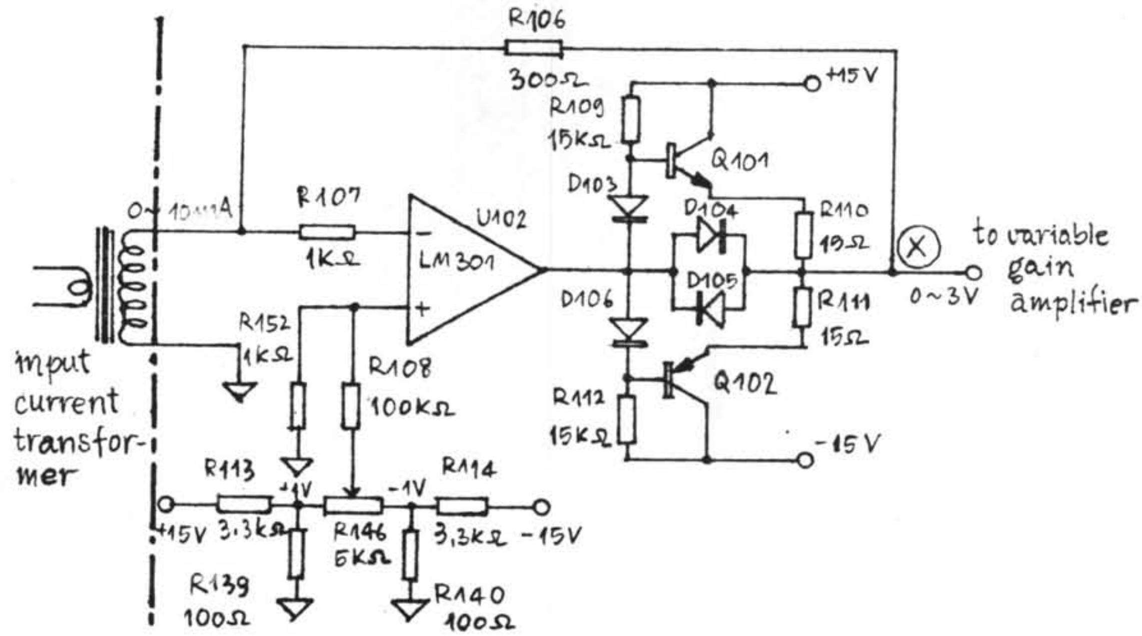


Fig. 4-18 First stage (A-to-V converter) of A-preamplifier

The main signal 10 mA full scale passes through R106 (300Ω) and gives a voltage of 3V at point X. U102, Q101, Q102 and the other components in this stage perform a function of bipolar voltage-to-current converters as described in Reference[4]

In the next stage variable-gain amplifier U103 (in AS:3), the $\sqrt{10}$ signal controls the switching relay RL101 for the negative feedback resistors R116 and R118 to vary the gain to −1 or $-3/\sqrt{10}$. Therefore, the output voltage of the amplifier becomes either −3V full scale, or $-3\times3/\sqrt{10}$ V full scale, when the input voltage is 3V full scale.

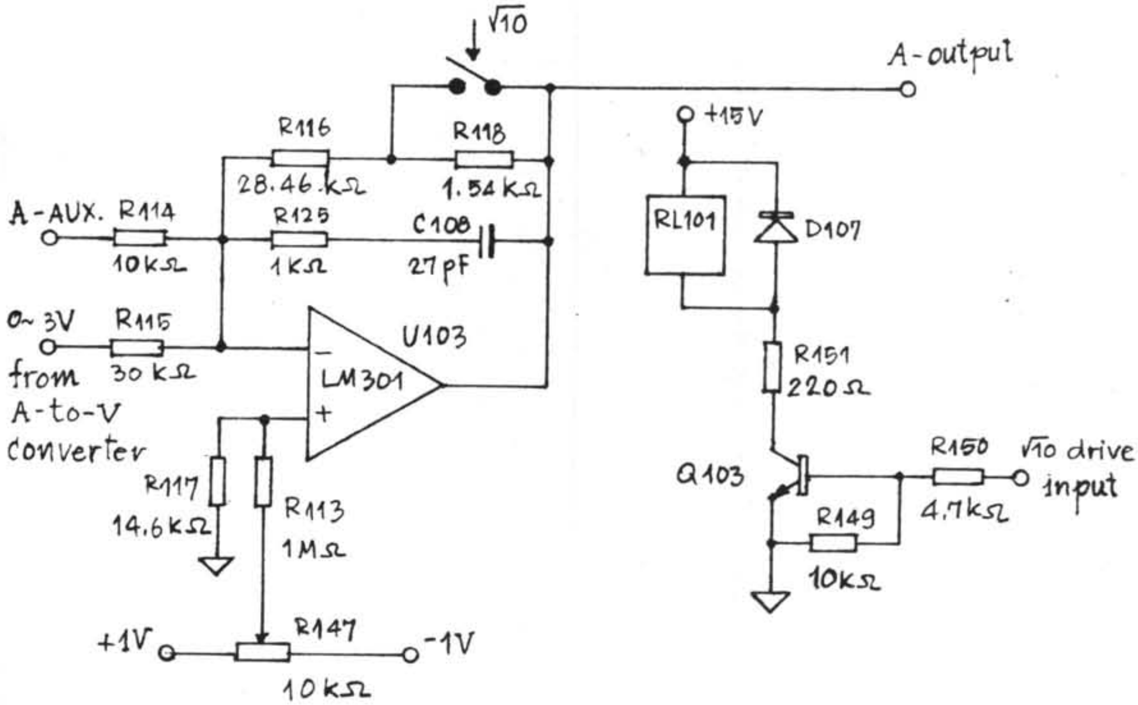


Fig. 4-19 Second stage of A-preamplifier

When the $\sqrt{10}$ signal is asserted the gain is $-3/\sqrt{10}$.

In this case, the gain of U101 = $-\frac{R116}{R115} = -3/\sqrt{10}$.

If we select R115 = 30 kΩ, then R116 = $3/\sqrt{10}$.R115 = $\frac{3\times30}{\sqrt{10}}$ = 28.46 kΩ

and when the $\sqrt{10}$ signal is absent the gain is -1.

From Fig. 4-19, the gain of the amplifier = $-\frac{R116+R118}{R115} = -1$

Thus, R118 = R115-R116 = 30-28.46 = 1.54 kΩ

R117 = R115 in parallel with R116,

= 14.6 kΩ

R113 and R147 perform a function of feed-through compensation

R125 and C108 are used to smooth the output of the op-amp. The value of C 108 must be small, being in the range of 10 to 40 pF, if R125 = 1 kΩ.

The values of each components in the $\sqrt{10}$ drive signal circuit is of the same design as described is Section 4.4.3.1 (b).

4.4.4.3 Ranging circuit

From Figs. 4-6 and 4-7, the output of the multiplier (AS:4), namely, W/RMS output, is sent to the ranging circuit to adapt the level of the output voltage corresponding to the initial range for display on the DVM. The ranging circuit is composed of two sections.

(1) Variable gain amplifier or ranging amplifier.

(2) Ranging relay circuit which changes the gain of the amplifier above as commanded by the ranging signal given in Table 4-3 Column 11.

From Table 4-3

Columns 1&2 - are all possible range settings.

on V-side = 3, 10, 30, 100, 300, and 600V full scale

on A-side = 0.1, 0.3, 1, 3, 6, 10, and 30A full scale

Columns 3 - is the range selection to display the initial value with $4\frac{1}{2}$ digits and 1 V full scale A-to-D converter. Note that the decimal point is not yet taken into consideration.

Columns 4-7 - Case Study I

Column 4 - shows the output of V-preamplifier without a difference between the voltage range settings in a multiple of 3 and 10. It is also fixed to 3V full scale.

Columns 5 - shows the output of A-preamplifier in the same condition as Column 4.

Columns 6 - shows the output of the multiplier (AS:4)

Columns 7 - shows the gain of ranging circuit which converts the output of multiplier (column 6) to become the initial values (column 3).

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
RANGE SET			CASE I				CASE II				CASE III				
V	A	$4\frac{1}{2}$ DIGIT DISPL.	V	A	Z	G	V	A	Z	GAIN	V	A	Z	GAIN	
3		0 3 0 0 0	3		3	1	$3\times3/\sqrt{10}$		$3\times3/\sqrt{10}$	$\sqrt{10}/3$	6		6	1/2	<A>
10		1 0 0 0 0	3		3	10/3	3		3	10/3	3		3	10/3	<B>
30	*	0 3 0 0 0	3	*	3	1	$3\times3/\sqrt{10}$	*	$3\times3/\sqrt{10}$	$\sqrt{10}/3$	6	*	6	1/2	
100		1 0 0 0 0	3		3	10/3	3		3	10/3	3		3	10/3	
300		0 3 0 0 0	3		3	1	$3\times3/\sqrt{10}$		$3\times3/\sqrt{10}$	$\sqrt{10}/3$	6		6	1/2	
600		0 6 0 0 0	3		3	2	$3\times3/\sqrt{10}$		$3\times3/\sqrt{10}$	$2\sqrt{10}/3$	6		6	1	
	0.1	1 0 0 0 0		3	3	10/3		3	3	10/3		3	3	10/3	
	0.3	0 3 0 0 0		3	3	1		$3\times3/\sqrt{10}$	$3\times3/\sqrt{10}$	$\sqrt{10}/3$		6	6	1/2	
	1	1 0 0 0 0		3	3	10/3		3	3	10/3		3	3	10/3	
*	3	0 3 0 0 0	*	3	3	1	*	$3\times3/\sqrt{10}$	$3\times3/\sqrt{10}$	$\sqrt{10}/3$	*	6	6	1/2	
	6	0 6 0 0 0		3	3	2		$3\times3/\sqrt{10}$	$3\times3/\sqrt{10}$	$2\sqrt{10}/3$		6	6	1	<C>
	10	1 0 0 0 0		3	3	10/3		3	3	10/3		3	3	10/3	
	30	0 3 0 0 0		3	3	1		$3\times3/\sqrt{10}$	$3\times3/\sqrt{10}$	$\sqrt{10}/3$		6	6	1/2	
3	0.1	0 3 0 0 0	3	3	3	1	$3\times3/\sqrt{10}$	3	$3\times3/\sqrt{10}$	$\sqrt{10}/3$	6	3	6	1/2	
3	0.3	0 9 0 0 0	3	3	3	3	$3\times3/\sqrt{10}$	$3\times3/\sqrt{10}$	27/10	10/3	6	6	12	3/4	<D>
3	1	0 3 0 0 0	3	3	3	1	$3\times3/\sqrt{10}$	3	$3\times3/\sqrt{10}$	$\sqrt{10}/3$	6	3	6	1/2	
3	3	0 9 0 0 0	3	3	3	3	$3\times3/\sqrt{10}$	$3\times3/\sqrt{10}$	27/10	10/3	6	6	12	3/4	
3	6	0 1 8 0 0	3	3	3	3/5	$3\times3/\sqrt{10}$	$3\times3/\sqrt{10}$	27/10	2/3	6	6	12	3/20	<E>
3	10	0 3 0 0 0	3	3	3	1	$3\times3/\sqrt{10}$	3	$3\times3/\sqrt{10}$	10/3	6	3	6	1/2	
3	30	0 9 0 0 0	3	3	3	3	$3\times3/\sqrt{10}$	$3\times3/\sqrt{10}$	27/10	10/3	6	6	12	3/4	
10	0.1	1 0 0 0 0	3	3	3	10/3	3	3	3	10/3	3	3	3	10/3	
10	0.3	0 3 0 0 0	3	3	3	1	3	$3\times3/\sqrt{10}$	$3\times3/\sqrt{10}$	$\sqrt{10}/3$	3	6	6	1/2	
10	1	1 0 0 0 0	3	3	3	10/3	3	3	3	10/3	3	3	3	10/3	
10	3	0 3 0 0 0	3	3	3	1	3	$3\times3/\sqrt{10}$	$3\times3/\sqrt{10}$	$\sqrt{10}/3$	3	6	6	1/2	
10	6	0 6 0 0 0	3	3	3	2	3	$3\times3/\sqrt{10}$	$3\times3/\sqrt{10}$	$2\sqrt{10}/3$	3	6	6	1	
10	10	1 0 0 0 0	3	3	3	10/3	3	3	3	10/3	3	3	3	10/3	
10	30	0 3 0 0 0	3	3	3	1	3	$3\times3/\sqrt{10}$	$3\times3/\sqrt{10}$	$\sqrt{10}/3$	3	6	6	1/2	
30	0.1	0 3 0 0 0	3	3	3	1	$3\times3/\sqrt{10}$	3	$3\times3/\sqrt{10}$	$\sqrt{10}/3$	6	3	6	1/2	
30	0.3	0 9 0 0 0	3	3	3	3	$3\times3/\sqrt{10}$	$3\times3/\sqrt{10}$	27/10	10/3	6	6	12	3/4	
30	1	0 3 0 0 0	3	3	3	1	$3\times3/\sqrt{10}$	3	$3\times3/\sqrt{10}$	$\sqrt{10}/3$	6	3	6	1/2	
30	3	0 9 0 0 0	3	3	3	3	$3\times3/\sqrt{10}$	$3\times3/\sqrt{10}$	27/10	10/3	6	6	12	3/4	
30	6	0 1 8 0 0	3	3	3	3/5	$3\times3/\sqrt{10}$	$3\times3/\sqrt{10}$	27/10	2/3	6	6	12	3/20	
30	10	0 3 0 0 0	3	3	3	1	$3\times3/\sqrt{10}$	3	$3\times3/\sqrt{10}$	$\sqrt{10}/3$	6	3	6	1/2	
30	30	0 9 0 0 0	3	3	3	3	$3\times3/\sqrt{10}$	$3\times3/\sqrt{10}$	27/10	10/3	6	6	12	3/4	
100	0.1	1 0 0 0 0	3	3	3	10/3	3	3	3	10/3	3	3	3	10/3	
100	0.3	0 3 0 0 0	3	3	3	1	3	$3\times3/\sqrt{10}$	$3\times3/\sqrt{10}$	$\sqrt{10}/3$	3	6	6	1/2	
100	1	1 0 0 0 0	3	3	3	10/3	3	3	3	10/3	3	3	3	10/3	
100	3	0 3 0 0 0	3	3	3	1	3	$3\times3/\sqrt{10}$	$3\times3/\sqrt{10}$	10/3	3	6	6	1/2	
100	6	0 6 0 0 0	3	3	3	2	3	$3\times3/\sqrt{10}$	$3\times3/\sqrt{10}$	$2\sqrt{10}/3$	3	6	6	1	
100	10	1 0 0 0 0	3	3	3	10/3	3	3	3	10/3	3	3	3	10/3	
100	30	0 3 0 0 0	3	3	3	1	3	$3\times3/\sqrt{10}$	$3\times3/\sqrt{10}$	$\sqrt{10}/3$	3	6	6	1/2	
300	0.1	0 3 0 0 0	3	3	3	1	$3\times3/\sqrt{10}$	3	$3\times3/\sqrt{10}$	$\sqrt{10}/3$	6	3	6	1/2	
300	0.3	0 9 0 0 0	3	3	3	3	$3\times3/\sqrt{10}$	$3\times3/\sqrt{10}$	27/10	10/3	6	6	12	3/4	
300	1	0 3 0 0 0	3	3	3	1	$3\times3/\sqrt{10}$	3	$3\times3/\sqrt{10}$	$\sqrt{10}/3$	6	3	6	1/2	
300	3	0 9 0 0 0	3	3	3	3	$3\times3/\sqrt{10}$	$3\times3/\sqrt{10}$	27/10	10/3	6	6	12	3/4	
300	6	0 1 8 0 0	3	3	3	3/5	$3\times3/\sqrt{10}$	$3\times3/\sqrt{10}$	27/10	2/3	6	6	12	3/20	
300	10	0 3 0 0 0	3	3	3	1	$3\times3/\sqrt{10}$	3	$3\times3/\sqrt{10}$	$\sqrt{10}/3$	6	3	6	1/2	
300	30	0 9 0 0 0	3	3	3	3	$3\times3/\sqrt{10}$	$3\times3/\sqrt{10}$	27/10	10/3	6	6	12	3/4	
600	0.1	0 6 0 0 0	3	3	3	2	$3\times3/\sqrt{10}$	3	$3\times3/\sqrt{10}$	$2\sqrt{10}/3$	6	3	6	1	
600	0.3	0 1 8 0 0	3	3	3	3/5	$3\times3/\sqrt{10}$	$3\times3/\sqrt{10}$	27/10	2/3	6	6	12	3/20	
600	1	0 6 0 0 0	3	3	3	2	$3\times3/\sqrt{10}$	3	$3\times3/\sqrt{10}$	$2\sqrt{10}/3$	6	3	6	1	
600	3	0 1 8 0 0	3	3	3	3/5	$3\times3/\sqrt{10}$	$3\times3/\sqrt{10}$	27/10	2/3	6	6	12	3/20	
600	6	0 3 6 0 0	3	3	3	6/5	$3\times3/\sqrt{10}$	$3\times3/\sqrt{10}$	27/10	4/3	6	6	12	3/10	<F>
600	10	0 6 0 0 0	3	3	3	2	$3\times3/\sqrt{10}$	3	$3\times3/\sqrt{10}$	$2\sqrt{10}/3$	6	3	6	1	
600	30	0 1 8 0 0	3	3	3	3/5	$3\times3/\sqrt{10}$	$3\times3/\sqrt{10}$	27/10	2/3	6	6	12	3/20	

Table 4-3 Relationship between ranging selection

Columns 8-11 - Case Study II

The meanings in Columns 8, 9, 10 and 11 are the same as in Columns 4, 5, 6 and 7, respectively. In this Case Study the voltage output of V and/or A-preamplifier is different from that in Case Study I. It is equal to 3V full scale when the range setting is a multiple of 10, and equal to $3\times3/\sqrt{10}$ V full scale when the range setting is a multiple of 3.

Columns 12-15- Case Study III

Case Study III is the same as the Case Study II but, instead of $3\times3/\sqrt{10}$, we use 3×2 or 6 V full scale when the range setting is a multiple of 3 to see the trend of the results

Result 1 : Considering lines A, B, C, D, E, and F and Columns 7, 11, and 15 we can see that

- In Case Study I we need 6 different gains of the ranging amplifier. (They are 1, 10/3, 2, 3, 3/5 and 6/5)
- In Case Study II we need 5 different gains of the ranging amplifier. (They are $\sqrt{10}/3$, 10/3, $2\sqrt{10}/3$, 2/3, and 4/3)
- In Case Study III we need 6 different gains of the ranging amplifier. (They are 1/2, 10/3, 1, 3/4, 3/20, and 3/10)

Result 2 : In Columns 6, 10 and 14

- Case Study I requires that the output of multiplier (AS:4) span from 0 to 3V.
- Case Study II requires that the output span from 0 to $3\times3/\sqrt{10}$ V and 3V.
- Case Study III requires that the output span from 0 to 12V.

From Result1we can see that Case Study II is the best because it needs only 5 different gains of the ranging amplifier. If we use more different gains of the amplifier then we need more decoding signals and relay drivers. It will also result in a larger amplification error due to the increasing number of series feedback resistors. Result 2 shows that Case Study I and Case Study II are nearly the same. However, Case Study III requires a longer span of linearlity for multiplication, and it is difficult to make a linearlity to cover the whole span. We can reduce the output of the multiplier by reducing the voltage output from V and/ or A-preamplifier but we cannot reduce the number of different gains for the ranging amplifier. This is the reason why we design the different voltage outputs of the V and A preamplifiers to make it agree with Case Study II.

In Figs. 4-6 and 4-7, the DC voltage output from multiplier (AS:4) is fed to the ranging amplifier. The gain of this amplifier can be varied by switching over the negative feedback resistor R129 to R132 in Fig. 4-20 by means of four relays, RL104 to 107 in the ranging relay circuit. The said relays are controled by the ranging signal which comes from the ranging encoder (on AS:8) through the signal isolator (on AS:6).

The translation of the main signal for the input from the front panel to the ranging output described above is illustrated in Table 4-4.

input voltage	attenuated voltage	amplification (AS:3)	computing (AS:2, AS:3)	ranging (AS:2, AS:3)
100 Vrms 600 Vrms	1 Vrms $1\times3/\sqrt{10}$ Vrms	3 Vrms $3\times3/\sqrt{10}$ Vrms	3 Vdc $3\times3/\sqrt{10}$ Vdc	1.0 Vdc 0.6 Vdc
input current	transformed current	conversion to voltage	computing (AS:2, AS:4)	ranging (AS:2, AS:3)
10 Arms 30 Arms	10mA rms 10mA rms	3 Vrms $3\times3/\sqrt{10}$ Vrms	3 Vdc $3\times3/\sqrt{10}$ Vdc	1.0 Vdc 0.3 Vdc

Table 4-4 Route of the input voltage and current up to ranging

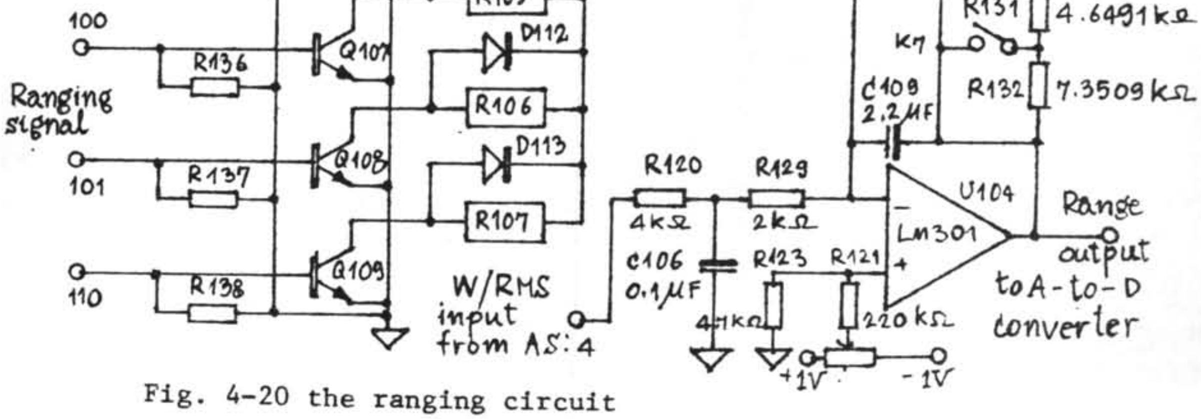


Fig. 4-20 the ranging circuit

To meet the requirement in Case Study II the ranging amplifier must vary the gain amplifier for 5 different gains, which are $-10/3$, $-2\sqrt{10}/3$, $-4/3$ $-\sqrt{10}/3$, and $-2/3$. In Fig. 4-20, when relay RL104 is energized the gain will be lowest and equal to $-2/3$.

Since the gain of the op-amp is

$$-\frac{R\ \text{feedback}}{R\ \text{input}} = \frac{-Rf}{Ri} \tag{4-10}$$

then

$$Rf = -Ri \times \text{Gain} \tag{4-11}$$

Choosing value for Ri =6 kΩ and substituting it into Eq. (4-11), we obtain

$$Rf1 = R126 = \frac{2.Ri}{3} = \frac{2\times 6}{3} = 4k\Omega$$

The next gain is $-\sqrt{10}/3$, which is obtained when RL105 is energized (range code N<u>o</u> 100). In this case

$$Rf2 = Rf1{+}R129 = \frac{\sqrt{10}.Ri}{3} = \frac{\sqrt{10}\times 6}{3} = 6.3245\ k\Omega$$

and

$$R129 = Rf2-R126 = 6.3245-4 = 2.3245\ k\Omega$$

For the gain of $-4/3$, RL106 is energized (range code N<u>o</u> 101). Also since

$$Rf3 = Rf2{+}R130 = \frac{4.RL}{3} = \frac{4\times 6}{3} = 8\ k\Omega$$

then

$$R130 = Rf3-Rf2 = 8-6.3245 = 1.6755\ k\Omega$$

The next gain is $-2\sqrt{10}/3$, which is obtained when RL107 is energized (range code N<u>o</u> 110). Since

$$Rf4 = Rf3+R131 = \frac{2\sqrt{10}.Ri}{3} = \frac{2\sqrt{10}.6}{3} = 12.6491 \text{ k}\Omega$$

then

$$R131= Rf4-Rf3 = 12.6491-8 = 4.6491 \text{ k}\Omega$$

The highest gain of 10/3 occurs when all relays are de-energized. Using Eq. (4-11) once again, we obtain

$$Rf5 = Rf4+R132 = \frac{10.Ri}{3} = \frac{10\times 6}{3} = 20 \text{ k}\Omega$$

and

$$R132= Rf5-Rf4 = 20-12.6491 = 7.3509 \text{ k}\Omega$$

From the circuit in Fig. 4-20, R input is R120 in series with R119 and C106 is used for noise suppression purpose.

R123 is equal to R input in parallel with R feedback as described in Subsection 4.4.4.3 (d). Its value is calculated to be about 4.7 kΩ.

In the relay circuit, the calculation is the same as mentioned in subsection 4.4.3.1 (b) and all relays are chosen to be those of single-pole single-trow reed type to minimize the power supply. The values of all components shown in Fig. 4-20 .

4.4.4.4 Auxiliary input circuit

As mentioned in section 3.7, various tests can be performed by applied 1 V rms or 1 Vdc to the V-and/or A-AUX input terminals. The discussion will be made here for such circuits with reference to Figs. 4-17 and 4-19

1) V-AUX input (see Fig. 4-17) : An input of 1V here is applied to the V-preamplifier (U101) without passing through the input voltage divider. With the V-range selector set to AUX, a signal corresponding to 100V range is sent out to the point, unit, and ranging encoder (AS:8). If the selector is set to another range, a signal corresponding to that range is sent out to AS:8. In the latter case, the output voltage from V-preamplifier will not exceed 3V for any range setting.

2) A-AUX input (see Fig. 4-19) : An input of 1V here is applied directly to the variable gain amplifier (U103) without passing through the input current transformer and the current-to-voltage converting amplifier (U102, AS:3). With the A-range selector set to AUX, a signal corresponding to 10 A range is sent out to AS:8. If the selector is set to another range, a signal corresponding to that range is sent out to AS:8. In the latter case, the output from A-preamplifier, as in (1) above, will not exceed 3V when range is set to 0.1A, 1A, or 10A, and $3\times3/\sqrt{10}$ V when 0.3A, 3A, 6A, and 30A. This is because of the influence of the $\sqrt{10}$ control signal.

3) Ranging (see Fig. 4-20) : An RMS value or power operational output by the above mentioned V-or A-output is again sent to the W/RMS input, and then to the ranging amplifier (U104). The gain of the ranging amplifier is controlled by the ranging signal and the output is displayed on the DVM.

According to the above principle, the relationship between the setting of the function V, A, W ranges and the displays for the AUX input level of 1V are given in Table 4-5. Here the difference between the voltage and current displays is clarified.

As is clear from the Table, a display on the DVM is 31.62 V when the range is set to 30V, but 30.00A in normal case when set to 30A. This is explained as follows.

For the 30V range of input, the V-output is 3V, and the operational output is 3V. As the range setting is not at AUX but at 30V, the gain of $\sqrt{10}/3$ is selected by the range signal code No 4 (100). Thus the display on the DVM becomes $3V \times \sqrt{10}/3$ or 31.62V.

For the 30 A range of input, on the other hand, the A-output is $3V \times 3/\sqrt{10}$, the operational output is $3 \times 3/\sqrt{10}V$, and range code is No 4 (100). Therefore the display on the DVM becomes $3 \times 3/\sqrt{10} \times \sqrt{10}/3$ or 30.00 A. Figure 4-21 shows a complete circuit diagram of AS:3.

V-function

Range	Reading	Unit
AUX	100.00	V
600 V	632.5	V
300 V	316.2	V
100 V	100.00	V
30 V	31.62	V
10 V	10.000	V
3 V	3.162	V

A-function

Range	Reading	Unit
AUX	10.000	A
30 A	30.00	A
10 A	10.000	A
6 A	6.000	A
3 A	3.000	A
1 A	1000.0	mA
0.3 A	300.0	mA
0.1 A	100.0	mA

W-function

A \ V	AUX	600 V	300 V	100 V	30 V	10 V	3 V
AUX	1000.0 W	6.325 kW	3.162 kW	1000.0 W	316.2 W	100.00 W	31.62 W
30 A	3.000 kW	18.97 kW	9.487 kW	3.000 kW	948.7 W	300.0 W	94.87 W
10 A	1000.0 W	6.325 kW	3.162 kW	1000.0 W	316.2 W	100.00 W	31.62 W
6 A	600.0 W	3.795 kW	1.897 kW	600.0 W	189.7 W	60.00 W	18.97 W
3 A	300.0 W	1.897 kW	948.7 W	300.0 W	94.87W	30.00 W	9.487W
1 A	100.00 W	632.5 W	316.2 W	100.00 W	31.62W	10.000 W	3.162W
0.3 A	30.00 W	189.7 W	94.87 W	30.00 W	9.487 W	3.000 W	948.7 mW
0.1 A	10.000 W	63.25 W	31.62 W	10.000 W	3.162 W	1000.0 mW	316.2 mW

Table 4-5 Functions and readings with 1.00V applied to AUX input terminal

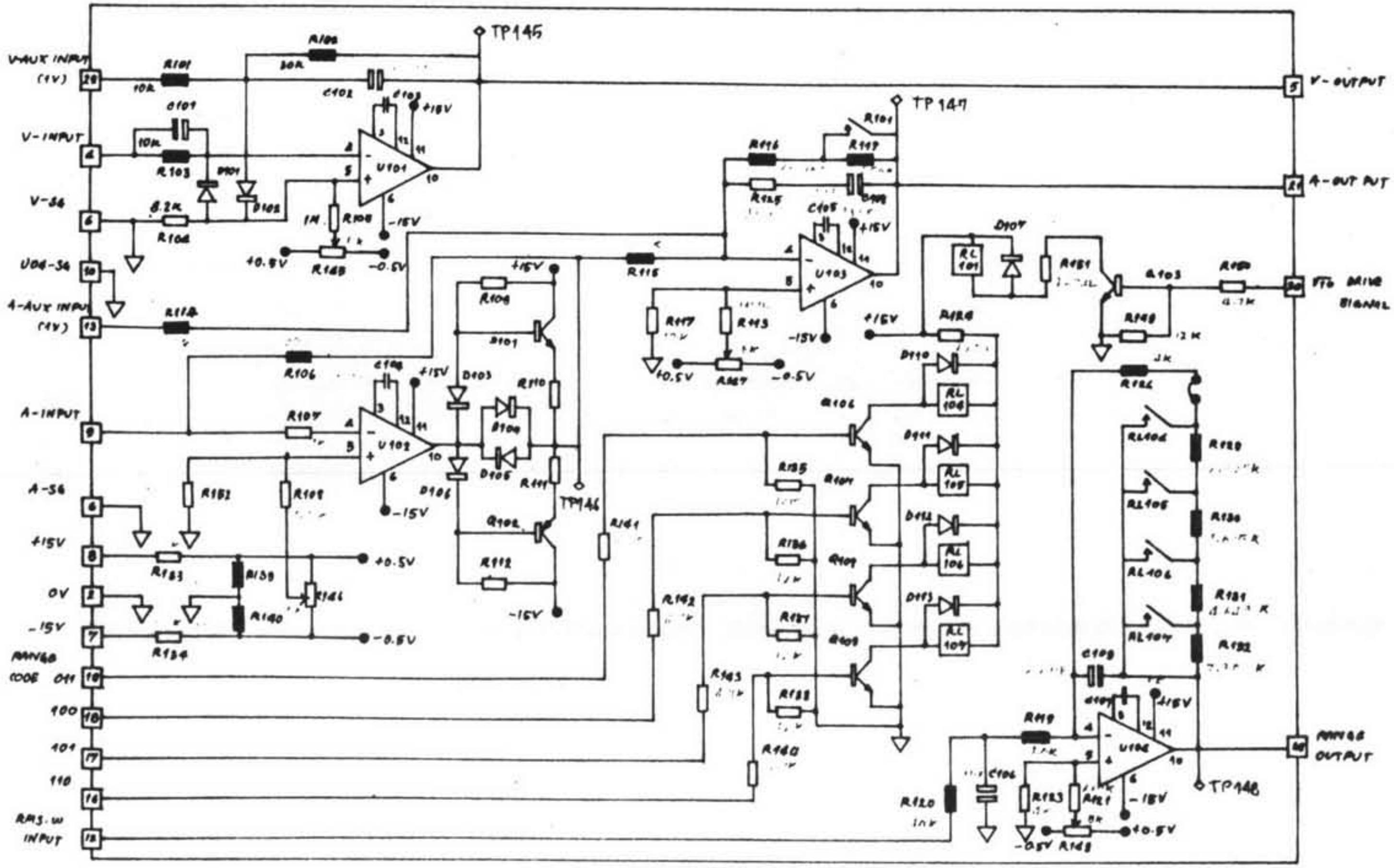


FIG. 4-21 PREAMPLIFIER & RANGING CCT. (AS 3)

4.4.5 Multiplier (AS:4)

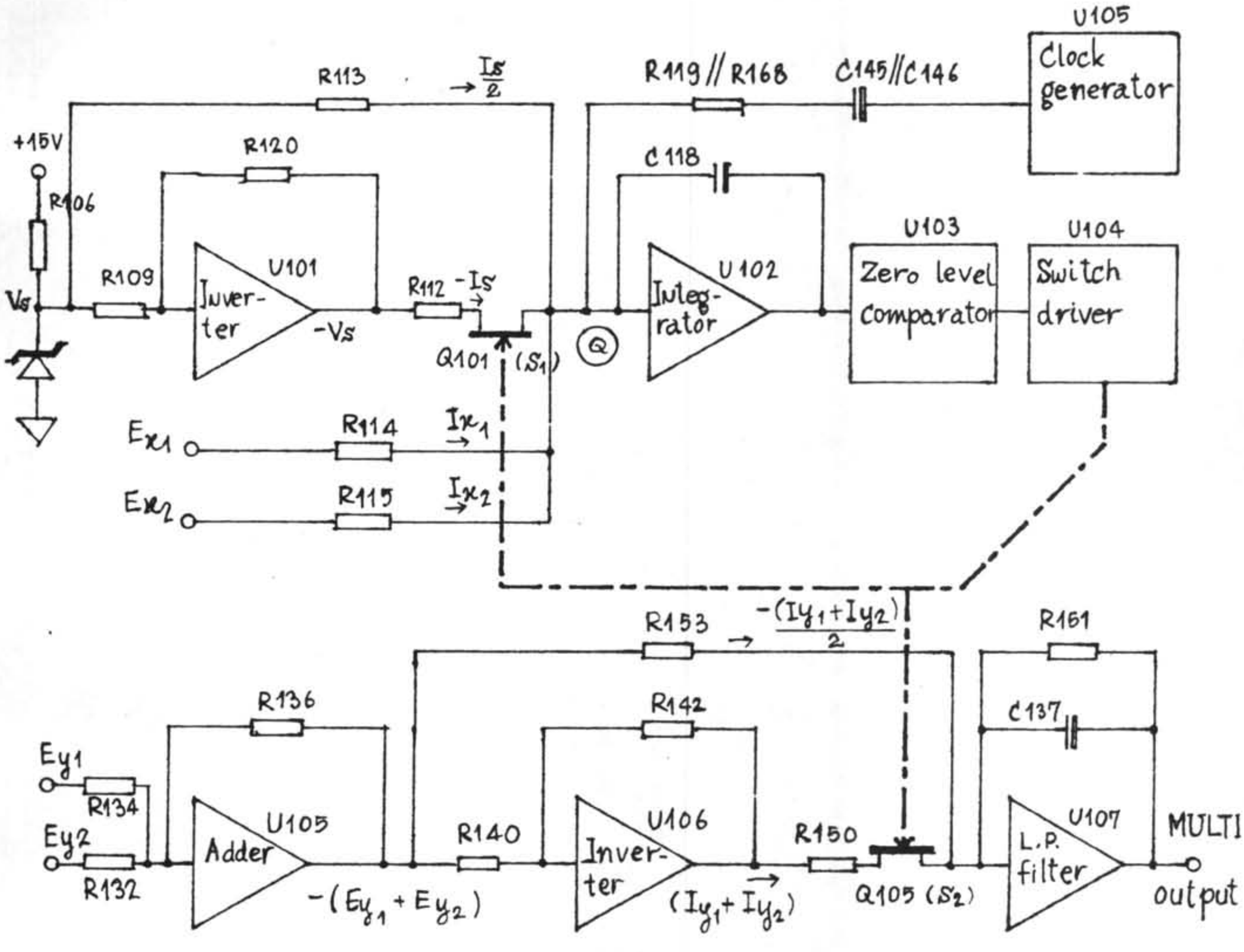


Fig. 4-22 AS:4 Multiplier on one-line diagram

With reference to the theory in subsection 3.3.2 and Fig. 4-22, the calculations and decided values of the main components according to a desired multiplication ratio are as fallows.

A reference voltage Vs consists of a 8.2V- reference diode 1N 430B in series with R106, which is connected to +15 Vdc. After inverted with a unity gain amplifier U101, the output voltage becomes -Vs. From Fig. 4-22 above, the current sum at point Q is

$$Ix_1+Ix_2+\frac{Is}{2} - Is.\frac{T2-T1}{T2+T1} = \frac{Ex1}{R114}+\frac{Ex2}{R115}+\frac{Es}{R113}-\frac{Es}{R112}\cdot\frac{T2-T1}{T2+T1} = 0 \quad (4\text{-}12)$$

where T1 is a time interval during which switch S1 (FET) is opened and T2 is a time interval during which switch S1 (FET) is closed. If we select R113 = 2R112, R114 = R115, Eq. (4-12) yields

$$\frac{T2-T1}{T2+T1} = \left(\frac{Ex1+Ex2}{R115}\right)\frac{R112}{ES}+\frac{1}{2} \quad (4\text{-}13)$$

In the lower part of Fig. 4-22, switch S2 (Q105) is driven in synchronism with S1, the MULTI OUT (Eout) is expressed as

$$Eout = (Ey1+Ey2)\frac{R151}{R153} - (Ey1+Ey2)\frac{R151}{R150}\cdot\frac{T2-T1}{T2+T1} \quad (4\text{-}14)$$

Selecting R153 = 2 R150, and substituting Eq. (4-13). into Eq. (4-14), we obtain

$$\begin{aligned} E\ out &= (Ey1+Ey2)\frac{R151}{2\ R150} - (Ey1+Ey2)\frac{R151}{R150}\left[\left(\frac{Ex1+Ex2}{R115}\right)\frac{R112}{ES}+\frac{1}{2}\right] \\ &= (Ey1+Ey2)\frac{R151}{2\ R150} - (Ey1+Ey2)(Ex1+Ex2)\frac{R112}{R150}\frac{R151}{R115}\cdot\frac{1}{Es} \\ &\quad -(Ey1+Ey2)\frac{R151}{2\ R150} \end{aligned}$$

$$= -\ (Ex1+Ex2)(Ey1+Ey2)\ \frac{R112}{R150}\,\frac{R151}{R115}\cdot\frac{1}{Es}$$

As mentioned in chapter III, the desired ratio for multiplication during power measuring is obtained from Eout $= -\frac{1}{3}$ (Ex1+Ex2)(Ey1+Ey2). Then the actual circuit must be designed so that the term $\frac{R112}{R150}\,\frac{R151}{R115}\cdot\frac{1}{Es}$ is exactly equal to $\frac{1}{3}$.

We can choose many combinations of R112, R151, R150, R115, and Es to obtain the ratio $\frac{1}{3}$. In this design, we choose R112 = 10 kΩ, R150 = 10 kΩ, R115 = 40 kΩ, Es = 8.2 V, and let R151 be a variable. The value of R151 is obtained as

$$R151 = \frac{1}{3}\,\frac{R150.R115}{R112} \times Es$$

$$= \frac{1}{3}\,\frac{10\times 40}{10}\times 8.2$$

$$= 109.3\ k\Omega$$

As shown in Fig. 4-23, R151 is fixed at 100 kΩ and is in series with ten-turn 20-kΩ pot R175 for coarse abjustment and with the 500-Ω R174 for fine adjustment. With this selection, R113, R153 are equal to 20 kΩ, and R114 = R115 = 40 kΩ.

The clock generator generates a pulse train at a frequency of 60 kHz. With this clock frequency, the multiplier can multiply any measuring signals of upto 1.5 kHz. The clock frequency is performed with 4 open-collector NAND gates. The output of the integrator (U102) is compared with zero level at pin 4 of the comparator U103. The power supply of U103 is given so that, every time the output of U102 is lower than 0V, U103 will switch the output from 0 to -5V. This signal is generated by IC 75110 (dual-line driver) to drive n-channel FET Q101 in synchronism with Q105 (all of FETs Q101 to Q108 on this assembly are working as electronci switch). Synchronizing with the switch driving signal, the inverted signal is sent to Q104 and Q106 to discharge the output of U101 and U107 to ground while Q101 and Q105 are cut-off. The complete circuit diagram is shown in Fig. 4-23.

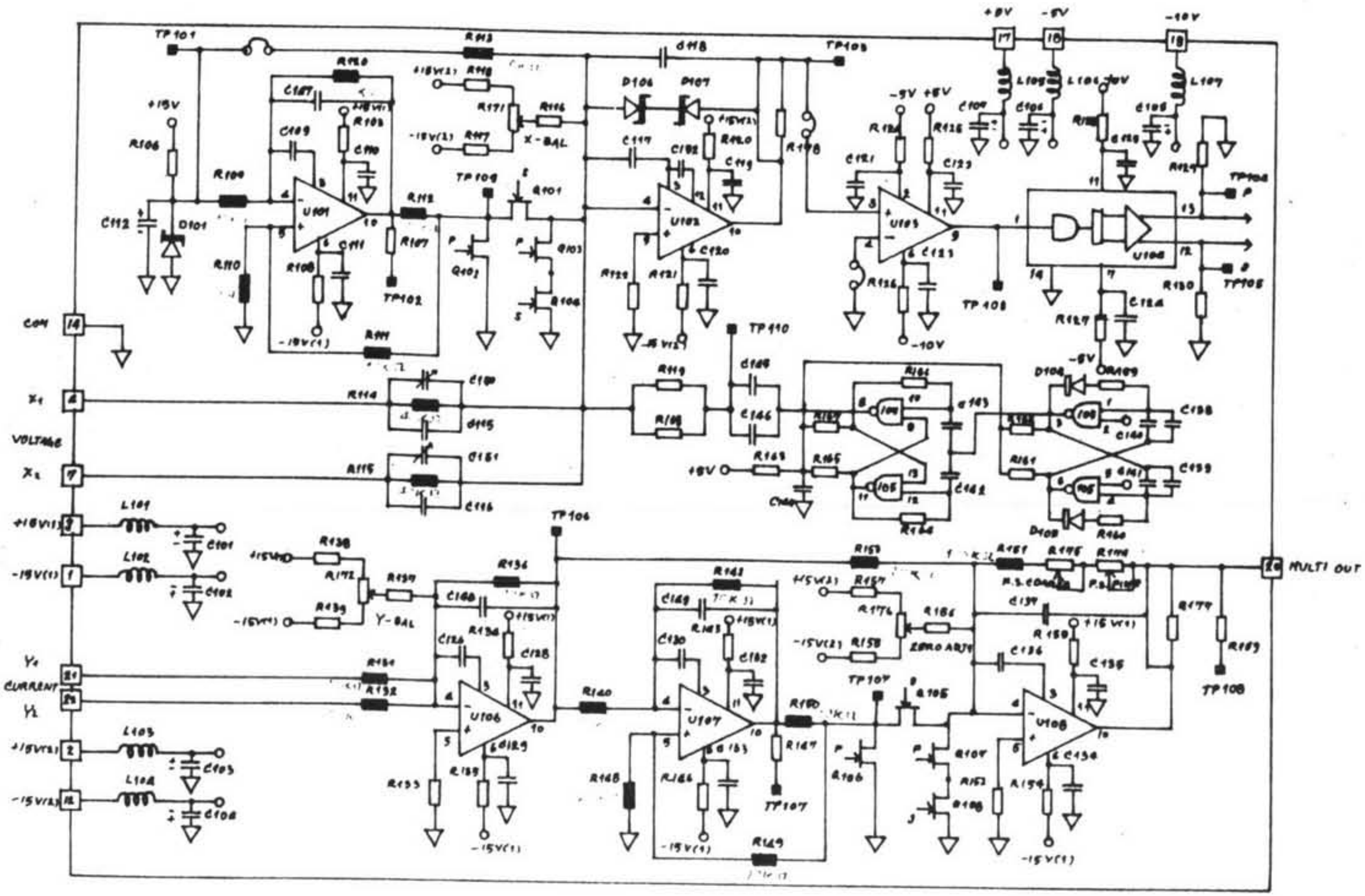


FIG. 4-23 MULTIPLIER (AS:4)

4.4.6 Power Supply -2 (AS:5) for digital zone

The designed circuit and construction are almost the same as those of Power Supply -1 (AS:0). The two power supplies have the same rating and same values of all components. However, no -10V regulator supply is required in Power Supply -2. Moreover, the zener diode (BZY 93) and R121 for current limiter are absent. The two groups of power supply are

(1) +5V/2.5A supplies to all TTL'S and 7-segment displays.

(2) $\pm$15/1.5A and -5V/0.5A supplies to the A-to-D converter assembly (AS:7)

The complete drawing of AS:5 is shown in Fig. 4-24.

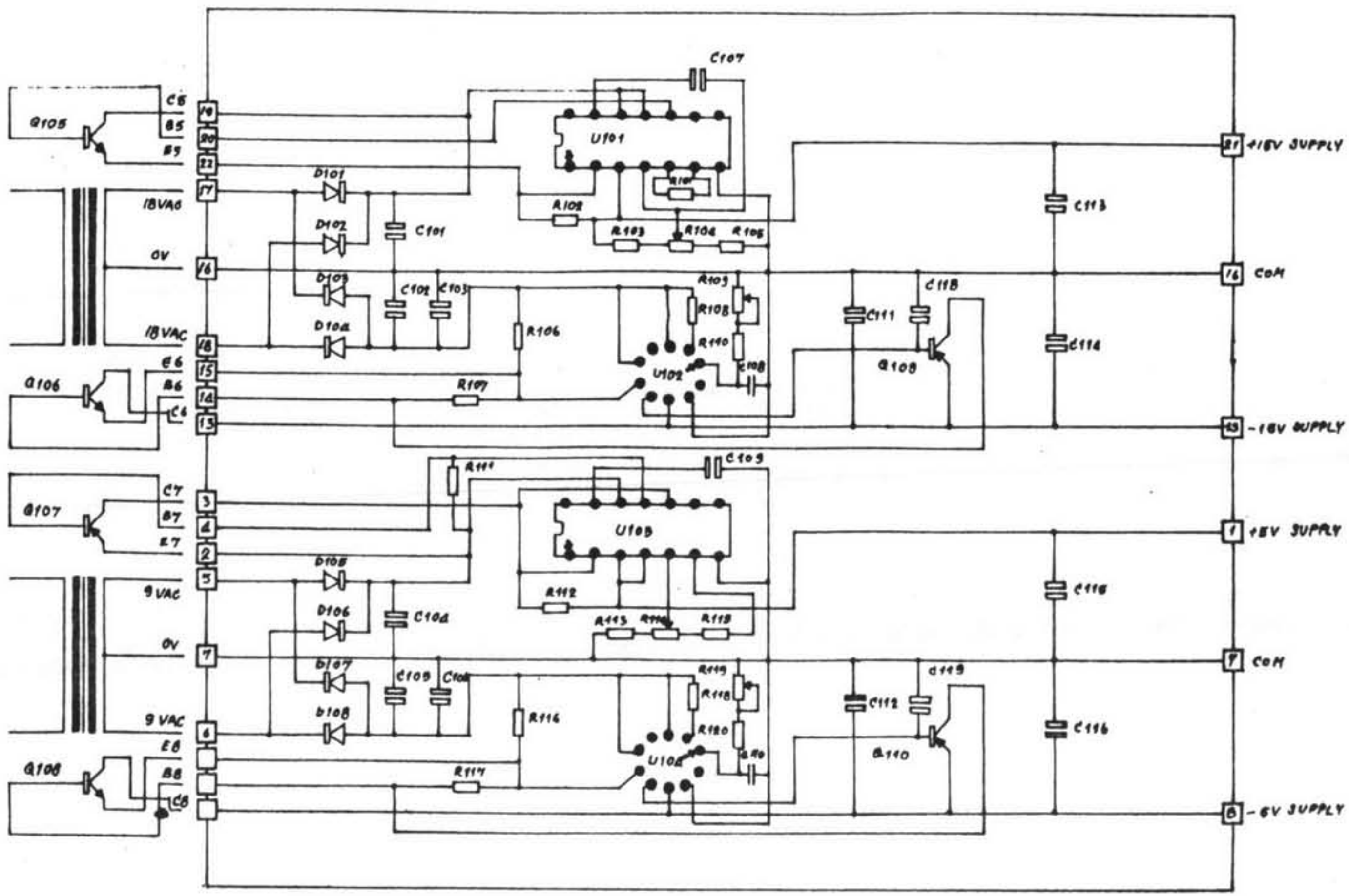


FIG. 4-24 POWER SUPPLY-2 (AS:5)

4.4.7 Control signal isolator (AS:6)

Because all the control signal circuits, i.e., the A-drive, V-drive, $\sqrt{10}$, and ranging control use the +5V supply and on the digital there are many TTL logics and LED displays which require the same level of supply. Every time the reading is sampled, (appx. 3 times/sec) a switching current is high. This current also affects the operation of the analog zone. In order to isolate all the signals transmitted between the analog zone and digital zone, the signals are concentrated here for coding and decoding. All signals are transmitted by means of photocouplers. In this way we can seperat the power supplies on both sides of the photocouplers from each other.

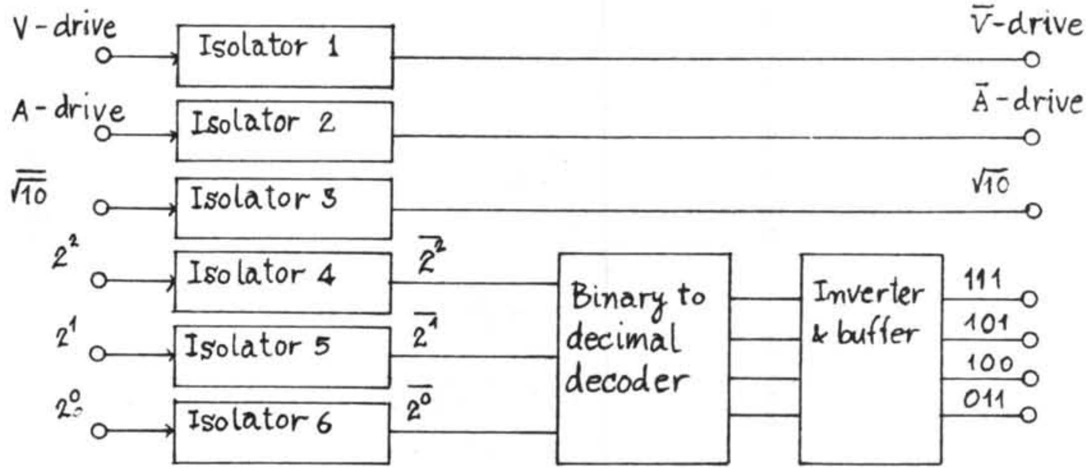
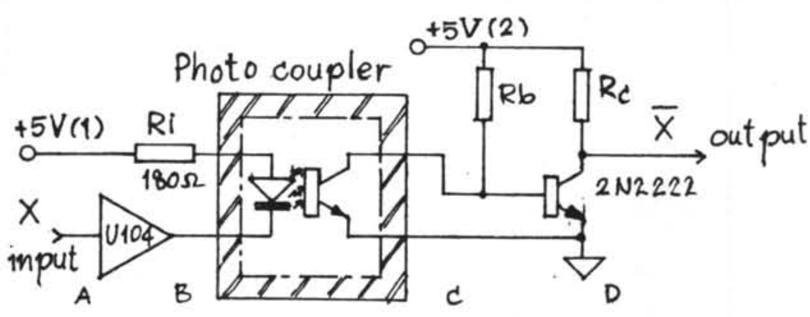


Fig. 4-25 AS:6 Control signal isolator block diagram



normal state

input	output		
A	B	C	D
0	0	0	1
1	1	1	0

Fig. 4-26 Route and truth value of each signal isolator

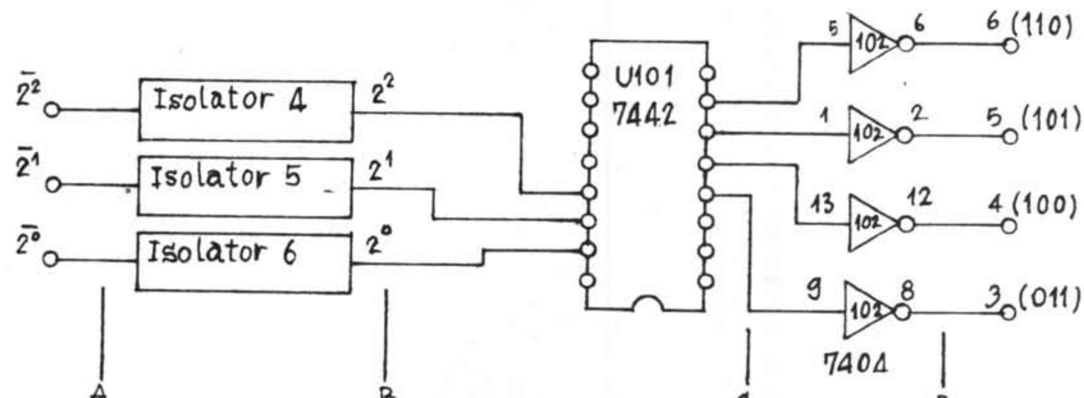
Each isolator (1-6) consists of various components as shown in Fig. 4-26. U104 is TTL buffer gate No 7407, transistor 2N2222 is of a general purpose NPN type, and photocoupler is No 4N26. The calculation is as follows.

$$Ri\ (max) = \frac{5V-\text{ voltage across the photocoupler on the diode side}}{\text{min. required current of the photocoupler}} \tag{4-15}$$

Normally, the voltage across the photocoupler on the diode side = 3V, and minimum required current = 20 mA. So

$$Ri(maximum) = \frac{5-3}{20\times10^{-3}} = 100\Omega$$

Rb and Rc form the bias circuit for the output transistor. Here we must make sure that the output at point X is TTL compatible. In this case Rb = 180 kΩ and Rc = 4.7 kΩ.



normal state

	input			output											
check point	A			B			C				D				
signal name	$\bar{2}^2$	$\bar{2}^1$	$\bar{2}^0$	2^2	2^1	2^0	$\bar{3}$	$\bar{4}$	$\bar{5}$	$\bar{6}$	3	4	5	6	
		0	0		1	1	0				1				3 (011)
truth value	0			1				0				1			4 (100)
	0		0	1		1			0				1		5 (101)
	0	0		1	1					0				1	6 (110)

Fig. 4.27 Routh and truth value of ranging signal isolators

The isolators 4, 5 and 6 have been described above. The input and output are clarify from the truth value shown in Fig. 4-27. The overall diagram of AS:6 is shown in Fig. 4-28.

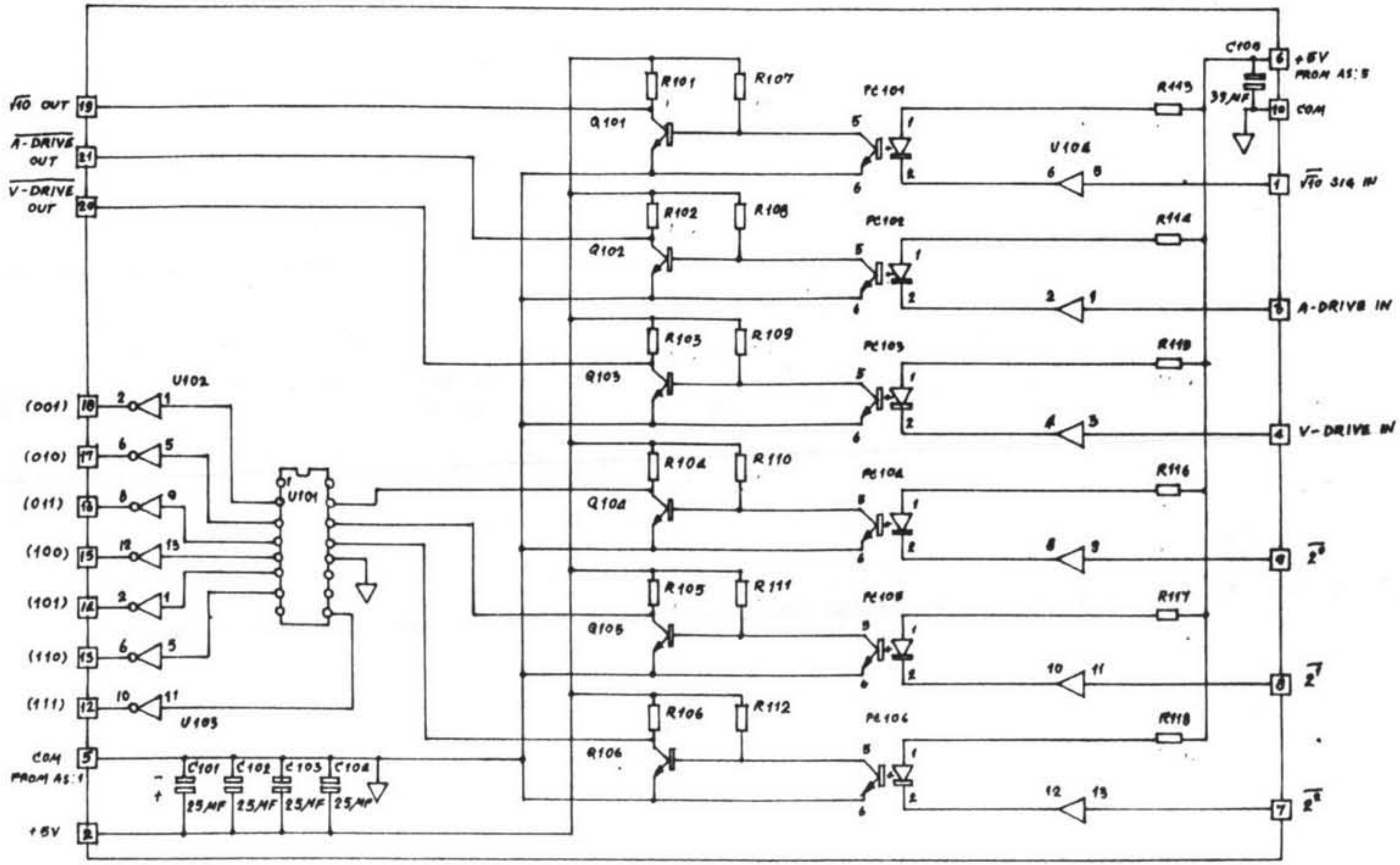


FIG. 4-28 SIGNAL ISOLATOR (AS:6)

4.4.8 A-to-D converter (AS:7)

This A-to-D converter circuit receives the analog main signal from the ranging circuit (ranging output on AS:3) which is constituted by a DC voltage under ranging, converts it into digital form, and sends it out to the display unit (AS:9). For these function, a presision $4\frac{1}{2}$ digit pair of A-to-D converter chips IC 8052A/7103A from INTERSIL are used. In addition to the clock generator circuit, we use a BCD to 7-segment decoder, a polarity driver, and a common display driver to complete the function of the A-to-D converter. Figure 4-29 shows the block diagram and Fig. 4-30 shows the circuit diagram of the A-to-D converter.

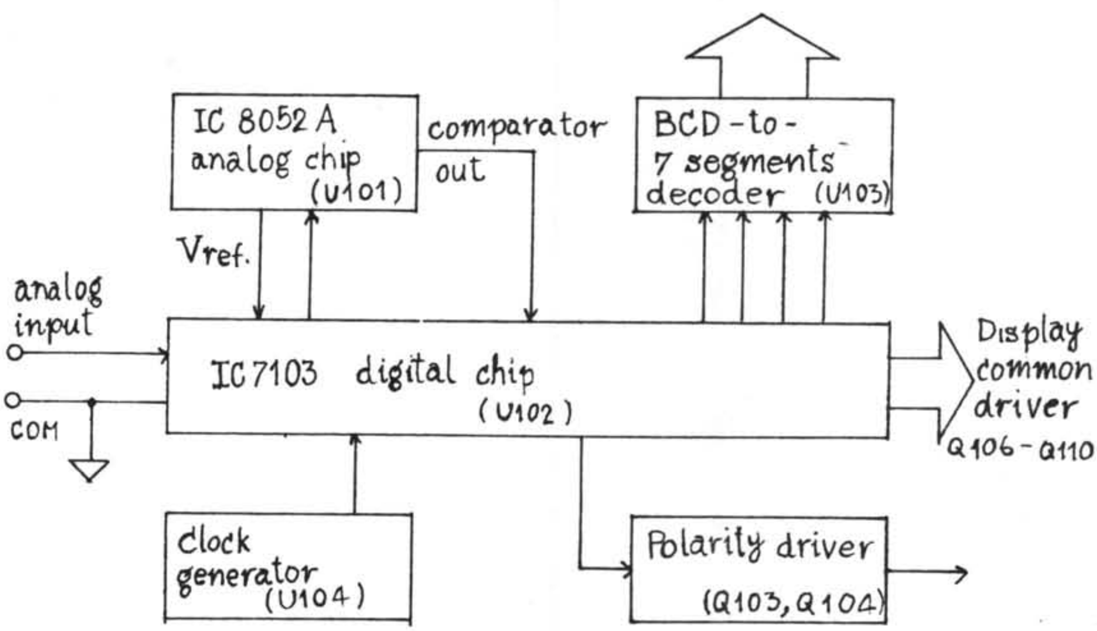


Fig.4-29 AS:7 4-to-D converter block diagram

The reason why IC 8052A/7103A is chosen is because it offers the following features.

1. Accuracy guaranteed to $\pm$ 1 count over entire $\pm$20,000 counts.

2. Guaganteed zero reading for 0 volt input.

3. True polarity at zero count for precise null detection.

4. All outputs are TTL compatible.

5. Blinking display gives visual indication of over-range.

Otherwise this system uses the time-proven dual-slope integration with all its advantages, i.e., non-critical components, high rejection of noise and AC signals, non-critical frequency, almost perfect differential linearity and true ratiomatic readings. At the same time the price is quite low and easy to obtain in local market. For detailed specifications of the IC, please refer to the databook of the manufacturer.

In Fig. 4-30 all of the basic components which are connected to IC 8052A and IC 7103A, such as reference capacitor, integrating capacitor, auto-zero capacitor, reference voltage, and variable resistor are specified from the manufacturer. The clock generator circuit provides a square pulse at a frequency of 120 kHz with 50% duty cycle for 3 reading per second. This frequency can be adjusted by the 10-turn POT R119. Care must be taken in selecting some discrete components of specified type. For instance, a very important characteristic of the integrating capacitor is low dielectric absorbtion. A polypropylene capacitor gave excellent results in this application.

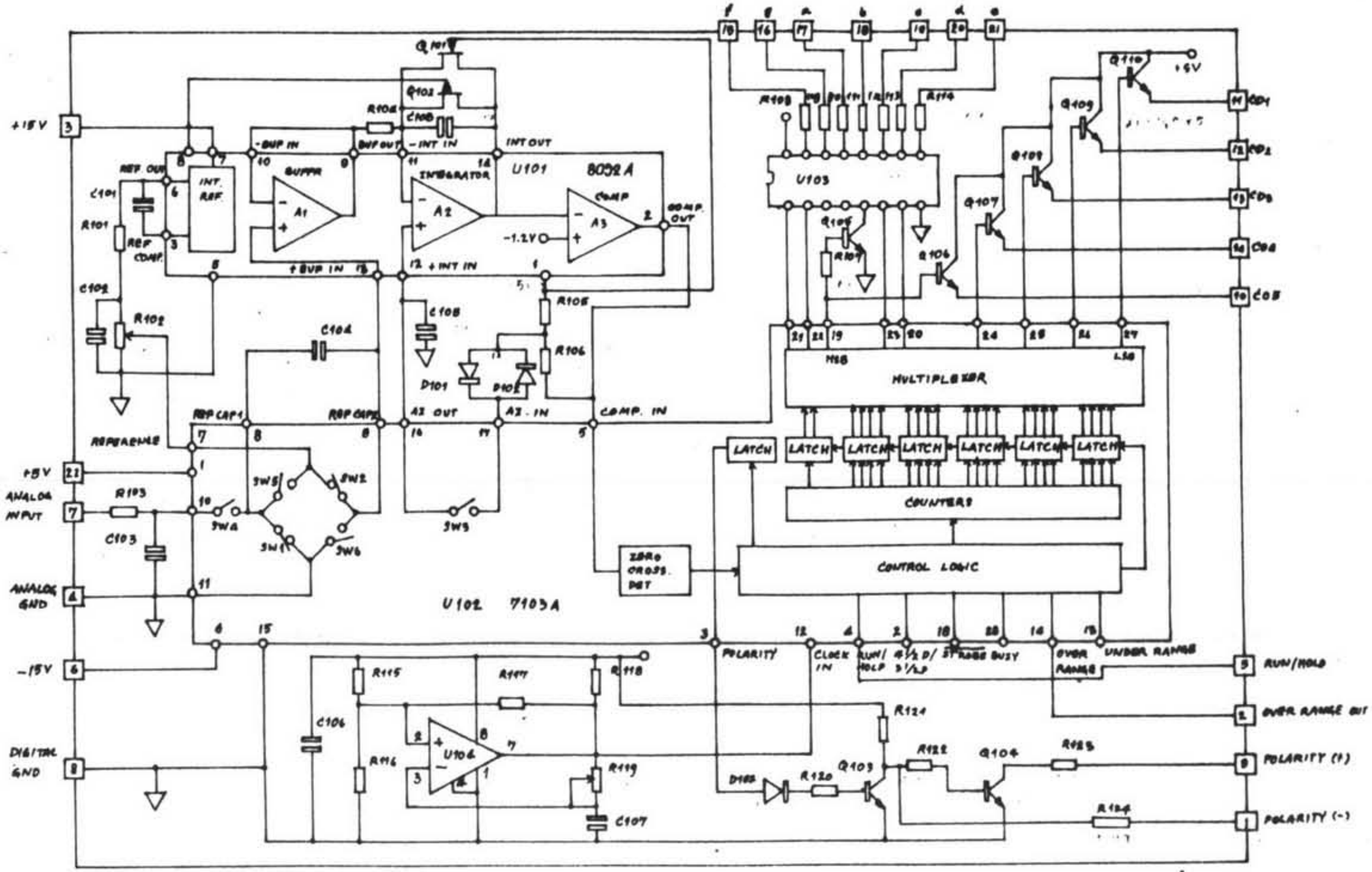


FIG 4-30 A TO D CONVERTER (AS 7)

4.4.9 Point, unit, and ranging encoder (AS:8)

This assembly generates signals of various output levels as shown Fig. 4-31 below by combining the input V, A and W function signals and a range signal determined by the setting of the V and/ or A range selector switch, and sending them out to the intended assemblies through a signal transmission channel as shown in Fig. 4-1. Figure 4-31 shows a block diagram of this assembly.

(1) Drive signal : A-Drive, V-drive, $\sqrt{10}$ signal.

(2) Ranging code : 2^0, 2^1, 2^2

(3) Point signal : For command of the position of decimal point display.

(4) Unit signal : For command of the display of unit (V, mA, A mW, W kW)

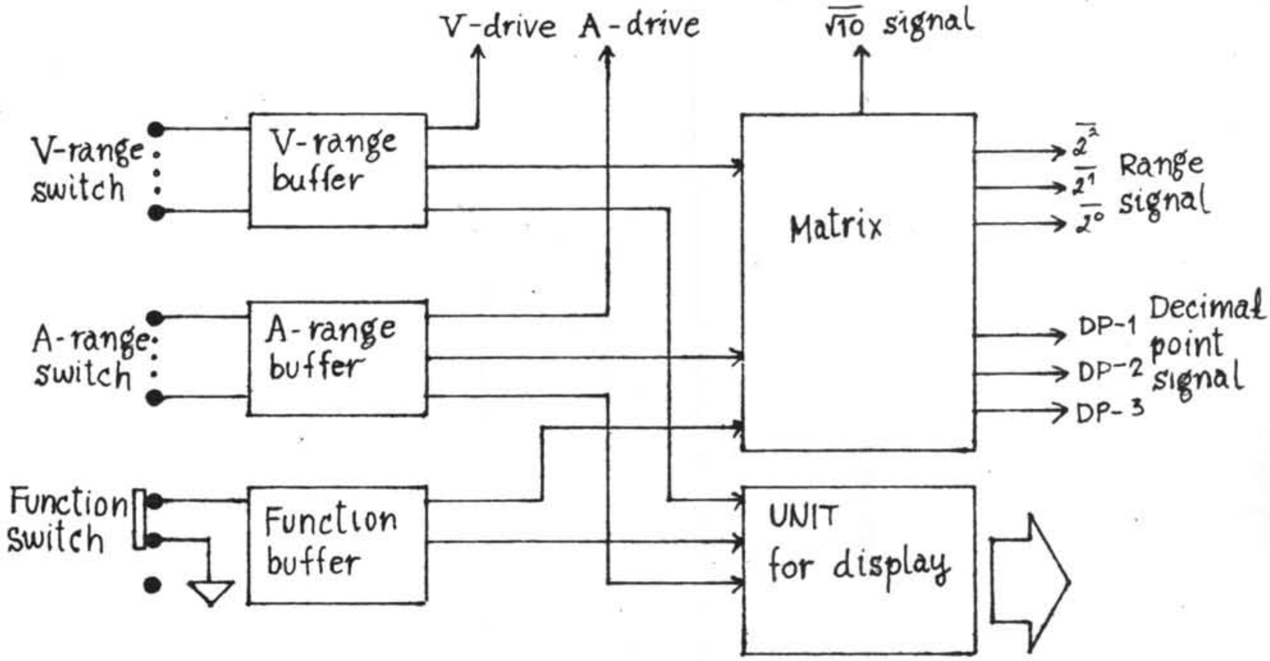


Fig. 4-31 AS:8 Point, unit, and ranging encoder block diagram

The relationship between this output signals and both function and level input signals, and their signal levels are indicated in Table 4-6. In Fig. 4-31 above, the matrix block diagram can be made in two ways. The first uses a combination of logic gates AND, NAND, NOR, and INVERTER to perform all the functions. The corresponding complete circuit is shown in Fig. 4-32. The second employs the EPROM IC No. MM 2708 with 1,024×8 bits format. By using the second method, can reduce the number of ICS on this assembly from 34 chips to 13 chips only. The program content is shown in Table 4-7 and the complete circuit diagram is shown in Fig. 4-33. Actually, in Table 4-7 we require only 7 bits, from A0 to A6 for address and the size of the EPROM is $2^7 = 128$ addresses with 8 data bits. For this property we have many chips from which we can choose, such as MM 1702 or equivalent. However, because the problem of the EPROM programmer machine and the ability to have this EPROM in local market, the author can have only the 1,024×8 bit IC No. MM 2708, which is of a larger size than the above mentioned but whose performance is nearly the same.

function	V-range	A-range	Input																Output														
			funct			V-range						A-range							brive			ranging			point			unit					
			V	A	W	$\overline{3}$	$\overline{10}$	$\overline{30}$	$\overline{100}$	$\overline{300}$	$\overline{600}$	$\overline{0.1}$	$\overline{0.3}$	$\overline{1}$	$\overline{3}$	$\overline{6}$	$\overline{10}$	$\overline{30}$	A	V	$\overline{\sqrt{10}}$	$\overline{2^0}$	$\overline{2^1}$	$\overline{2^2}$	1	2	3	V	A	mA	kW	W	mW
	3		0			0														1		0					1	1					
	10		0				0													1							1	1					
	30		0					0												1		0				1		1					
V	100	*	0						0											1						1		1					
	300		0							0										1		0			1			1					
	600		0								0									1		0	0		1			1					
		0.1		0								0							1							1				1			
		0.3		0									0						1		0	0			1					1			
		1		0										0					1						1					1			
A	*	3		0											0				1		0	0					1		1				
		6		0												0			1		0	0	0				1		1				
		10		0													0		1								1		1				
		30		0														0	1		0	0				1			1				
		0.1			0	0						0										0			1								1
		0.3			0	0							0								0				1								1
		1			0	0								0								0					1					1	
W	3	3			0	0									0						0						1					1	
		6			0	0										0					0		0	0		1						1	
		10			0	0											0					0				1						1	
		30			0	0												0			0					1						1	
		0.1			0		0					0													1								1
		0.3			0		0						0								0	0					1					1	
		1			0		0							0													1					1	
W	10	3			0		0								0						0	0				1						1	
		6			0		0									0					0	0	0			1						1	
		10			0		0										0									1						1	
		30			0		0											0			0	0			1							1	
		0.1			0			0				0										0					1					1	
		0.3			0			0					0								0						1					1	
		1			0			0						0								0				1						1	
W	30	3			0			0							0						0					1						1	
		6			0			0								0					0		0	0	1							1	
		10			0			0									0					0			1							1	
		30			0			0										0			0				1							1	
		0.1			0				0			0															1					1	
		0.3			0				0				0								0	0				1						1	
		1			0				0					0												1						1	
W	100	3			0				0						0						0	0			1							1	
		6			0				0							0					0	0	0		1							1	
		10			0				0								0								1							1	
		30			0				0									0			0	0					1				1		
		0.1			0					0		0										0				1						1	
		0.3			0					0			0								0					1						1	
		1			0					0				0								0			1							1	
W	300	3			0					0					0						0				1							1	
		6			0					0						0					0		0	0			1				1		
		10			0					0							0					0					1				1		
		30			0					0								0			0						1				1		
		0.1			0						0	0										0	0			1						1	
		0.3			0						0		0								0		0	0	1							1	
		1			0						0			0								0	0		1							1	
W	600	3			0						0				0						0		0	0			1				1		
		6			0						0					0					0	0		0			1				1		
		10			0						0						0					0	0				1				1		
		30			0						0							0			0					1					1		

Table 4-6 input and output signals of AS:8

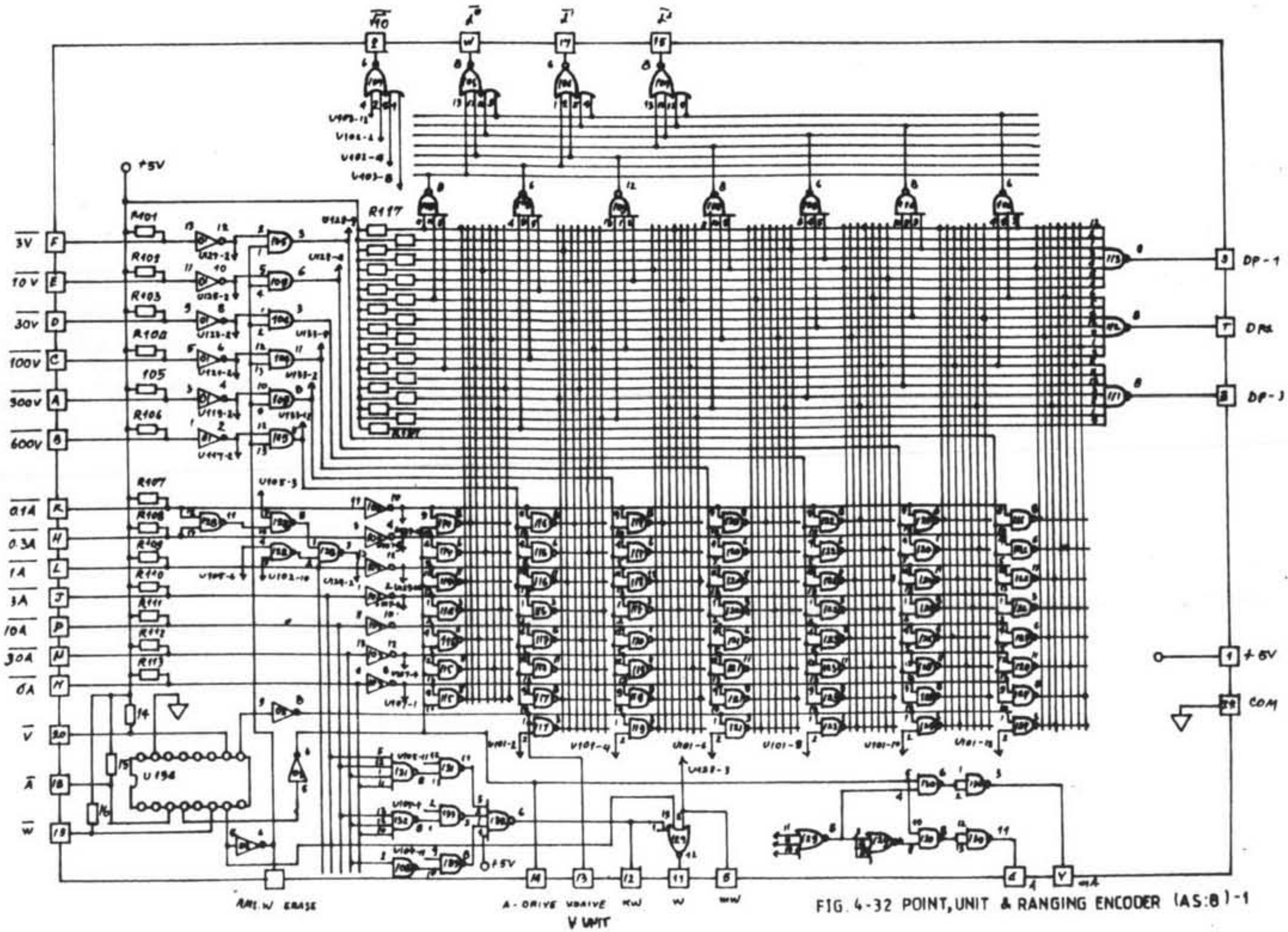


FIG. 4-32 POINT, UNIT & RANGING ENCODER (AS:8)-1

FUNCTION	V-RANGE	A-RANGE	DECODED ADDRESS							ADR (HEXA)		OUTPUT DATA								DATA (HEXA)	
			W	V			A					RANGE			PT		UNIT				
			A6	A5	A4	A3	A2	A1	A0			B7	B6	B5	B4	B3	B2	B1	B0		
	3		0	1	1	0	1	1	1	3	7	0	1	1	1	0	1	1	0	7	6
	10		0	1	0	1	1	1	1	2	F	1	1	1	1	0	1	1	0	F	6
V	30	*	0	1	0	0	1	1	1	2	7	0	1	1	0	1	1	1	0	6	E
	100		0	0	1	1	1	1	1	1	F	1	1	1	0	1	1	1	0	E	E
	300		0	0	1	0	1	1	1	1	7	0	1	1	0	0	1	1	0	6	6
	600		0	0	0	1	1	1	1		F	0	0	1	0	0	1	1	0	2	6
		0.1	0	1	1	1	1	1	0	3	E	1	1	1	0	1	1	0	0	E	C
		0.3	0	1	1	1	1	0	1	3	D	0	1	1	0	0	1	0	0	6	4
		1	0	1	1	1	1	0	0	3	C	1	1	1	0	0	1	0	0	E	4
A	*	3	0	1	1	1	0	1	1	3	B	0	1	1	1	0	1	0	1	7	5
		6	0	1	1	1	0	1	0	3	A	0	0	1	1	0	1	0	1	3	5
		10	0	1	1	1	0	0	1	3	9	1	1	1	1	0	1	0	1	F	5
		30	0	1	1	1	0	0	0	3	8	0	1	1	0	1	1	0	1	6	D
		0.1	1	1	1	0	1	1	0	7	6	0	1	1	0	0	0	0	1	6	1
		0.3	1	1	1	0	1	0	1	7	5	1	1	1	0	0	0	0	1	E	1
		1	1	1	1	0	1	0	0	7	4	0	1	1	1	0	0	1	0	7	2
W	3	3	1	1	1	0	0	1	1	7	3	1	1	1	1	0	0	1	0	F	2
		6	1	1	1	0	0	1	0	7	2	1	0	0	0	1	0	1	0	8	A
		10	1	1	1	0	0	0	1	7	1	0	1	1	0	1	0	1	0	6	A
		30	1	1	1	0	0	0	0	7	0	1	1	1	0	1	0	1	0	E	A
		0.1	1	1	0	1	1	1	0	6	E	1	1	1	0	0	0	0	1	E	1
		0.3	1	1	0	1	1	0	1	6	D	0	1	1	1	0	0	1	0	7	2
		1	1	1	0	1	1	0	0	6	C	1	1	1	1	0	0	1	0	F	2
W	10	3	1	1	0	1	0	1	1	6	B	0	1	1	0	1	0	1	0	6	A
		6	1	1	0	1	0	1	0	6	A	0	0	1	0	1	0	1	0	2	A
		10	1	1	0	1	0	0	1	6	9	1	1	1	0	1	0	1	0	E	A
		30	1	1	0	1	0	0	0	6	8	0	1	1	0	0	0	1	0	6	2

FUNC-TION	V-RANGE	A-RANGE	DECODED ADDRESS							ADR (HEXA)	OUTPUT DATA								DATA (HEXA)
			W	V		A					RANGE			PT		UNIT			
			A6	A5	A4	A3	A2	A1	A0		B7	B6	B5	B4	B3	B2	B1	B0	
W	30	0.1	1	1	0	0	1	1	0	66	0	1	1	1	0	0	1	0	72
		0.3	1	1	0	0	1	0	1	65	1	1	1	1	0	0	1	0	F2
		1	1	1	0	0	1	0	0	64	0	1	1	0	1	0	1	0	6A
		3	1	1	0	0	0	1	1	63	1	1	1	0	1	0	1	0	EA
		6	1	1	0	0	0	1	0	62	1	0	0	0	0	0	1	0	82
		10	1	1	0	0	0	0	1	61	0	1	1	0	0	0	1	0	62
		30	1	1	0	0	0	0	0	60	1	1	1	0	0	0	1	0	E2
W	100	0.1	1	0	1	1	1	1	0	5E	1	1	1	1	0	0	1	0	F2
		0.3	1	0	1	1	1	0	1	5D	0	1	1	0	1	0	1	0	6A
		1	1	0	1	1	1	0	0	5C	1	1	1	0	1	0	1	0	EA
		3	1	0	1	1	0	1	1	5B	0	1	1	0	0	0	1	0	62
		6	1	0	1	1	0	1	0	5A	0	0	1	0	0	0	1	0	22
		10	1	0	1	1	0	0	1	59	1	1	1	0	0	0	1	0	E2
		30	1	0	1	1	0	0	0	58	0	1	1	1	0	0	1	1	73
W	300	0.1	1	0	1	0	1	1	0	56	0	1	1	0	1	0	1	0	6A
		0.3	1	0	1	0	1	0	1	55	1	1	1	0	1	0	1	0	EA
		1	1	0	1	0	1	0	0	54	0	1	1	0	0	0	1	0	62
		3	1	0	1	0	0	1	1	53	1	1	1	0	0	0	1	0	E2
		6	1	0	1	0	0	1	0	52	1	0	0	1	0	0	1	1	93
		10	1	0	1	0	0	0	1	51	0	1	1	1	0	0	1	1	73
		30	1	0	1	0	0	0	0	50	1	1	1	1	0	0	1	1	F3
W	600	0.1	1	0	0	1	1	1	0	4E	0	0	1	0	1	0	1	0	2A
		0.3	1	0	0	1	1	0	1	4D	1	0	0	0	0	0	1	0	82
		1	1	0	0	1	1	0	0	4C	0	0	1	0	0	0	1	0	22
		3	1	0	0	1	0	1	1	4B	1	0	0	1	0	0	1	1	93
		6	1	0	0	1	0	1	0	4A	0	1	0	1	0	0	1	1	53
		10	1	0	0	1	0	0	1	49	0	0	1	1	0	0	1	1	33
		30	1	0	0	1	0	0	0	48	1	0	0	0	1	0	1	1	83

Table 4-7 AS:8, Program mapping for EPROM application

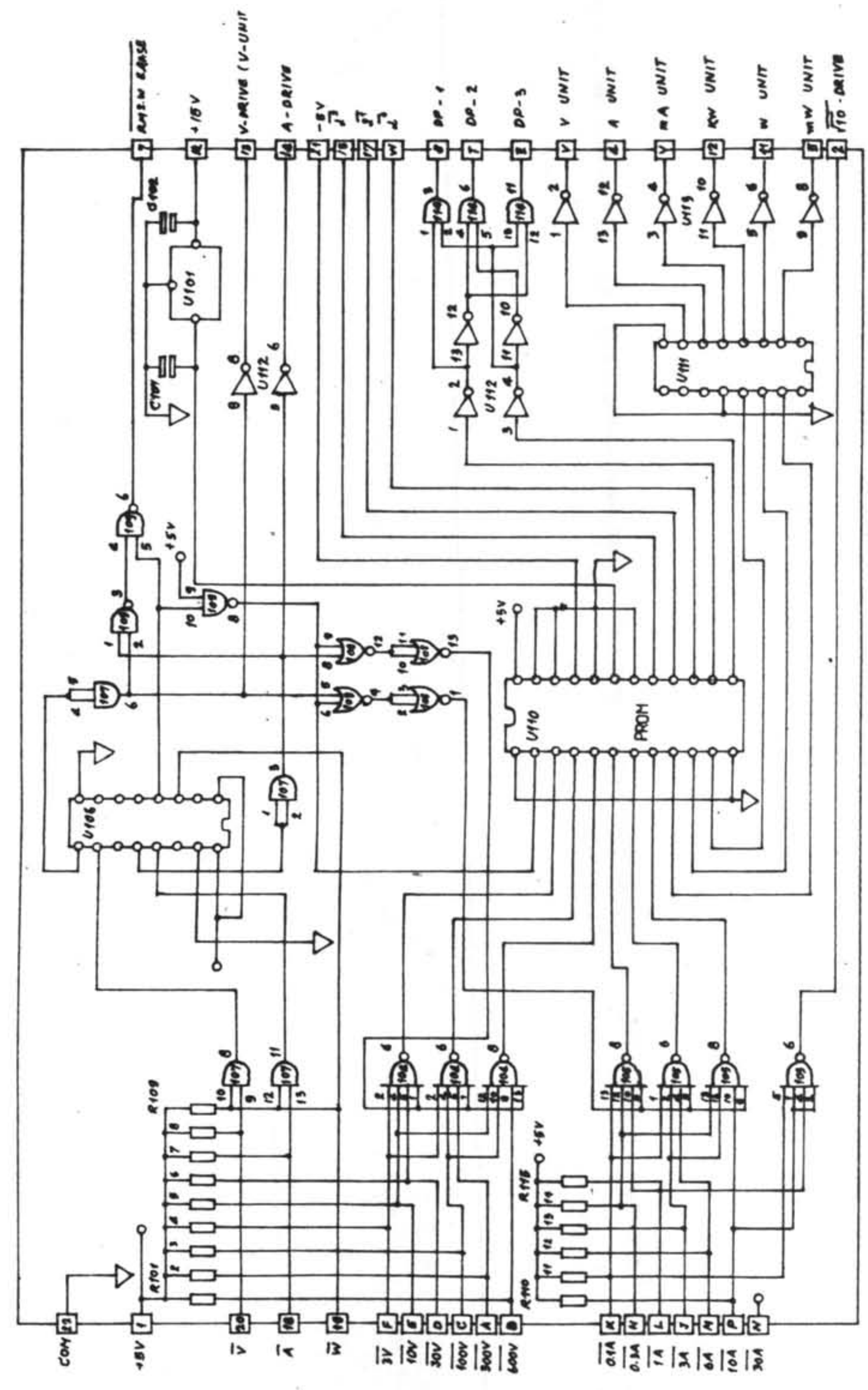


FIG. 4-33 POINT, UNIT & RANGING ENCODER (AS-8)-2

4.4.10 Display unit (AS:9)

The assembly displays measured value in $4\frac{1}{2}$ digits by a 7- segment LED of common anode type. The driving signal is obtained from A-to-D converter (AS:7), and those signals for the unit and dicimal point displays from AS:8.

All buffer/inverter gates for the indicator LED driver are IC 7404 because each indicator LED requires approximately 10 mA to turn on its light. To limit this amount of current we use a 180-Ω resistor. The complete circuit diagram is shown in Fig. 4-34.

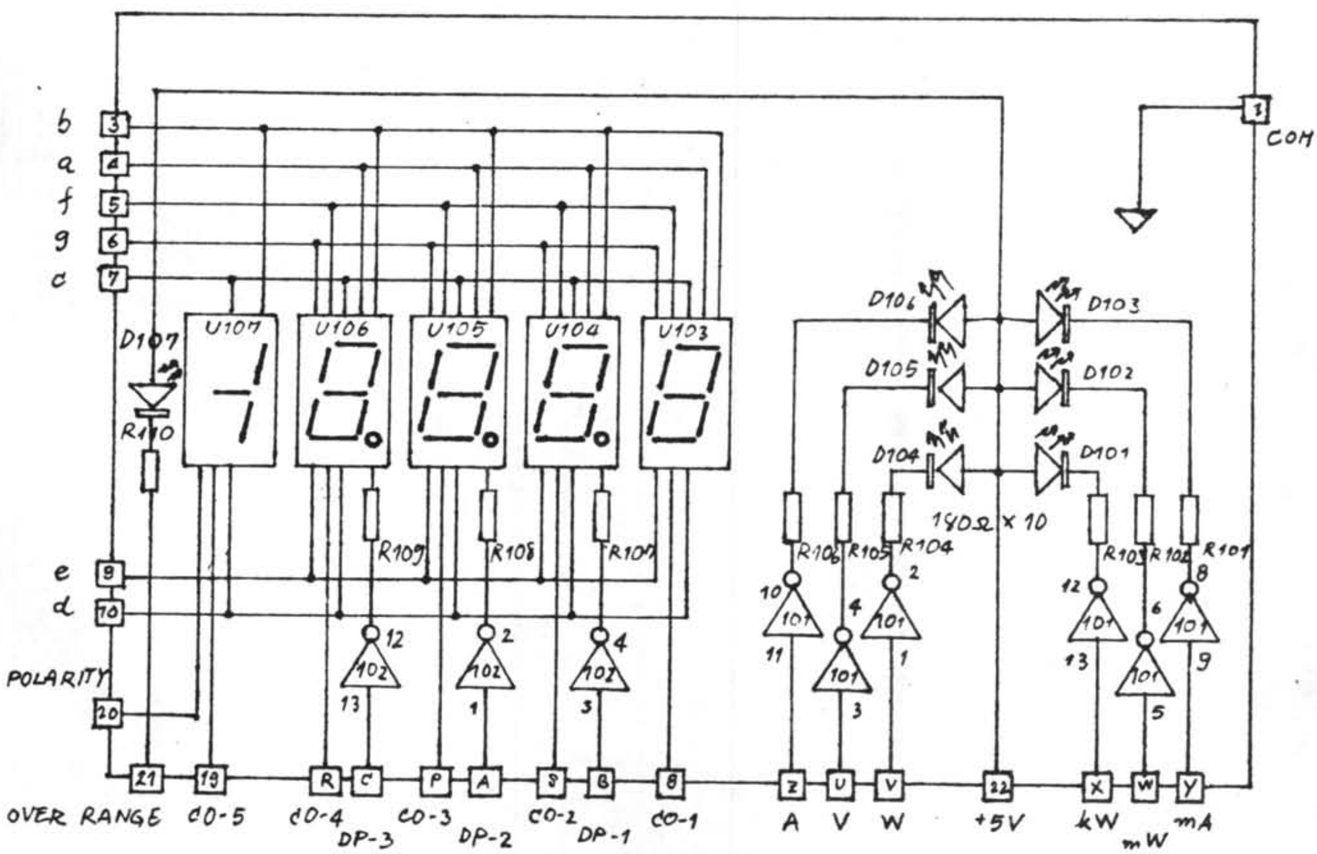


Fig. 4-34 Display (AS:9)

4.4.11 Bypass transistor card (AS:10)

This assembly consists only of the bypass transistors of all regulators for power supply AS:1 and AS:5. These transistors are attached to the aluminium heat-sink and are applied with the thermal-solution to improve power dissipation. The layout of the card is as shown in Fig. 4-35.

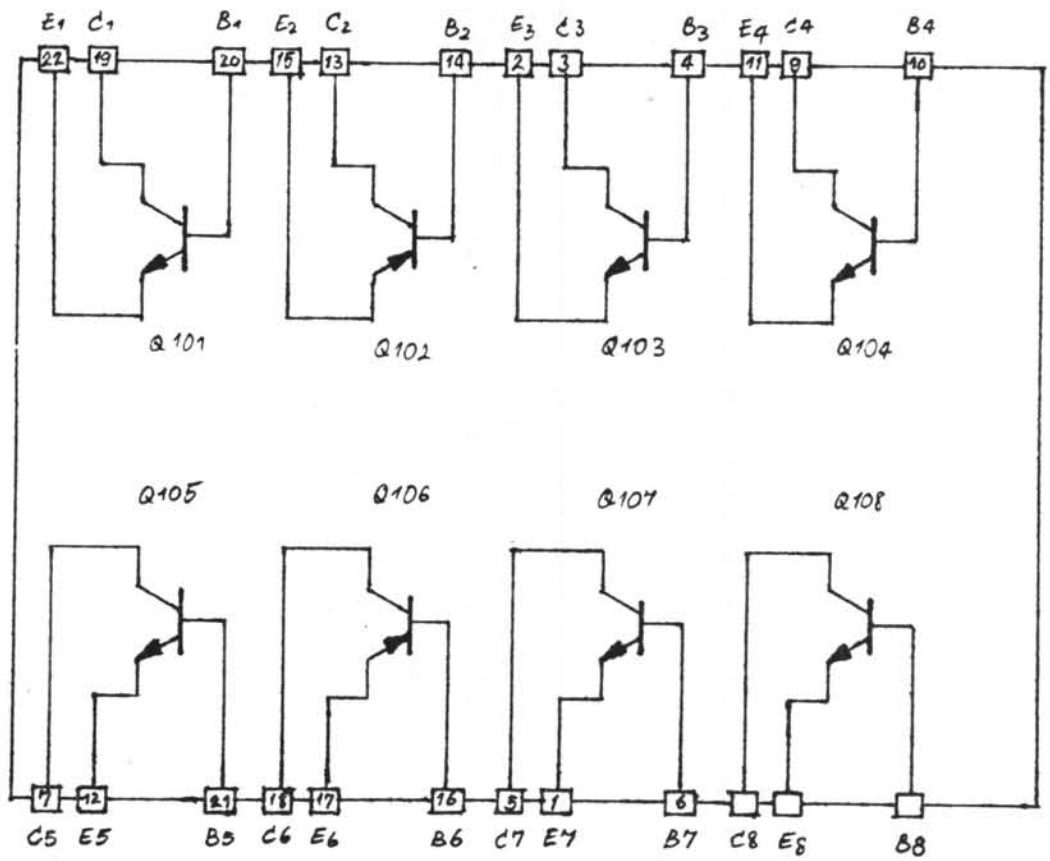


Fig. 4-35 Bypass transistors card (AS:10)

To complete the construction step, the component list and component layout are given in Appendix C and Appendix D. The interconnection and wiring list are in Appendix B. Also the detail of the calibration of this AC power meter is shown in chapter V.