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# NOVEL TOPOLOGIES FOR THREE-LEVEL BACK-TO-BACK CONVERTERS BASED ON MATRIX CONVERTER THEORY

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กรวิชญ์ นิยมเสถียร : โครงสร้างใหม่ของคอนเวอร์เตอร์สามระดับแบบหลังชนหลังโดยอาศัยทฤษฎีเมทริกซ์คอนเวอร์เตอร์. (NOVEL TOPOLOGIES FOR THREE-LEVEL BACK-TO-BACK CONVERTERS BASED ON MATRIX CONVERTER THEORY) อ.ที่ปรึกษาวิทยานิพนธ์หลัก : ผศ.ดร.สมบูรณ์ แสงวงค์วาณิชย์, 136 หน้า.

การใช้เทคนิคการมอดูเลตความกว้างพัลส์ความถี่สูงทั้งในส่วนของวงจรเรียงกระแสและวงจรอินเวอเตอร์ในคอนเวอร์เตอร์สามระดับแบบหลังชนหลังแบบดั้งเดิมทำให้เกิดกำลังสูญเสียจากการสวิตช์อย่างมาก ในการแก้ปัญหาดังกล่าววิทยานิพนธ์นี้ได้นำเสนอสองโครงสร้างใหม่ของคอนเวอร์เตอร์สามระดับแบบหลังชนหลังได้แก่ เมทริกซ์คอนเวอร์เตอร์แบบอ้อมสามระดับ และคอนเวอร์เตอร์สามระดับแบบหลังชนหลังแบบสมมาตร พร้อมทั้งวิธีการมอดูเลต โดยพัฒนามาจากทฤษฎีการมอดูเลตความกว้างพัลส์แบบพาหะคู่สำหรับเมทริกซ์คอนเวอร์เตอร์ วงจรเรียงกระแสในคอนเวอร์เตอร์สามระดับแบบหลังชนหลังแบบโครงสร้างใหม่จะสวิตช์ที่ความถี่สายกำลังเพื่อสร้างแรงดันสามระดับเรียงจากมากไปน้อยที่บัสไฟตรงสามระดับ ในขณะที่วงจรอินเวอร์เตอร์จะสวิตช์ที่ความถี่สูงและใช้เทคนิคการมอดูเลตแบบความกว้างพัลส์เพื่อสร้างแรงดันด้านออก เพราะฉะนั้นกำลังสูญเสียจากการสวิตช์และการแทรกสอดทางแม่เหล็กไฟฟ้าที่เกิดจากวงจรเรียงกระแสของคอนเวอร์เตอร์โครงสร้างใหม่จะลดลงอย่างมากเทียบกับโครงสร้างแบบดั้งเดิม และในกรณีที่ต้องการแรงดันด้านออกสูง วงจรเรียงกระแสสามารถเปลี่ยนมาใช้เทคนิคการมอดูเลตความกว้างพัลส์ที่ความถี่สูงในลักษณะเดียวกับโครงสร้างแบบดั้งเดิมได้ ผลการจำลองการทำงานชี้ให้เห็นว่าคอนเวอร์เตอร์ทั้งสองโครงสร้างที่นำเสนอสามารถทำงานได้อย่างดีตามสมรรถนะพื้นฐานของวงจรแปลงผันไฟสลับ-ไฟสลับ และเกิดกำลังสูญเสียจากการสวิตช์ในวงจรเรียงกระแสน้อยมาก นอกจากนี้เครื่องต้นแบบของคอนเวอร์เตอร์สามระดับแบบหลังชนหลังแบบสมมาตรที่พัฒนาขึ้นสามารถทำงานได้เป็นอย่างดีสอดคล้องกับผลทางทฤษฎี

ภาควิชา วิศวกรรมไฟฟ้า ลายมือชื่อ .....

สาขาวิชา วิศวกรรมไฟฟ้า ลายมือชื่อ อ.ที่ปรึกษาวิทยานิพนธ์หลัก .....

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KEYWORDS : THREE-LEVEL BACK-TO-BACK CONVERTER / INDIRECT MATRIX CONVERTER / DOUBLE-CARRIER-BASED PWM

KORAWICH NIYOMSATIAN : NOVEL TOPOLOGIES FOR THREE-LEVEL BACK-TO-BACK CONVERTERS BASED ON MATRIX CONVERTER THEORY. ADVISOR : ASST. PROF. SOMBOON SANGWONGWANICH, Ph. D., 136 pp.

To reduce the increase in switching losses caused by PWM operations at both the input and output stages of three-level back-to-back (3L-BTB) converters, two novel topologies of 3L-BTB converters, which are three-level indirect matrix converter (3L-IMC) and the symmetrical three-level back-to-back (S3L-BTB) converter, together with a new modulation strategy are developed. The proposed 3L-BTB converters are based on the double-carrier-based dipolar PWM theory of the matrix converters, and are comprised of a fundamental-frequency switching rectifier and a PWM inverter. The slow-switching rectifier is employed to generate the required max-mid-min dc links for the PWM inverter stage. The switching losses and EMI at the input are significantly reduced as compared to those of the conventional PWM rectifier. Moreover, the topology of the S3L-BTB converter allows the rectifier to be operated in the usual PWM mode and becomes the conventional PWM 3L-BTB converter if required. Simulations are conducted, and the results confirm the performances of the proposed converters as AC/AC converters and their benefit in loss reduction. The laboratory prototype of the S3L-BTB converter is also constructed and tested. The experimental results are in good agreement with the theoretical results.

Department : Electrical Engineering Student's Signature .....
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# List of Abbreviations

## Variables

| | |
|---|---|
| $*$ | commanded value |
| $R, S, T$ | Instantaneous input terminal voltages |
| $v_R, v_S, v_T$ | Instantaneous supply voltages |
| $i_R, i_S, i_T$ | Instantaneous supply currents |
| $u, v, w$ | Instantaneous output voltages |
| $u^*, v^*, w^*$ | Instantaneous commanded output voltages |
| $v_z$ | Instantaneous output voltages |
| $i_u, i_v, i_w$ | Instantaneous output currents for phase $u$,$v$,$w$ |
| $v_{max}, v_{mid}, v_{min}$ | Instantaneous dc-link voltages |
| $i_{max}, i_{mid}, i_{min}$ | Instantaneous dc-link currents of the 3L-IMC |
| $i_{max}^{(r)}, i_{mid}^{(r)}, i_{min}^{(r)}$ | Instantaneous dc-link currents at the rectifier side of the S3L-BTB converter |
| $i_{max}^{(i)}, i_{mid}^{(i)}, i_{min}^{(i)}$ | Instantaneous dc-link currents at the inverter side of the S3L-BTB converter |
| $\mathbf{v}_i$ | Input voltage vector |
| $\mathbf{v}_o$ | Output voltage vector |
| $\mathbf{v}_{dc}$ | Dc-link voltage vector |
| $\Vert \bullet \Vert$ | Magnitude of a vector |
| $\mathbf{i}_i$ | Input current vector |
| $\mathbf{i}_o$ | Output current vector |
| $\mathbf{i}_{dc}$ | Dc-link current vector |
| $\mathbf{i}_{dc}^{(r)}$ | Rectifier side dc-link current vector |
| $\mathbf{i}_{dc}^{(i)}$ | Inverter side dc-link current vector |
| $\mathbf{i}_C$ | Capacitor current vector |
| $\mathbf{u}_{\mathrm{p}}, \mathbf{u}_{\mathrm{n}}$ | References vector for double-carrier-based PWM |
| $\mathbf{J}$ | $90^\circ$-counter-clockwise rotation matrix |
| $\mathbf{M}$ | Modulation matrix for conventional matrix converters |
| $m_{ij}$ | Modulation functions for the matrix converter |
| $\mathbf{M}_r$ | Rectifier modulation matrix for the proposed 3L-BTB converters |
| $\mathbf{M}_i$ | Inverter modulation matrix for the proposed 3L-BTB converters |
| $m_{ij}^{(i)}$ | Modulation function for the inverter stage of the proposed 3L-BTB converters |

| | |
|---|---|
| $k_1$ | Free modulation parameter for controlling input reactive power |
| $k_2$ | Free modulation parameter for adjusting PWM switching pattern |
| $x,y,z$ | Free modulation parameter for output zero voltage generation |
| $x', y', z'$ | Free modulation parameter for output zero voltage generation for the proposed 3L-BTB converters |
| $p_i, p_o$ | Input and output active power |
| $q_i$ | Input reactive power |
| $p_C, q_C$ | Active and reactive power consumed by the capacitor network at the dc link |
| $M$ | Modulation index |
| $f_o$ | Output frequency |
| $V_i$ | Input line-to-line voltage in root-mean-square |
| $L$ | Inductance |
| $R$ | Resistance |
| $C_\Delta$ | Capacitor at the dc-link of the proposed 3L-BTB converters |
| $L_f, C_Y, R_f$ | Inductance, Capacitance and damping resistance of the filter |
| $f_n$ | Cut-off frequency of the filter |
| $\zeta$ | Damping factor of the filter |
| $\omega$ | Angular frequency |
| $v_{po}, v_{no}$ | Line voltage of the ‘max’ and ‘min’ links relative to the ‘mid’ link |

**Abbreviations**

| | |
|---|---|
| AC | Alternating Current |
| A/D, ADC | Analog-to-Digital Converter |
| BTB Converter | Back-to-Back Converter |
| EMF | Electromotive Force |
| CMC | Conventional Matrix Converter |
| D/A, DAC | Digital-to-Analog Converter |
| DC | Direct Current |
| DSP | Digital Signal Processor |
| EMI | Electromagnetic interference |
| FPGA | Field Programmable Gate Array |
| IMC | Indirect Matrix Converter |
| NPC | Neutral-Point-Clamped |

| | |
|---|---|
| PWM | Pulse Width Modulation |
| S3L-BTB Converter | Symmetrical Three-Level Back-to-Back Converter |
| USMC3 | Three-Level Unidirectional Indirect Matrix Converter |
| 2L-BTB Converter | Two-Level Back-to-Back Converter |
| 3L-BTB Converter | Three-Level Back-to-Back Converter |
| 3L-IMC | Three-Level Indirect Matrix Converter |

# CHAPTER I

# INTRODUCTION

PWM AC-AC converters nowadays have become increasingly used in many power-conversion applications, especially in industrial motor drives, utility interface for renewable energy systems, and traction drive systems. The converters in these applications should be able to operate at their highest efficiency or minimum power losses and satisfy the following requirements:

- Controllability of output voltages and frequency.
- Sinusoidal input and output currents.
- Power factor correction or operation with unity input power factor.
- Bidirectional power flow capability.
- Low electromagnetic interference.

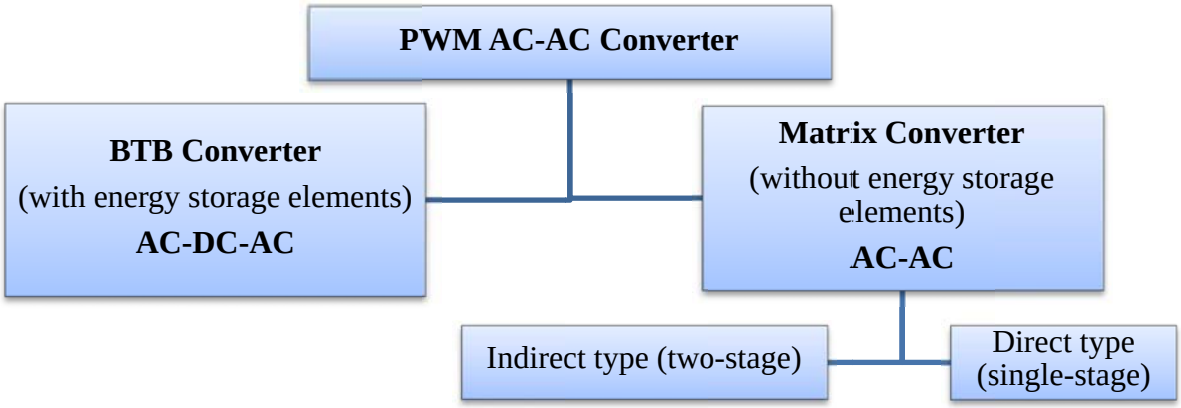



Figure 1.1 Classification of three-phase PWM AC-AC converters.

As shown in Figure 1.1, based on the presence of energy storage elements PWM AC-AC converters can be roughly classified into two categories [1], [2]: the back-to-back converters and the matrix converters. One of the topologies of the back-to-back converters widely used for medium or high power applications is the neutral-point-clamped three-level back-to-back converter (NPC 3L-BTB converter). Power modules for the NPC structure are also now supported by many power device manufacturers. Industries have gained lots of experiences on using the NPC

converters, especially in the medium and high power applications. As such, the NPC structure can be said to be mature and reliable enough to be considered as one of the basic power electronic building blocks. Although the NPC three-level back-to-back converter can fulfill the aforementioned requirements for the back-to-back converters and benefits from the properties of the three-level structure, its major problems are high switching losses and electromagnetic interference (EMI) noises. This is because one has to use the PWM technique both at the rectifier and the inverter stages. To retain the advantages of three-level structure and to alleviate the switching losses and EMI problems, new topologies for the three-level back-to-back converters need to be devised.

The matrix converters are other converter topologies that can control the output voltages and the input currents at the same time. They perform a direct conversion from AC to AC without energy storage elements. Matrix converters are divided into the direct and indirect types as shown in Figure 1.1. Though the direct matrix converter shows some promising benefits, it has not been well accepted in real applications because of the need of four-quadrant switches and also the limited range of output voltages. On the other hand, the indirect matrix converter which functions as a AC-DC-AC converter is in principle a back-to-back converter without energy storage elements. Control strategies for the indirect matrix converters have been developed by decomposing the modulation process into the rectifier and inverter stages. The rectifier generates the required virtual dc-link voltage, while the inverter utilizes that dc-link voltage to construct the output PWM voltages. Several topologies for indirect matrix converters have thereafter been proposed, whose modulation strategies are mostly based on the space vector PWM. One of the main differences between the indirect matrix converters and the back-to-back converters is how the PWM modulation is performed. The front-end rectifier and the back-end inverter of the indirect matrix converters must always cooperate to control the output voltage and the input current simultaneously, while those of the back-to-back converters usually works independently. Although this flexibility of the back-to-back converters enables the rectifier and the inverter to be switched independently without any concern on the commutation constraint, the possibility to operate the rectifier and the inverter in a cooperation manner to achieve preferable performances has been neglected in the past

researches. In addition, the viewpoint to consider the matrix converter as a 3-to-1-to-3 or AC-DC-AC converter has introduced a limit in the structure of the indirect matrix converters. It allows one to consider only the two-level rectifier as the candidate for the back-to-back structure of the indirect matrix converters. Accordingly, the indirect matrix converters proposed until now are mostly not of the three-level back-to-back structure. As a result, several fruitful results of the indirect matrix converters achieved in the literature cannot be applied directly to the three-level back-to-back converters. To overcome this obstacle, one needs to develop a new viewpoint to consider the matrix converter as a 3-to-3-to-3 AC-DC-AC converter instead.

In this work, new topologies for the three-level back-to-back converters and a new PWM strategy shall be proposed to alleviate the switching losses and EMI problems based on the switching cooperation between the rectifier and inverter stages.

To give some background on the current status of the development concerning the back-to-back converters and matrix converters, a brief review of modern AC-AC converters is presented in the following [1].

## 1.1 Conventional Three-Level Back-to-Back Converters

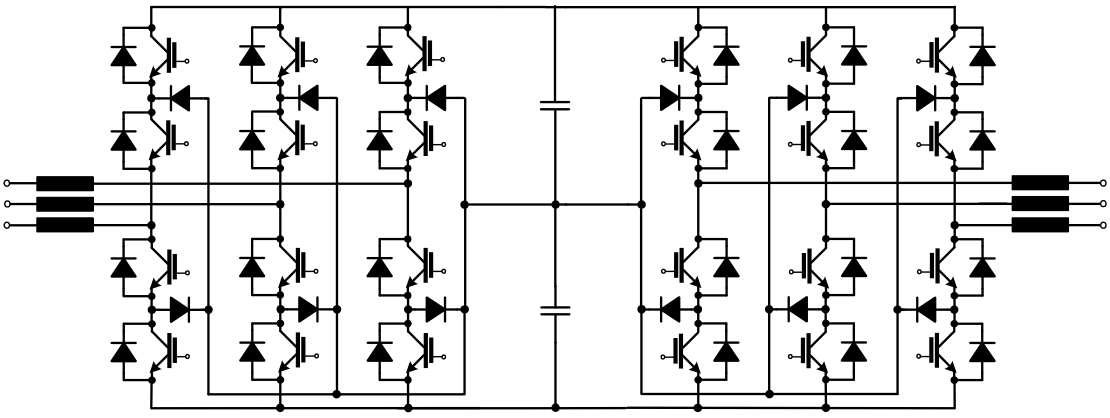


Figure 1.2 Conventional three-level back-to-back converter topology.

The popular circuit topology for the three-level back-to-back converters is based on the NPC structure as shown in Figure 1.2. This topology consists of two stages: the rectifier and inverter stages. The two stages are connected together in a back-to-back way through an intermediate dc link. Two capacitors are used as energy

storage elements in the dc link, and it is a usual perception that the dc link of this converter is a kind of symmetrical two-phase circuit. The converter converts the input AC voltages into two DC voltages at the dc link, and subsequently the DC voltages are converted into the output AC voltages. Thus, the conversion is AC-DC-AC.

Despite the plentiful merits of this topology such as low distortions in the output voltages and input currents as well as less voltage stresses across a switch, the main drawbacks are that switching losses and EMI noises are considerably increased due to the PWM technique used both at the rectifier and the inverter stages.

## 1.2 Matrix Converters

Another type of PWM AC-AC converters is the matrix converter. The matrix converter generates the output voltages directly from the input voltages using PWM method. In contrast to the conventional back-to-back converter, the conversion of the matrix converter is a direct AC-AC one without any energy storage elements. The matrix converters can be categorized further as a conventional type or direct type and an indirect type as shown in Figure 1.1.

Since the indirect-type matrix converter is of a back-to-back topology, it may be adopted as a good starting framework to develop novel topologies for three-level back-to-back converters with reduced switching losses and EMI noises. Therefore, some indirect-type topologies of the matrix converters will be reviewed in this Section [3].

### 1.2.1 Indirect Matrix Converters (IMC)

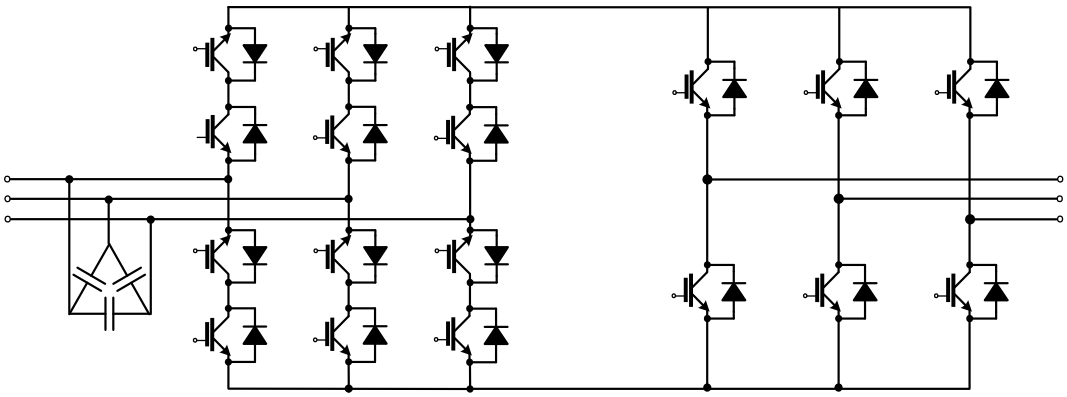


Figure 1.3 The indirect matrix converter topology

The indirect matrix converter has the topology of a two-level back-to-back structure without any energy storage elements as depicted in Figure 1.3. The inverter stage is a two-level voltage-source inverter, whereas the rectifier stage is a two-level current-source inverter. This topology originated from physical realization of the conventional indirect modulation method which views the ‘fictitious dc link’ as a two-level link [1], [4] , [5]. Due to this structural difference, any characteristics or research results belonging to the conventional IMC cannot be directly applied to the three-level back-to-back converters.

### 1.2.2 The Indirect Matrix Converter with Three-Level Output Stage

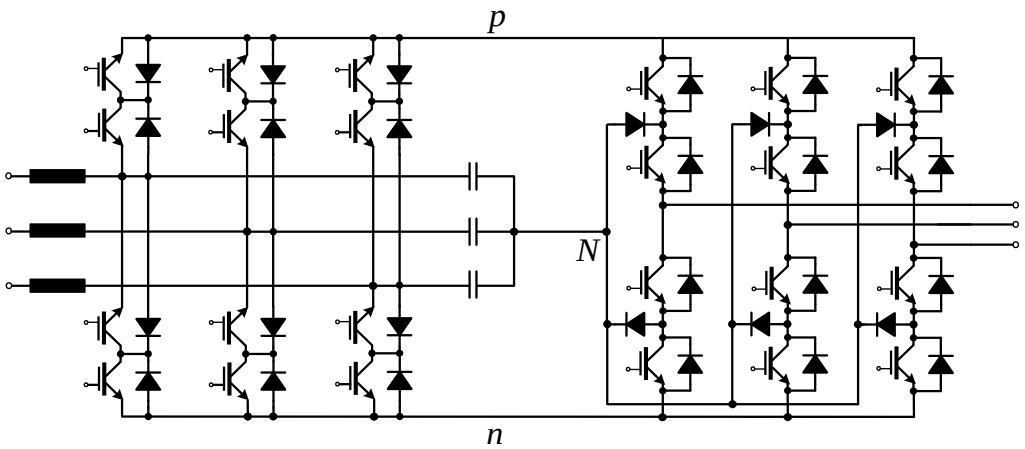



Figure 1.4 The indirect matrix converter with three-level output stage topology.

The indirect matrix converter with three-level output stage topology in Figure 1.4 replaces the two-level inverter stage in the IMC with a three-level NPC inverter. This indirect matrix converter and its modulation method were proposed in [6] and [7], respectively. However, the rectifier remains a two-level one with the neutral point established using a capacitor network. The two-level rectifier still impedes further development for the three-level back-to-back converter topology.

### 1.2.3 Three-Level Unidirectional Indirect Matrix Converters (USMC3)

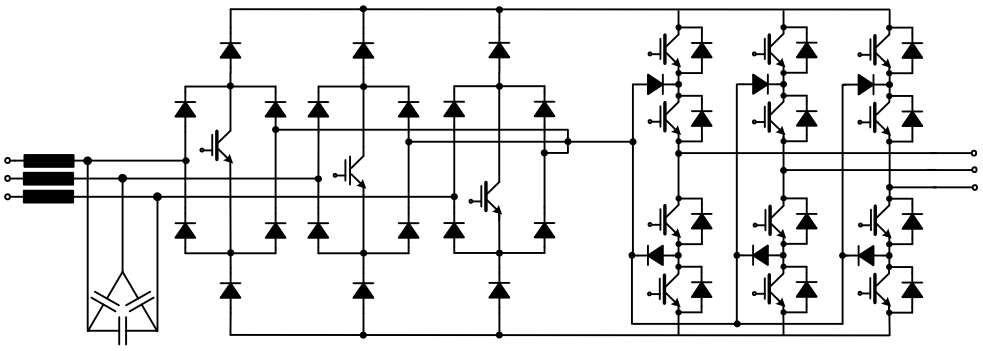


Figure 1.5 The three-level unidirectional indirect matrix converter (USMC3) topology

In [1], a brief discussion of a three-level unidirectional indirect matrix converter topology in Figure 1.5 was given. This topology has the actual three-level structure both at the rectifier and inverter stages: the Vienna rectifier as the front-end rectifier and the three-level NPC structure as the inverter. Moreover, the Vienna rectifier in this topology switches at the fundamental or power-line frequency leading to reduction of switching losses and EMI noises. However, its modulation method to achieve both the output voltage and input current controls has not been clarified. Another drawback of this topology is the operation limits on both the input and output power factors.

From the past literature review regarding researches on the indirect-type matrix converters, none of them has the structure of a three-level back-to-back topology, except for the USMC3 topology. But the USMC3 topology is not

acceptable due to its limits on input and output power factor and its unclear control strategy.

## 1.3 Objective of Research

The main purpose of this work is to develop novel topologies for three-level back-to-back converters together with their modulation strategies based on the matrix converter theory, aiming to reduce switching losses and EMI noises at the rectifier stage and to fulfill the fundamental requirements of AC-AC converters.

## 1.4 Scope of Research

The scope of this research is to develop novel topologies for three-level back-to-back converters together with their modulation strategies. An operational prototype will be built and the performances of the proposed back-to-back converters will be verified by simulation and experiment.

## 1.5 Research Methodology

1. Study the background knowledge of the conventional three-level back-to-back converters and their problems.
2. Review the past literature relevant to matrix converters which have the back-to-back topology.
3. Study the unified PWM method for conventional matrix converters and its carrier-based realization.
4. Propose the new topologies for three-level back-to-back converters aiming to reduce switching losses and EMI.
5. Validate the proposed concepts with simulations.
6. Design and build an operational prototype of the proposed three-level back-to-back converter.
7. Verify and evaluate performances of the prototyped converter.
8. Analyze the experimental results.
9. Draw a conclusion, and write the thesis.

## 1.6 Expected Contribution

1. Novel topologies for three-level back-to-back converters with reduced switching losses and EMI noises at the rectifier stage.
2. Novel PWM strategy which efficiently coordinates the modulation of the rectifier and the inverter of the back-to-back converters.
3. Derivation of new topologies for the indirect matrix converters which are truly equivalent to the conventional matrix converters.

## 1.7 Organization of the Thesis

In Chapter II, fundamental PWM theory of the conventional matrix converters will be reviewed to provide a basic framework to develop the new three-level back-to-back converters. The PWM theory explained in Chapter II differs very much from the conventional PWM theory which is normally adopted as the basics for development of the indirect-type topologies of the matrix converter todays. The PWM theory in Chapter II is based on double-carrier-based dipolar PWM which fits well with the three-level back-to-back topology, making it the perfect tool necessary for the development of new topologies for the three-level back-to-back converters. The double-carrier-based dipolar PWM will be revised and a three-level indirect modulation strategy will be introduced.

Subsequently in Chapter III, the three-level indirect modulation will be applied to establish two novel topologies for three-level back-to-back converters. The first topology is called the three-level indirect matrix converter (3L-IMC), and the second one is the symmetrical three-level back-to-back converter (S3L-BTB converter). Their PWM modulation technique which is based on the cooperation between the switching of the rectifier and that of the inverter will also be derived in Chapter III.

Chapter IV presents and discusses the simulation results to verify the performances of the proposed topologies. Moreover, the semiconductor losses of the proposed S3L-BTB converter are numerically evaluated and compared to those of the conventional back-to-back converters to point out a remarking reduction of switching losses at the rectifier stage.

In Chapter V, a laboratory prototype development of the S3L-BTB converter will be discussed. The functional diagram of the prototype which is implemented on a single FPGA as a purely digital controller and the overall experimental setup will be explained. Experimental results will then be shown and analyzed. The power losses of the rectifier and the inverter stage will also be measured and discussed.

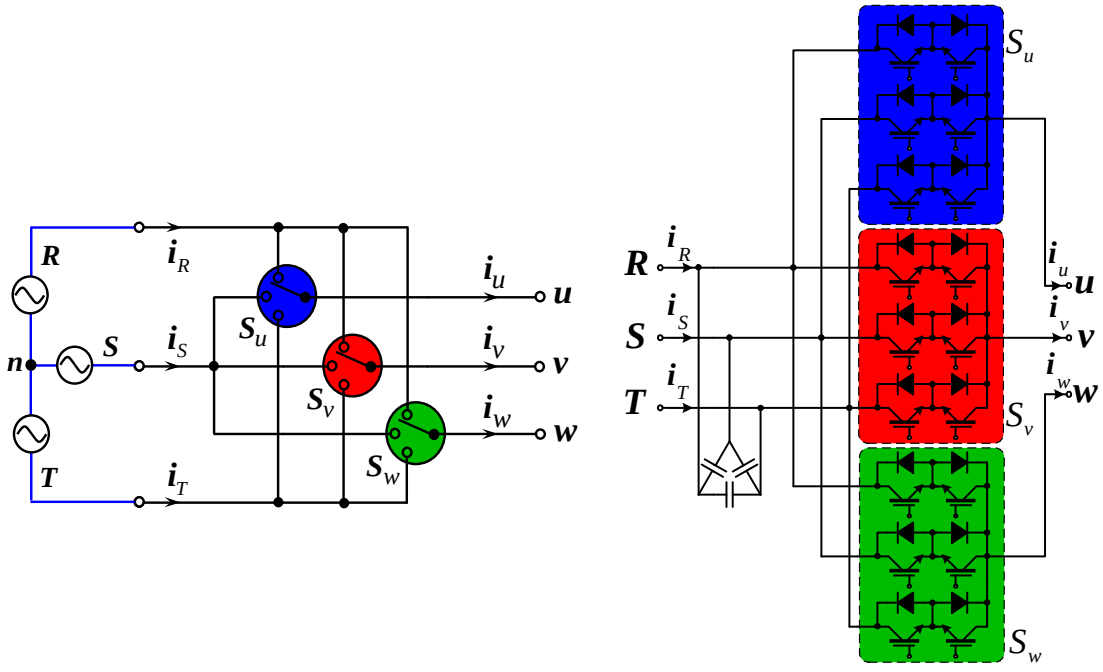
Conclusion and suggestions for future work are summarized in Chapter VI. Finally, a method used for calculating the semiconductor losses in Chapter IV are given in the Appendix.

# CHAPTER II

# MATRIX CONVERTER THEORY

As the basic concept of novel topologies for three-level back-to-back converters to be introduced in Chapter III is based on the matrix converter theory, some fundamental subjects and the generalized modulation strategy for the conventional matrix converter derived in [8] will be reviewed in this chapter.

## 2.1 Conventional Matrix Converters (CMC)




(a) (b)

Figure 2.1 Matrix converters. (a) conceptual model (b) conventional matrix converter

The conventional matrix converter is a converter topology that can directly generate three-phase output voltages from three-phase input voltages in a single stage. Its conceptual operation can be modeled as shown in Figure 2.1(a) with three triple-pole triple-throw ideal switches. Each output phase can be independently connected

to any selected input phase. Each of the ideal three-pole switches can be realized by using six IGBTs forming as three four-quadrant switches as depicted in Figure 2.1(b).

## 2.2 **Mathematical Model of Matrix Converters**

Considering the conceptual model of matrix converters in Figure 2.1(a), the averaged input-output voltage and current equations can be expressed by (2.1) and (2.2), respectively.

$$\overbrace{\begin{bmatrix} u \\ v \\ w \end{bmatrix}}^{\mathbf{v}_o} = \begin{bmatrix} u^* + v_z \\ v^* + v_z \\ w^* + v_z \end{bmatrix} = \overbrace{\begin{bmatrix} m_{11} & m_{12} & m_{13} \\ m_{21} & m_{22} & m_{23} \\ m_{31} & m_{32} & m_{33} \end{bmatrix}}^{\mathbf{M}} \overbrace{\begin{bmatrix} R \\ S \\ T \end{bmatrix}}^{\mathbf{v}_i} \Leftrightarrow \mathbf{v}_o = \mathbf{M}\mathbf{v}_i \tag{2.1}$$

$$\overbrace{\begin{bmatrix} i_R \\ i_S \\ i_T \end{bmatrix}}^{\mathbf{i}_i} = \overbrace{\begin{bmatrix} m_{11} & m_{12} & m_{13} \\ m_{21} & m_{22} & m_{23} \\ m_{31} & m_{32} & m_{33} \end{bmatrix}^T}^{\mathbf{M}^T} \overbrace{\begin{bmatrix} i_u \\ i_v \\ i_w \end{bmatrix}}^{\mathbf{i}_o} \Leftrightarrow \mathbf{i}_i = \mathbf{M}^T \mathbf{i}_o \tag{2.2}$$

where $\mathbf{v}_i = \begin{bmatrix} R & S & T \end{bmatrix}^T$ is the instantaneous input voltage vector,

$\mathbf{i}_i = \begin{bmatrix} i_R & i_S & i_T \end{bmatrix}^T$ is the instantaneous input current vector,

$\mathbf{v}_o = \begin{bmatrix} u & v & w \end{bmatrix}^T$ is the instantaneous output voltage vector,

$\mathbf{i}_o = \begin{bmatrix} i_u & i_v & i_w \end{bmatrix}^T$ is the instantaneous output current vector,

$*$ denotes the commanded value,

$v_z$ is the injected zero voltage.

Here $\mathbf{M}$ is the modulation matrix, and its element $m_{ij}$ represents the duty cycle which each output phase $\{u,v,w\}$ is connected to each input phase $\{R,S,T\}$ during a switching period. The duty cycles must satisfy the following constraints:

$0 \le m_{ij} \le 1$ and $\sum_{j=1}^{3} m_{ij} = 1,\ i \in \{1,2,3\},\ j \in \{1,2,3\}$.

According to the analysis results in [8], the general form of the modulation matrix $\mathbf{M}$ is given by (2.3),

$$\mathbf{M} = \mathbf{M}_{\mathrm{U}} + \mathbf{M}_{\mathrm{I}} + \mathbf{M}_{\mathrm{N}} + \mathbf{M}_{0} \tag{2.3}$$

where

$$\mathbf{M}_{\mathrm{U}} = \frac{1}{\|\mathbf{v}_i\|^2}\mathbf{v}_o^*[\mathbf{v}_i]^T = \frac{1}{R^2+S^2+T^2}\begin{bmatrix} u^* \\ v^* \\ w^* \end{bmatrix}[R \quad S \quad T] \tag{2.4}$$

$$\mathbf{M}_{\mathrm{I}} = \frac{k_1}{\|\mathbf{v}_i\|^2}\mathbf{i}_o[\mathbf{J}\mathbf{v}_i]^T = \frac{k_1}{\sqrt{3}(R^2+S^2+T^2)}\begin{bmatrix} i_u \\ i_v \\ i_w \end{bmatrix}[S-T \quad T-R \quad R-S] \tag{2.5}$$

$$\mathbf{M}_{\mathrm{N}} = \frac{k_2}{\|\mathbf{v}_i\|^2}\mathbf{J}\mathbf{i}_o[\mathbf{J}\mathbf{v}_i]^T = \frac{k_2}{3(R^2+S^2+T^2)}\begin{bmatrix} i_v-i_w \\ i_w-i_u \\ i_u-i_v \end{bmatrix}[S-T \quad T-R \quad R-S] \tag{2.6}$$

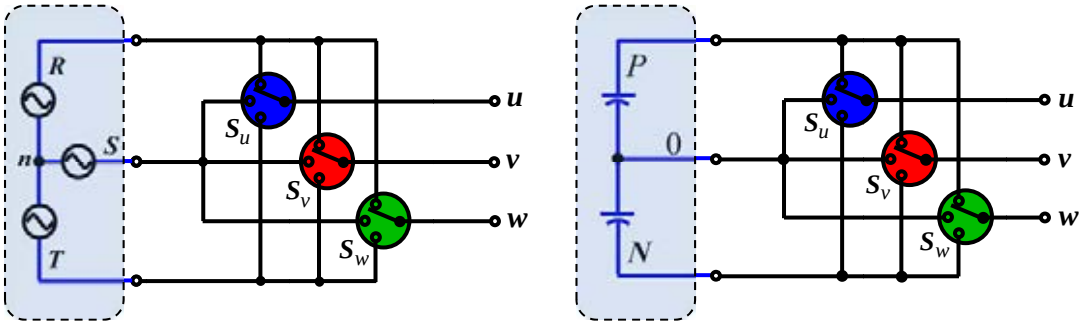
$$\mathbf{M}_0 = \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}[x \quad y \quad z] \qquad ; \qquad 0 \le x, y, z \le 1 \quad x+y+z=1 \tag{2.7}$$

Here, $\mathbf{J} = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}$ is the $90^\circ$-counter-clockwise rotation matrix, and $\|\cdot\|$ denotes the magnitude of a vector. $k_1$ in (2.5) is the modulation free parameter for controlling the reactive current through the modulation matrix $\mathbf{M}_{\mathrm{I}}$, while $k_2$ in (2.6) is the free parameter for adjusting the switching pattern through the modulation matrix $\mathbf{M}_{\mathrm{N}}$, without affecting the output voltages and the input currents.

The modulation matrix $\mathbf{M}_{\mathrm{U}}$ produces the required output voltage $\mathbf{v}_o^*$ and the active component of the input current $\mathbf{i}_i$. In other words, a unity power factor is obtained when $\mathbf{M} = \mathbf{M}_{\mathrm{U}} + \mathbf{M}_0$ $(k_1 = k_2 = 0)$ is selected, where $\mathbf{M}_0$ is the zero-voltage matrix which determines the injected zero voltage through the parameters *x*, *y* and *z*.

## 2.3 **Double-Carrier-Based Dipolar PWM for Matrix Converters**

To generate the PWM switching signals corresponding to the modulation matrix **M** in (2.3) - (2.7), the double-carrier-based dipolar PWM technique will be applied.




(a) CMC (b) Three-level inverters

Figure 2.2 Similarity between the CMC and the three-level inverter.

The double-carrier-based dipolar PWM technique in [9] has been originally introduced for the three-level inverter. However, the similarity between the CMC and the three-level inverter seen in Figure 2.2 suggests that it may be possible to modify the technique for the CMC. The CMC differs from the three-level inverter in that the polarities of the three input voltages of the CMC are not unidirectional like those of the three-level inverter. Therefore, to make this technique applicable to the CMC, the unidirectional polarities of the input voltages must be ensured. This can be done by viewing the modulation process as an indirect modulation, with which the overall modulation process will be decomposed into two stages, i.e. the rectifier and the inverter stages, as explained in the following.

### 2.3.1 Rectifier Stage

First, the input voltages $\{R,S,T\}$ are virtually rectified or sorted into a descending order as:

$$v_{max} = \max(R,S,T) \tag{2.8}$$

$$v_{mid} = \text{med}(R,S,T) \tag{2.9}$$

$$v_{min} = \min(R,S,T). \tag{2.10}$$

For the case that the input voltages are balanced three-phase sinusoidal waveforms, the resultant rectified voltages will be as depicted in Figure 2.3. This operation is exactly the same as that obtained from a three-level rectifier. The three pole voltages $v_{max}, v_{mid}, v_{min}$ will be used as new input voltages for the inverter

operation in the next step. As a result, the polarities of the input voltages are now guaranteed to be unidirectional as required because $v_{max} \geq v_{mid} \geq v_{min}$ always holds.

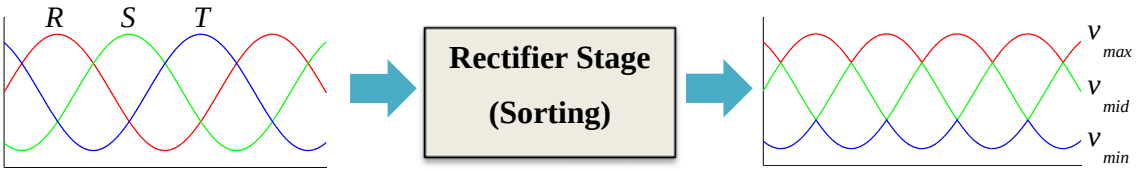



Figure 2.3 Sorting operation of the rectifier stage

### 2.3.2 Inverter Stage

To explain how the inverter stage works, taking the mid-point pole as the reference the dc link is now considered to be composed of two dc-link voltages: the upper dc-link voltage ($v_{max} - v_{mid}$) and the lower one ($v_{mid} - v_{min}$). The output voltages will be generated from these two dc-link voltages using the PWM modulation technique. For this purpose, the output voltages equation (2.1) is rewritten by changing the reference point to the mid-phase voltage $v_{mid}$ as expressed in (2.11). As can be seen from (2.11), the output voltages are given as a sum of two output voltages $\mathbf{u}_p$ and $\mathbf{u}_n$ generated from each of the upper and lower dc-link voltages, respectively.

$$\begin{bmatrix} u - v_{mid} \\ v - v_{mid} \\ w - v_{mid} \end{bmatrix} = \underbrace{\begin{bmatrix} m_{1p} \\ m_{2p} \\ m_{3p} \end{bmatrix} (v_{max} - v_{mid})}_{\mathbf{u}_p} + \underbrace{\begin{bmatrix} -m_{1n} \\ -m_{2n} \\ -m_{3n} \end{bmatrix} (v_{mid} - v_{min})}_{\mathbf{u}_n} \tag{2.11}$$

Here, the subscripts ‘p’ and ‘n’ denote the column indices of the modulation matrix corresponding to the maximum and the minimum phase voltages, respectively.

Eq. (2.11) indicates that one can use the two voltages $\mathbf{u}_p$ and $\mathbf{u}_n$ as references for the double-carrier-based dipolar PWM which is originally developed for three-level inverters [8]. Figure 2.4 illustrates how to use double carriers and the two reference voltages to generate the required PWM signals. In the left-most part of Figure 2.4(a), the three dc voltages $v_{max}, v_{mid}, v_{min}$ are chosen as the three levels of the two carrier waveforms. The amplitudes of the two carriers are thus the two dc-link

voltages ($v_{max} - v_{mid}$) and ($v_{mid} - v_{min}$). This kind of representation makes it easier to understand how the double-carrier based PWM works. However, for hardware or software implementation, it often requires that the amplitudes of the carriers be unity. This can be easily done by normalizing the upper and lower parts of the figure separately with the corresponding dc-link voltages. From (2.11), the normalized double-carrier based PWM is obtained as shown on the right, wherein it is clear that the two references after normalization become just the duty cycles or the elements of the modulation matrix. Figure 2.4(b) gives an example of the output PWM voltage when the triangular signals are used as the two carrier waveforms. Figure 2.5 shows the conceptual diagram of the inverter stage with the sorted unidirectional dc-link voltages and the resultant output PWM voltages. It is seen that the envelopes of the PWM waveforms follow the three-level dc-link voltages of Figure 2.3 as expected.

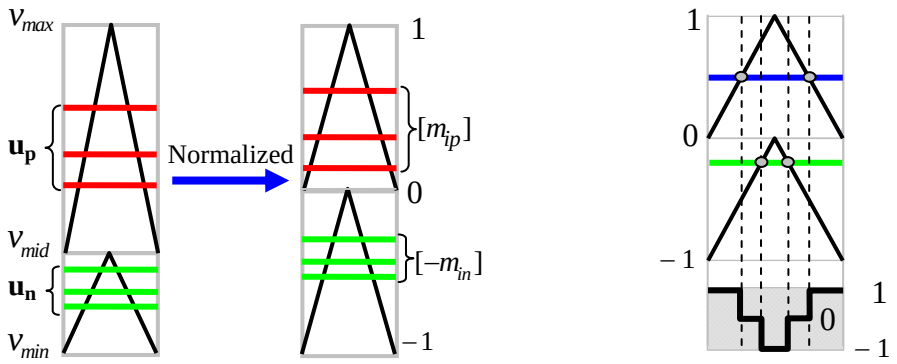



Figure 2.4 Double-carrier-based PWM for matrix converters. (a) two reference voltages and their normalization (b) switching signal for one phase.

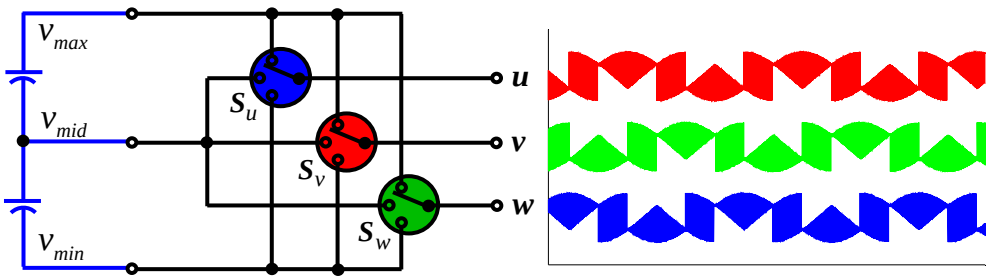



Figure 2.5 Conceptual diagram of the inverter stage with the unidirectional dc-link voltages and its generated output PWM voltages

## 2.4 Three-Level Indirect Modulation

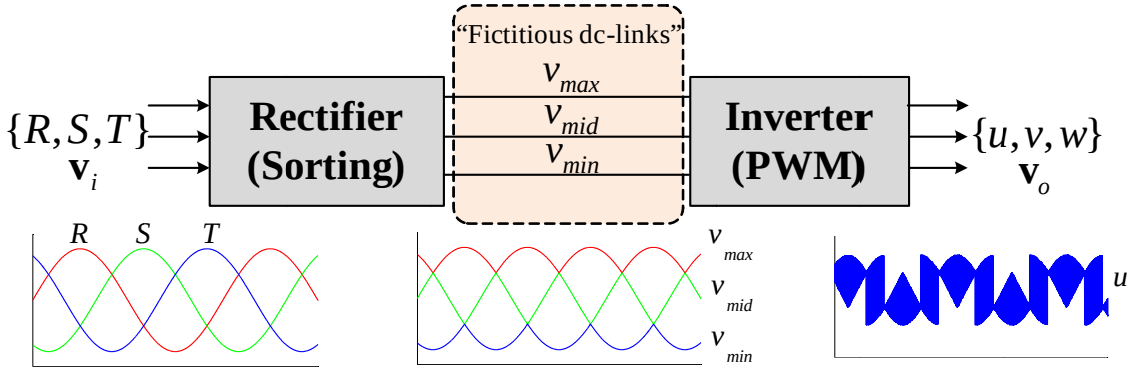



Figure 2.6 Three-level indirect modulation strategy derived from double-carrier-based PWM.

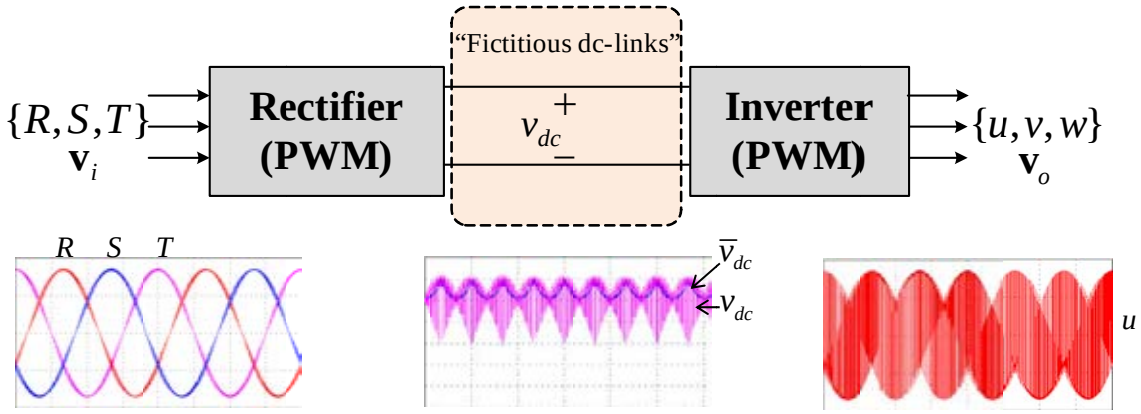



Figure 2.7 Conventional indirect modulation strategy [10].

When combining the two stages together and considering the three-level fictitious dc-links introduced virtually, the whole process can be drawn as a diagram in Figure 2.6 and is called here as 'Three-level indirect modulation'. For comparison, the conventional indirect modulation in [10] is shown in Figure 2.7. Although both indirect modulation strategies share the two-stage modulation structure in common, there is a significant difference between them regarding the fictitious dc link of the rectifier stage. The rectifier stage of the three-level indirect modulation constructs the fictitious dc link as a three-level dc link, and the rectifier switches at the power line frequency to sort the input voltages into a descending order. On the contrary, the

rectifier in the conventional indirect modulation views the fictitious dc link as a two-level dc link, and it switches at a very high frequency by the PWM method. Accordingly, the output PWM voltages generated by each modulation strategy are significantly different. Owing to the existence of the three-level dc link, the three-level indirect modulation can employ any of the three input voltages to construct the output voltage at any instant within a switching period, which is equivalent to the direct modulation. On the other hands, the conventional indirect modulation is limited to employ only two of the three input voltages at any instant in a switching period. To overcome this limitation, the rectifier stage has to generate two different dc-link voltages during one PWM period so that one can regain the utilization of all the three input voltages. However, there is still one problem left by this approach. The three input voltages cannot be used simultaneously at any instant within the switching period to generate the output voltages, making the conventional indirect modulation only a subset of the direct modulation.

In summary, it can be concluded that the three-level indirect modulation introduced in the thesis is truly equivalent to the direct modulation of the CMC. In other words, the indirect modulation for the CMC should be a three-level indirect modulation whose rectifier and inverter stages function as a 3-to-3-to-3-phase conversion rather than a 3-to-1-to-3-phase conversion of the conventional indirect modulation. All of these conclusions are quite natural because the CMC's topology is inherently a kind of three-level converter as depicted in Figure 2.1.

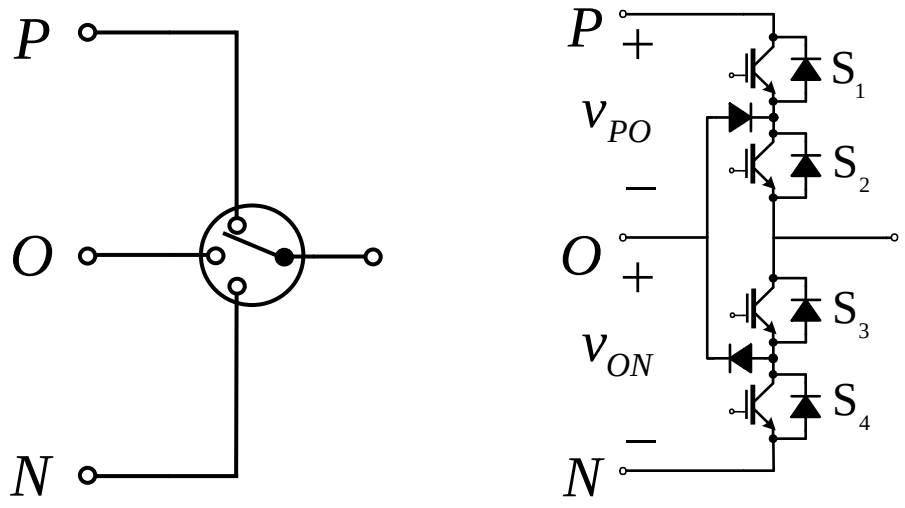
Furthermore, with the aforementioned insight, it becomes soon clear that a serious consequence if one adopts the conventional indirect modulation is that it does not allow one to apply such an indirect modulation technique of the CMC to a three-level back-to-back converter which functions as a 3-to-3-to-3-phase conversion. However, this is possible and straightforward with the proposed three-level indirect modulation, and this will be the main topic of the following chapter.

# CHAPTER III
# NOVEL TOPOLOGIES FOR THREE-LEVEL BACK-TO-BACK CONVERTERS

The conventional three-level back-to-back converters allow one to simultaneously generate any commanded output voltages and control the input currents for power factor correction requirement. The output voltage generation task is the responsibility of the back-end inverter, while the input current control is taken care of by the frond-end rectifier of the conventional converter. Normally, the rectifier and inverter operate independently in the PWM mode using the dc link as an intermediate buffer. However, as pointed out in Chapter I, the conventional three-level back-to-back converter has some disadvantages regarding switching losses and EMI. This is mainly due to the PWM operation of the frond-end rectifier which is introduced to replace the conventional diode rectifier for power factor correction. To solve these problems, two novel topologies for three-level back-to-back converts will be proposed in this Chapter.

The main idea newly proposed in this thesis is that the switching behaviors of the rectifier and the inverter should be cooperated or combined to reduce switching losses and EMI [11] [12]. This could be achieved without loss of the input current and output voltage controllability by using the three-level indirect modulation explained in the previous Chapter. The structure of the three-level converters used in this thesis is the well-known neutral-point-clamped (NPC) structure. All the theoretical results derived in this thesis are however not only limited to the NPC structure, but also are valid for all structures of three-level converters.

## 3.1 **Three-Level Neutral-Point-Clamped (NPC) Structure**




(a) (b)

Figure 3.1 Single-phase NPC three-level converter topology.
(a) conceptual model (b) real circuit

The conceptual model for a single-phase three-level converter topology is shown in Figure 3.1(a). It consists of three inputs and one output terminal; the output terminal can be connected to any of the input terminals. Although there are a lot of structures applicable to construct this topology, the widely used one is the three-level NPC structure depicted in Figure 3.1(b). This structure was firstly introduced by Nabae et al [13]. It contains four IGBTs, four anti-parallel diodes, and two clamping diodes. In this case, the three input voltages must be unidirectional, i.e. $v_P \geq v_O \geq v_N$ or $v_{PO}, v_{ON} \geq 0$. One advantage of this structure is that the voltage stress across each switch and diode is only half of the dc-link voltage. As a result, the NPC structure is suitable for medium and high voltage applications.

The instantaneous value of the output voltage at the output terminal can be any levels of the three input voltages depending on the status of the switches S1-S4 as shown in Table 3.1. A three-phase three-level NPC converter can be easily constructed by paralleling three legs of the NPC structure as shown in Figure 3.2.

Table 3.1 Relation between the output voltage and the status of each switch.

| **Connected bus** | **Output voltage relative to mid-point *O*** | **$S_1$** | **$S_2$** | **$S_3$** | **$S_4$** |
|---|---|---|---|---|---|
| *P* | $v_{PO}$ | On | On | Off | Off |
| *O* | 0 | Off | On | On | Off |
| *N* | $-v_{ON}$ | Off | Off | On | On |

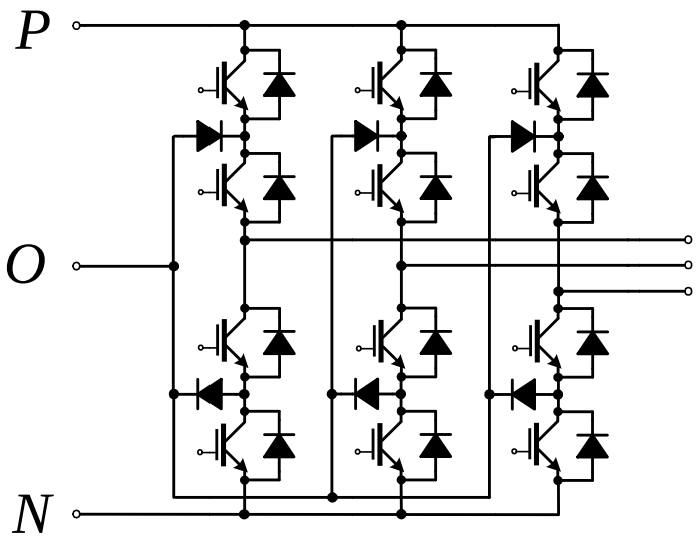



Figure 3.2 Three-phase three-level NPC structure.

## 3.2 **Novel Topologies for Three-Level Back-to-Back Converters**

Based on the three-level indirect modulation technique of Figure 2.6, novel topologies for three-level back-to-back converters can be developed by realizing the virtual or mathematical rectifier and inverter stages with physical circuits.

### 3.2.1 **Three-Level Indirect Matrix Converters**

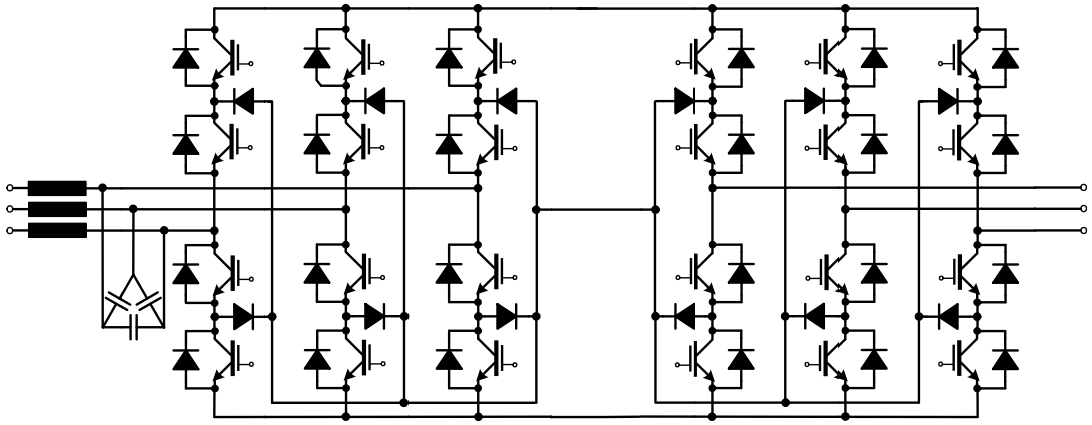


Figure 3.3 Three-level indirect matrix converter (3L-IMC).

The first back-to-back topology to be proposed is constructed by directly realizing the virtual rectifier and inverter stages of the three-level indirect modulation of Figure 2.6 with a three-level rectifier and a three-level inverter, respectively. This topology is called hereafter as a "Three-Level Indirect Matrix Converter" or 3L-IMC. Because the polarities of three dc-link voltages are unidirectional, the three-phase three-level NPC structure can be adopted for both the rectifier and the inverter as shown in Figure 3.3. In this Figure, a network of inductors and capacitors is added at the input of the converter to function as a low-pass filter to filter out switching ripples contained in the PWM input current. This kind of topology has never been discussed in the past literature [3], though it is one of a straightforward and simple one. This may be due to a lack of appropriate modulation technique to control both the rectifier and inverter simultaneously. The main difference from the conventional three-level back-to-back converter of Figure 1.2 is that there is no capacitive energy storage at the dc link of the 3L-IMC, which is an inherent character of the matrix converter in general.

It should be emphasized that since the three-level indirect modulation functions as a 3-to-3-to-3-phase conversion, the dc link of the 3L-IMC operating based on this principle must be viewed as a three-phase circuit. This is an important difference compared with the conventional three-level back-to-back converter of

Figure 1.2 which is usually treated as a 3-to-2-to-3 conversion. The dc link of the conventional back-to-back converter is thus normally considered as a two-phase circuit. This significant change of viewpoint will be utilized to further the development of the back-to-back converter in Section 3.2.2.

As explained in Section 2.3, from the fact that the back-end inverter of the 3L-IMC topology can use all three input voltages simultaneously to generate the PWM output voltages within a switching period, the 3L-IMC is perfectly equivalent to the CMC. Therefore, the 3L-IMC possesses all the input-output characteristics of the conventional (direct) matrix converter.

The main features of this 3L-IMC topology can be summarized as follows:

1) The rectifier operates at the fundamental (power-line) frequency in order to produce the max-mid-min links illustrated in Figure 2.3.
2) The dc link is thus not a constant voltage source as in the conventional three-level inverter.
3) The inverter operates in the PWM mode by applying the double-carrier dipolar modulation technique with the max-mid-min dc links
4) The inverter controls both the output voltages and input currents simultaneously with the help of the rectifier.

The aforementioned features contribute to the following merits of the 3L-IMC:

1) The output voltages are generated as commanded with sinusoidal input currents similar to those achieved by the matrix converter.
2) Switching losses at the rectifier stage are lower compared to those of the conventional 3L-BTB converter which operates in the PWM mode.
3) The voltage waveforms at the input of the rectifier are sinusoidal with only small switching ripples. Therefore, compared to the conventional PWM rectifier in Figure 1.2, the 3L-IMC has less EMI problems, and smaller EMI filters at the input can be used.

Nevertheless, the output voltage range of the 3L-IMC is limited to 87% of the input voltage, which is the inherent characteristic of the matrix converter. In addition, commutation timing must be carefully considered so as not to cause open-circuit conditions at the load or short-circuit conditions at the source.

### 3.2.2 **Symmetrical Three-Level Back-to-Back Converters**

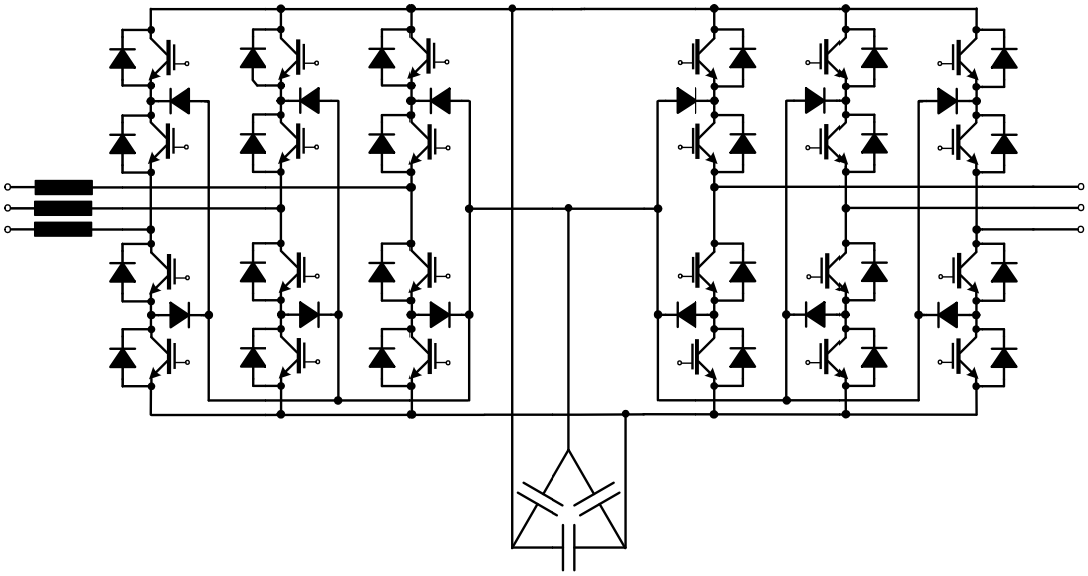


Figure 3.4 Symmetrical three-level back-to-back converter (S3L-BTB converter).

The commutation constraint and the limitation of the output voltage range of the 3L-IMC pointed out previously can be overcome with a new back-to-back converter topology derived in the following.

With a careful investigation of Figure 3.3, it is realized that the input-filter capacitors can still function properly even though they are moved inside to be connected at the dc link. This modification results in a symmetrical three-phase circuit at the dc link as illustrated in Figure 3.4. This new circuit topology is thus called a "Symmetrical Three-Level Back-to-Back Converter" or S3L-BTB converter.

It should be noticed that the proposed S3L-BTB converter looks almost the same as the conventional 3L-BTB converter shown in Figure 1.2. However, as mentioned earlier, the dc link of the S3L-BTB converter together with the capacitors forms a symmetrical three-phase circuit, while that of the conventional 3L-BTB converter does not. Due to the close similarity between the S3L-BTB converter topology and the conventional 3L-BTB topology shown in Figure 1.2., the S3L-BTB

converter can operate as the latter, but the reverse is not possible. It should be underlined that the conventional 3L-BTB converter in Figure 1.2 can be simply modified to be the S3L-BTB converter by adding just one capacitor between the positive and negative buses. Nevertheless, the capacitors can also be connected as wye in the S3L-BTB converter. The S3L-BTB converter enjoys the same low losses and low EMI properties of the 3L-IMC with the following additional merits.

1) The front-end rectifier and the back-end inverter are able to switch independently without any constraint on the commutation timing. This is owing to the existence of the capacitors at the dc link. The rectifier and the inverter still however cooperate to control both the output voltages and the input currents as is done in the 3L-IMC. This kind of cooperation is not possible with the conventional 3L-BTB converter because of the unsymmetrical three-phase circuit at the dc link.
2) The input currents flowing through the front-end rectifier becomes piecewise sinusoidal waveforms without any impulsive spikes from the PWM operation of the back-end inverter. The PWM current ripples will be by-passed by the capacitors at the dc link. This property is very important for simplification of the circuit topology in the case of unidirectional power flow [14].
3) The output voltage range can be extended beyond 87% of the input voltage if necessary by changing the operation of the rectifier from the fundamental frequency switching to the PWM mode, with which the dc-link voltages can be boosted up. This is possible because as pointed earlier the S3L-BTB converter can work as the conventional 3L-BTB converter. The switching losses and EMI merits are lost by this changing of operation, however.
4) The capacitors at the dc link can be designed to help buffer the energy during voltage dips. For this purpose, large capacitors will be required to store the energy and may lead to unwanted leading power factor at the input. If only the filtering function is expected, the dc-link capacitors shall be small. This merit is however not available in the CMC.

## 3.3 Modulation Strategy for the Proposed 3L-BTB Converters

### 3.3.1 The modulation functions for the rectifier and the inverter of the proposed 3L-BTB Converters

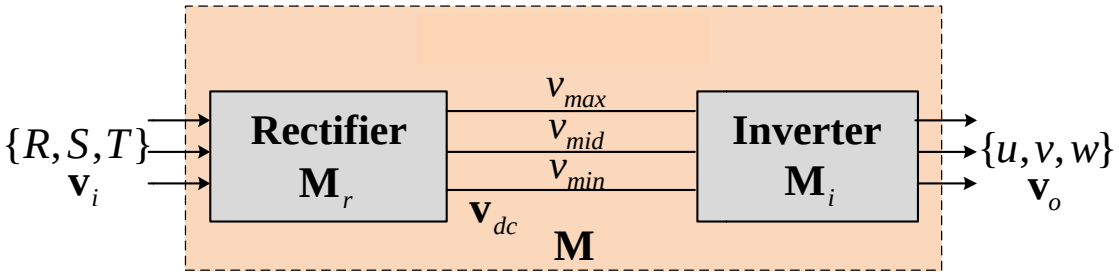



Figure 3.5 Three-level indirect modulation functions for the proposed 3L-IMC and S3L-BTB converters

Since the proposed topologies for three-level back-to-back converters are based on the concept of the three-level indirect modulation which is the modulation strategy of the matrix converter, the modulation functions or matrices of the rectifier and the inverter of the 3L-IMC and S3L-BTB converters shall be derived from the mathematical analysis results of the matrix converter explained in Chapter II.

According to Figure 3.5, the modulation matrix $\mathbf{M}$ of the proposed converters is composed of two modulation matrices: the rectifier modulation matrix $\mathbf{M}_r$ and the inverter modulation matrix $\mathbf{M}_i$. These two modulation matrices will be derived in the following.

The voltage equations for each part of Figure 3.5 can be written as (3.1) - (3.3).

Rectifier Stage: $$\mathbf{v}_{dc} = \mathbf{M}_r \mathbf{v}_i \quad (3.1)$$

Inverter Stage: $$\mathbf{v}_o = \mathbf{M}_i \mathbf{v}_{dc} \quad (3.2)$$

Thus, $$\mathbf{v}_o = \mathbf{M}_i \mathbf{M}_r \mathbf{v}_i \quad (3.3)$$

and $$\mathbf{M} = \mathbf{M}_i \mathbf{M}_r \quad (3.4)$$

Because the proposed converters, 3L-IMC and S3L-BTB converter, are truly equivalent to the CMC, the modulation matrix $\mathbf{M}$ must be the same. Therefore, the

modulation matrix $\mathbf{M}$ in (3.4) must be as expressed in (2.3)-(2.7). The generalized modulation matrix is repeated here for clarity.

$$\mathbf{M} = \mathbf{M}_i\mathbf{M}_r = \mathbf{M}_{\mathrm{U}} + \mathbf{M}_{\mathrm{I}} + \mathbf{M}_{\mathrm{N}} + \mathbf{M}_0 \tag{3.5}$$

First, considering that the function of the rectifier is to sort the three input voltages into the three dc-link voltages $\mathbf{v}_{dc} = \begin{bmatrix} v_{max} & v_{mid} & v_{min} \end{bmatrix}^T$ in a descending order, the rectifier modulation matrix $\mathbf{M}_r$ can be determined for each sector of the input voltages as shown in Table 3.2.

Table 3.2 Rectifier modulation matrix for each sector of the input voltages

| **No. of Sector** $n$ | **dc-link voltages** | | | **Rectifier Modulation Matrix** $\mathbf{M}_r$ | **Geometric Transformation category** |
|---|---|---|---|---|---|
| | $v_{max}$ | $v_{mid}$ | $v_{min}$ | | |
| 1 | $R$ | $S$ | $T$ | $\begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$ | Rotation |
| 2 | $S$ | $R$ | $T$ | $\begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix}$ | Reflection |
| 3 | $S$ | $T$ | $R$ | $\begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 0 \end{bmatrix}$ | Rotation |
| 4 | $T$ | $S$ | $R$ | $\begin{bmatrix} 0 & 0 & 1 \\ 0 & 1 & 0 \\ 1 & 0 & 0 \end{bmatrix}$ | Reflection |
| 5 | $T$ | $R$ | $S$ | $\begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix}$ | Rotation |
| 6 | $R$ | $T$ | $S$ | $\begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix}$ | Reflection |

Using (2.3) and the rectifier modulation matrix given in Table 3.2, the inverter modulation matrix $\mathbf{M}_i$ is determined by (3.6).

$$\mathbf{M}_i = \mathbf{M}\mathbf{M}_r^{-1} = (\mathbf{M}_{\mathrm{U}} + \mathbf{M}_{\mathrm{I}} + \mathbf{M}_{\mathrm{N}} + \mathbf{M}_0)\mathbf{M}_r^{-1} \tag{3.6}$$

Substituting (2.4) – (2.7) into (3.6) yields

$$\mathbf{M}_i = \frac{\mathbf{v}_o^* \mathbf{v}_i^T}{\|\mathbf{v}_i\|^2}\mathbf{M}_r^{-1} + \frac{\mathbf{i}_o^* (\mathbf{J}\mathbf{v}_i)^T}{\|\mathbf{v}_i\|^2}\mathbf{M}_r^{-1} + \frac{\mathbf{J}\mathbf{i}_o (\mathbf{J}\mathbf{v}_i)^T}{\|\mathbf{v}_i\|^2}\mathbf{M}_r^{-1} + \mathbf{M}_0\mathbf{M}_r^{-1}. \tag{3.7}$$

Because the rectifier modulation matrix $\mathbf{M}_r$ is a kind of basic geometric transformation as indicated in Table 3.2, from the geometric viewpoint the following relations (3.8) - (3.10) for the $n^{th}$ sector of the input voltages can be obtained.

$$\mathbf{M}_r^{-1} = \mathbf{M}_r^T \tag{3.8}$$

$$(\mathbf{J}\mathbf{v}_i)^T \mathbf{M}_r^{-1} = (-1)^{n+1}(\mathbf{J}\mathbf{M}_r\mathbf{v}_i)^T = (-1)^{n+1}(\mathbf{J}\mathbf{v}_{dc})^T \tag{3.9}$$

$$\|\mathbf{v}_i\| = \|\mathbf{v}_{dc}\| \tag{3.10}$$

Using the relations (3.1), (3.2), (3.6)-(3.10), the general form of the inverter modulation matrix $\mathbf{M}_i$ is finally derived as:

$$\mathbf{M}_i = \mathbf{M}'_{\mathrm{U}} + (-1)^{n+1}\mathbf{M}'_{\mathrm{I}} + (-1)^{n+1}\mathbf{M}'_{\mathrm{N}} + \mathbf{M}'_0 \tag{3.11}$$

where

$$\mathbf{M}'_{\mathrm{U}} = \frac{\mathbf{v}_o^*}{\|\mathbf{v}_{dc}\|^2}(\mathbf{v}_{dc})^T = \frac{1}{v_{max}^{\ 2} + v_{mid}^{\ 2} + v_{min}^{\ 2}}\begin{bmatrix} u^* \\ v^* \\ w^* \end{bmatrix}\begin{bmatrix} v_{max} & v_{mid} & v_{min} \end{bmatrix} \tag{3.12}$$

$$\mathbf{M}'_{\mathrm{I}} = \frac{k_1}{\|\mathbf{v}_{dc}\|^2}\mathbf{i}_o(\mathbf{J}\mathbf{v}_{dc})^T = \frac{k_1}{\sqrt{3}\left(v_{max}^2 + v_{mid}^2 + v_{min}^2\right)}\begin{bmatrix} i_u \\ i_v \\ i_w \end{bmatrix}\begin{bmatrix} v_{mid} - v_{min} & v_{min} - v_{max} & v_{max} - v_{mid} \end{bmatrix} \tag{3.13}$$

$$\mathbf{M}'_{\mathrm{N}} = \frac{k_2}{\|\mathbf{v}_{dc}\|^2}\mathbf{J}\mathbf{i}_o(\mathbf{J}\mathbf{v}_{dc})^T = \frac{k_2}{3\left(v_{max}^2 + v_{mid}^2 + v_{min}^2\right)}\begin{bmatrix} i_v - i_w \\ i_w - i_u \\ i_u - i_v \end{bmatrix}\begin{bmatrix} v_{mid} - v_{min} & v_{min} - v_{max} & v_{max} - v_{mid} \end{bmatrix} \tag{3.14}$$

$$\mathbf{M}_0' = \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \begin{bmatrix} x' & y' & z' \end{bmatrix} \quad ; \quad 0 \le x', y', z' \le 1 \;\; x' + y' + z' = 1. \tag{3.15}$$

It should be noticed that the inverter modulation matrix $\mathbf{M}_i$ is very similar to the modulation matrix $\mathbf{M}$ of the CMC. Each component of the modulation matrix $\mathbf{M}_i$ can be obtained by replacing $\mathbf{v}_i$ in (2.4)–(2.7) with $\mathbf{v}_{dc}$ , except for the sign change which takes place every time the sector of the input voltages changes. Moreover, the functions of each component and of the free parameters in the modulation matrix $\mathbf{M}_i$ are still the same. The component matrix $\mathbf{M}_{\mathrm{U}}'$ produces the required output voltages and the active component of the input current $\mathbf{i}_i$ , while $\mathbf{M}_{\mathrm{I}}'$ controls the reactive component through the free parameter $k_1$ without affecting the output voltages, and $\mathbf{M}_{\mathrm{N}}'$ adjusts the switching pattern through the free parameter $k_2$ .

In summary, the rectifier modulation matrix $\mathbf{M}_r$ and the inverter modulation matrix $\mathbf{M}_i$ can be directly calculated from the instantaneous values of the commanded output voltages, the input or dc-link voltages, the output currents, and the zero voltage (which is determined by the zero-voltage matrix). The output PWM signals for the inverter can then be straightforwardly generated using the double-carrier-based PWM discussed in Section 2.3.2. To exemplify this process, the equation (3.2) will be rewritten in full form as:

$$\overbrace{\begin{bmatrix} u \\ v \\ w \end{bmatrix}}^{\mathbf{v}_o} = \overbrace{\begin{bmatrix} m_{11}^{(i)} & m_{12}^{(i)} & m_{13}^{(i)} \\ m_{21}^{(i)} & m_{22}^{(2)} & m_{23}^{(i)} \\ m_{31}^{(i)} & m_{32}^{(i)} & m_{33}^{(i)} \end{bmatrix}}^{\mathbf{M}_i} \overbrace{\begin{bmatrix} v_{max} \\ v_{mid} \\ v_{min} \end{bmatrix}}^{\mathbf{v}_i} \tag{3.16}$$

Here the element $m_{jk}^{(i)}$ represents the duty cycle which each output phase $\{u,v,w\}$ is connected to each dc link $\{v_{max},v_{mid},v_{min}\}$ during a switching period. The duty cycles must satisfy the following constraints:

$0 \le m_{jk}^{(i)} \le 1$ and $\sum_{k=1}^{3} m_{jk}^{(i)} = 1,\ j \in \{1,2,3\}, k \in \{1,2,3\}$.

The double-carrier-based PWM can be straightforwardly employed by taking the mid-phase voltage $v_{mid}$ as the reference. As a result, the output voltage will be generated from the two dc-link voltages: the upper dc-link voltage ($v_{max} - v_{mid}$) and the lower one ($v_{mid} - v_{min}$). This process can be written mathematically in (3.17).

$$\begin{bmatrix} u - v_{mid} \\ v - v_{mid} \\ w - v_{mid} \end{bmatrix} = \begin{bmatrix} m_{11}^{(i)} \\ m_{21}^{(i)} \\ m_{31}^{(i)} \end{bmatrix} (v_{max} - v_{mid}) + \begin{bmatrix} -m_{13}^{(i)} \\ -m_{23}^{(i)} \\ -m_{33}^{(i)} \end{bmatrix} (v_{mid} - v_{min}) \tag{3.17}$$

As demonstrated in Figure 2.4, when the two normalized triangular carriers are used, only the first and the third columns of the inverter modulation matrix $\mathbf{M}_i$ will become the references whose the general forms are expressed as shown in (3.18)-(3.21). The flow chart of the whole steps is drawn in Figure 3.6.

$$\begin{bmatrix} m_{11}^{(i)} \\ m_{21}^{(i)} \\ m_{31}^{(i)} \end{bmatrix} = \begin{bmatrix} m_{11}'^{(i)} + x' \\ m_{21}'^{(i)} + x' \\ m_{31}'^{(i)} + x' \end{bmatrix} \tag{3.18}$$

$$\begin{bmatrix} m_{13}^{(i)} \\ m_{23}^{(i)} \\ m_{33}^{(i)} \end{bmatrix} = \begin{bmatrix} m_{13}'^{(i)} + z' \\ m_{23}'^{(i)} + z' \\ m_{33}'^{(i)} + z' \end{bmatrix} \tag{3.19}$$

where

$$\begin{bmatrix} m_{11}'^{(i)} \\ m_{21}'^{(i)} \\ m_{31}'^{(i)} \end{bmatrix} = \frac{1}{\left(v_{max}^2 + v_{mid}^2 + v_{min}^2\right)} \begin{pmatrix} v_{max} \begin{bmatrix} u^* \\ v^* \\ w^* \end{bmatrix} + (-1)^{n+1} \frac{k_1}{\sqrt{3}} (v_{mid} - v_{min}) \begin{bmatrix} i_u \\ i_v \\ i_w \end{bmatrix} + \\ (-1)^{n+1} \frac{k_2}{3} (v_{mid} - v_{min}) \begin{bmatrix} i_v - i_w \\ i_w - i_u \\ i_u - i_v \end{bmatrix} \end{pmatrix} \tag{3.20}$$

$$\begin{bmatrix} -m_{13}'^{(i)} \\ -m_{23}'^{(i)} \\ -m_{33}'^{(i)} \end{bmatrix} = -\frac{1}{\left(v_{max}^2 + v_{mid}^2 + v_{min}^2\right)} \left( \begin{aligned} & v_{min} \begin{bmatrix} u^* \\ v^* \\ w^* \end{bmatrix} + (-1)^{n+1} \frac{k_1}{\sqrt{3}} \left(v_{max} - v_{mid}\right) \begin{bmatrix} i_u \\ i_v \\ i_w \end{bmatrix} \\ & + (-1)^{n+1} \frac{k_2}{3} \left(v_{max} - v_{mid}\right) \begin{bmatrix} i_v - i_w \\ i_w - i_u \\ i_u - i_v \end{bmatrix} \end{aligned} \right) \quad (3.21)$$

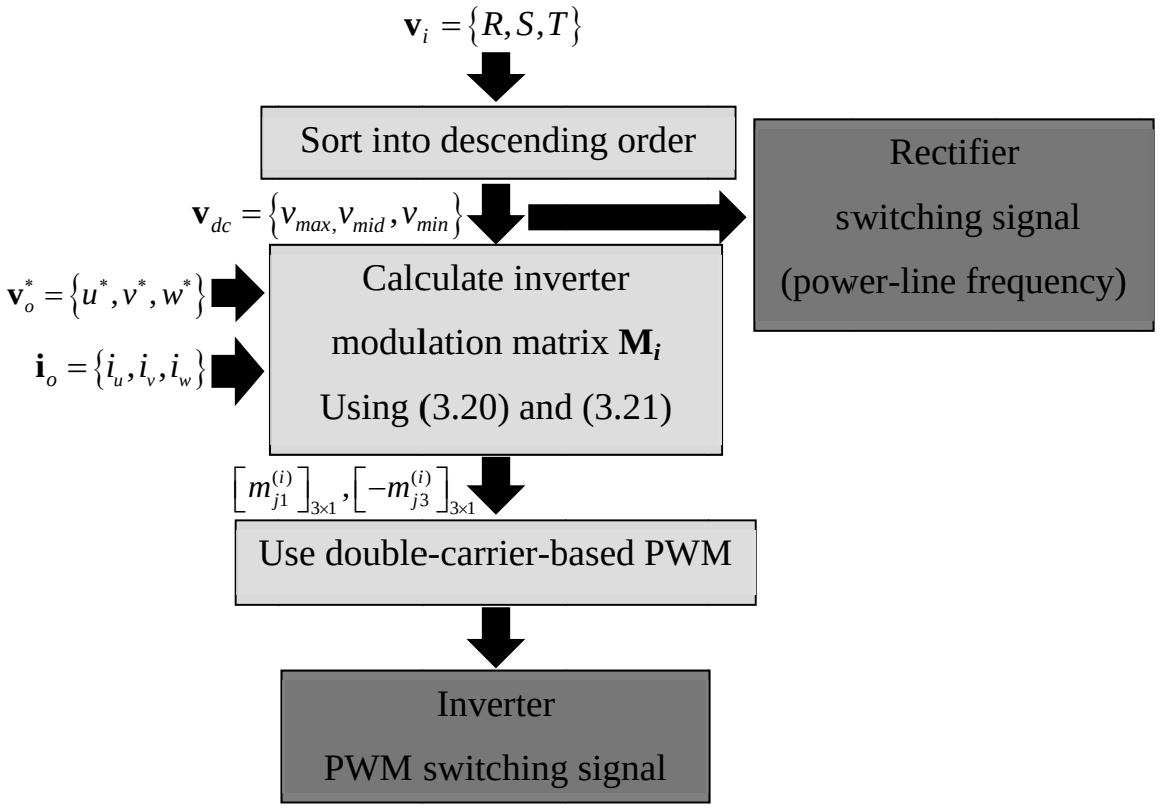



Figure 3.6 Flow chart of the modulation strategy for the proposed 3L-BTB converters

### 3.3.2 Control of Input Reactive Power of the Proposed 3L-BTB Converters

#### Case I) Three-Level Indirect Matrix Converters

One important task of the back-to-back converters is to control the power factor or reactive power at the input. This can be achieved with the help of the modulation matrix derived in (3.11) - (3.15). Consider here first for the case of the

3L-IMC, the relations among the input, output, and dc-link currents of the 3L-IMC in Figure 3.7 can be written as shown in (3.22)-(3.24).

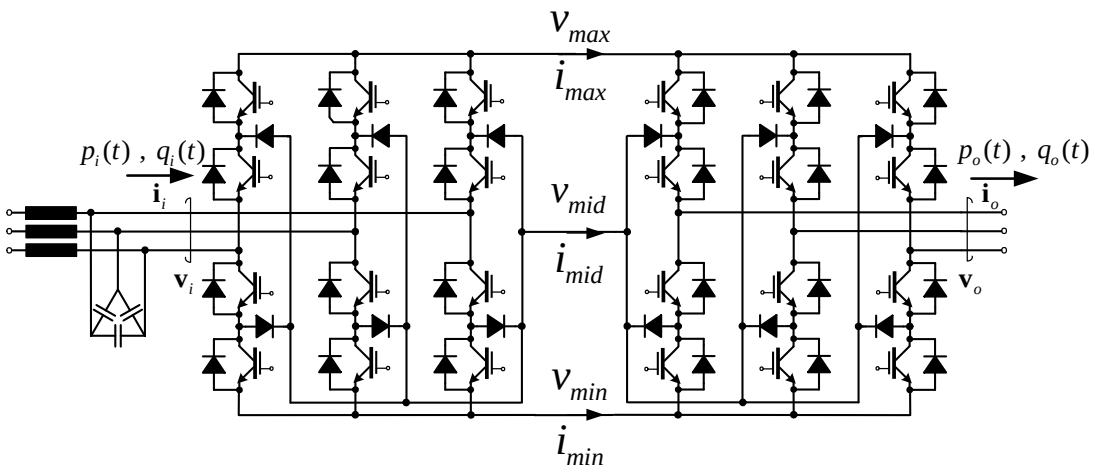



Figure 3.7 Definitions of variables in the 3L-IMC topology.

Rectifier stage: $$\mathbf{i}_i = \mathbf{M}_r^T \mathbf{i}_{dc} \tag{3.22}$$

Inverter stage: $$\mathbf{i}_{dc} = \mathbf{M}_i^T \mathbf{i}_o \tag{3.23}$$

where $\mathbf{i}_{dc} = \{i_{max}, i_{mid}, i_{min}\}$

$$\mathbf{i}_i = \mathbf{M}_r^T \mathbf{M}_i^T \mathbf{i}_o = (\mathbf{M}_i \mathbf{M}_r)^T \mathbf{i}_o \tag{3.24}$$

From (3.4) and (2.3)-(2.7), then the input current finally becomes

$$\begin{aligned} \mathbf{i}_i &= \mathbf{M}^T \mathbf{i}_o \\ &= \underbrace{\mathbf{v}_i \frac{\mathbf{v}_o^{*T} \mathbf{i}_o}{\|\mathbf{v}_i\|^2}}_{\mathbf{M}_U^T \mathbf{i}_o} + \underbrace{\mathbf{J}\mathbf{v}_i \frac{k_1}{\|\mathbf{v}_i\|^2} \mathbf{i}_o^T \mathbf{i}_o}_{\mathbf{M}_I^T \mathbf{i}_o} + \underbrace{\mathbf{J}\mathbf{v}_i \frac{k_2}{\|\mathbf{v}_i\|^2} \left(\mathbf{J}\mathbf{i}_o\right)^T \mathbf{i}_o}_{\mathbf{M}_N^T \mathbf{i}_o} \\ &= \underbrace{\mathbf{v}_i \frac{p_o}{\|\mathbf{v}_i\|^2}}_{\text{active current}} + \underbrace{\mathbf{J}\mathbf{v}_i \frac{k_1}{\|\mathbf{v}_i\|^2} \|\mathbf{i}_o\|^2}_{\text{reactive current}} \end{aligned} \tag{3.25}$$

where $p_o(t) = \mathbf{v}_o^T \mathbf{i}_o = \mathbf{v}_o^{*T} \mathbf{i}_o$ is the instantaneous output power.

From (3.25), it can be seen that the input current $\mathbf{i}_i$ has a unique active component (in phase with the input voltage $\mathbf{v}_i$), which is determined by the output power at that instant. Also, the input current can have a reactive component (perpendicular to the input voltage), which is controlled by the free parameter $k_1$. This

characteristic is consistent with the input-output current equation of the CMC in (2.2) derived in [8], which confirms the equivalence between the 3L-IMC and the CMC. We can therefore control the reactive power or the power factor at the input side of the converter by adjusting the free parameter $k_1$ so long as no overmodulation occurs. The instantaneous input active power $p_i(t)$ and reactive power $q_i(t)$ at the converter terminals are then given by (3.26) and (3.27), respectively.

$$\begin{aligned} p_i(t) &= \mathbf{v}_i^T \mathbf{i}_i \\ &= p_o(t) \end{aligned} \tag{3.26}$$

$$\begin{aligned} q_i(t) &= \left(-\mathbf{J}\mathbf{v}_i\right)^T \mathbf{i}_i \\ &= -k_1 \left\|\mathbf{i}_o(t)\right\|^2 \end{aligned} \tag{3.27}$$

It should be note that the reactive power in (3.27) does not include the reactive power generated by the filter capacitors.

## Case II) Symmetrical Three-Level Back-to-Back Converters

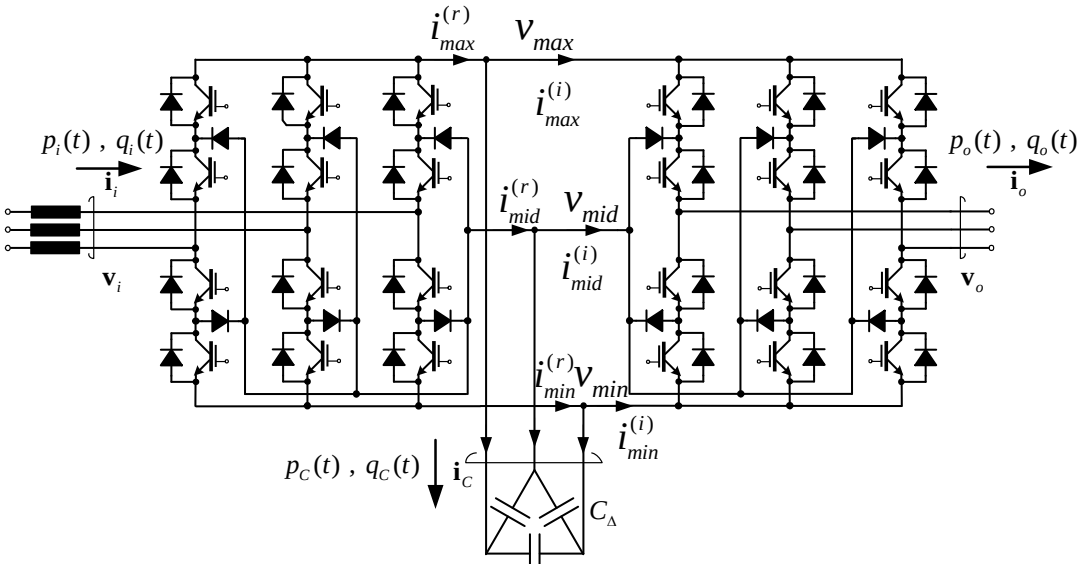



Figure 3.8 Definitions of variables in the S3L-BTB converter topology.

For the S3L-BTB converter shown in Figure 3.8, due to the existing of the capacitor network at the dc link, we have to distinguish the dc-link currents at the

rectifier side $\mathbf{i}_{dc}^{(r)} = \left\{ i_{max}^{(r)}, i_{mid}^{(r)}, i_{min}^{(r)} \right\}$ from those at the inverter side $\mathbf{i}_{dc}^{(i)} = \left\{ i_{max}^{(i)}, i_{mid}^{(i)}, i_{min}^{(i)} \right\}$. In this case, under the same rectifier and inverter modulation matrices, the relations among all the currents in the converter become (3.28) - (3.30).

Rectifier stage: $$\mathbf{i}_i = \mathbf{M}_r^T \mathbf{i}_{dc}^{(r)} \tag{3.28}$$

Inverter stage: $$\mathbf{i}_{dc}^{(i)} = \mathbf{M}_i^T \mathbf{i}_o \tag{3.29}$$

with $$\mathbf{i}_{dc}^{(r)} = \mathbf{i}_{dc}^{(i)} + \mathbf{i}_C \tag{3.30}$$

where $\mathbf{i}_{dc}^{(r)} = \left\{ i_{max}^{(r)}, i_{mid}^{(r)}, i_{min}^{(r)} \right\}$ is the dc-link current at the rectifier side after filtered by the capacitor–network,

$\mathbf{i}_{dc}^{(i)} = \left\{ i_{max}^{(i)}, i_{mid}^{(i)}, i_{min}^{(i)} \right\}$ is the dc-link current at the inverter side generated by the inverter stage, and

$\mathbf{i}_C = 3C_\Delta \dfrac{d\mathbf{v}_{dc}}{dt}$ is the current flowing through the capacitor network.

Considering that the rectifier modulation matrix is constant almost everywhere except at the switching instant (i.e. $d\mathbf{M}_r / dt = 0$) and that the currents flowing through the input inductors must be continuous, the input current of the S3L-BTB converter can be derived with the relation (3.8) as shown below.

$$\begin{aligned}
\mathbf{i}_i &= \mathbf{M}_r^T (\mathbf{M}_i^T \mathbf{i}_o + \mathbf{i}_C) = (\mathbf{M}_i \mathbf{M}_r)^T \mathbf{i}_o + \mathbf{M}_r^T \mathbf{i}_C \\
&= (\mathbf{M}_i \mathbf{M}_r)^T \mathbf{i}_o + \mathbf{M}_r^T 3C_\Delta \frac{d\mathbf{v}_{dc}}{dt} \\
&= (\mathbf{M}_i \mathbf{M}_r)^T \mathbf{i}_o + 3C_\Delta \frac{d\mathbf{M}_r^T \mathbf{v}_{dc}}{dt} \\
&= (\mathbf{M}_i \mathbf{M}_r)^T \mathbf{i}_o + 3C_\Delta \frac{d\mathbf{M}_r^{-1} \mathbf{v}_{dc}}{dt} \\
&= (\mathbf{M}_i \mathbf{M}_r)^T \mathbf{i}_o + 3C_\Delta \frac{d\mathbf{v}_i}{dt} \\
&= \mathbf{M}^T \mathbf{i}_o + 3C_\Delta \frac{d\mathbf{v}_i}{dt} \\
&= \underbrace{\mathbf{v}_i \frac{p_o}{\|\mathbf{v}_i\|^2}}_{\text{active current}} + \underbrace{\mathbf{J}\mathbf{v}_i \frac{k_1}{\|\mathbf{v}_i\|^2} \|\mathbf{i}_o\|^2}_{\text{reactive current}} + 3C_\Delta \frac{d\mathbf{v}_i}{dt}
\end{aligned} \tag{3.31}$$

According to (3.31), while the first two terms on the right-hand side is the same as the input current of the 3L-IMC in (3.25), the last term is caused by the charging/discharging current of the capacitor network which is moved into the dc link. This additional-term current can be proved to be equal to the capacitor current of the filter in the 3L-IMC topology. Therefore, the input current of the S3L-BTB converter is exactly equal to the input current of the 3L-IMC taking into account the filter current. The power factor controllability of the two converters is thus the same. We can therefore control the reactive power or the power factor at the input side of the proposed converters by adjusting the free parameter $k_1$ so long as no overmodulation occurs.

The instantaneous input active power $p_i(t)$ and reactive power $q_i(t)$ for this topology can be calculated as follows.

$$p_i(t) = \mathbf{v}_i^T \mathbf{i}_i = p_o(t) + \mathbf{v}_i^T \mathbf{M}_r^T \mathbf{i}_C \tag{3.32}$$

$$= p_o(t) + \left(\mathbf{M}_r \mathbf{v}_i\right)^T \mathbf{i}_C$$

Substituting (3.1) into (3.32) yields

$$p_i(t) = p_o(t) + \underbrace{\mathbf{v}_{dc}^T \mathbf{i}_C}_{p_C(t)} \quad . \tag{3.33}$$

Eq. (3.33) reveals that the amount of instantaneous input power is equal to the output power plus the net charging/discharging power of the dc-link capacitors. And under the balanced conditions where the net charging/discharging power is zero,

$$p_i(t) = p_o(t)$$

is obtained.

On the other hand, from (3.27) the input reactive power $q_i(t)$ can be obtained as:

$$q_i(t) = \left(-\mathbf{J}\mathbf{v}_i\right)^T \mathbf{i}_i = -k_1 \left\|\mathbf{i}_o(t)\right\|^2 + \overbrace{\left(-\mathbf{J}\mathbf{v}_i\right)^T \mathbf{M}_r^T \mathbf{i}_C}^{q_C(t)} \quad . \tag{3.34}$$

Considering the second term on the right-hand side,

$$q_C(t) = \left(-\mathbf{J}\mathbf{v}_i\right)^T \mathbf{M}_r^T \mathbf{i}_C = \left(-\mathbf{J}\mathbf{v}_i\right)^T \left(3C_\Delta \frac{d\mathbf{v}_i}{dt}\right) \tag{3.35}$$

which is the same reactive power required as when the capacitor network is connected in front of the converter of the 3L-IMC.

For the normal case which the input line-to-line voltages are sinusoidal, the reactive power consumed by the capacitor network can be calculated as

$$q_C(t) = -\frac{3\|\mathbf{v}_i\|^2}{2X_{C_\Delta}} = -\frac{3V_i^2}{X_{C_\Delta}} \tag{3.36}$$

where $V_i$ is the rms value of the line-to-line voltages. As a conclusion, taking the capacitor network into consideration the total reactive power $q_i(t)$ consumed by the 3L-IMC or the S3L-BTB converter is given by

$$q_i(t) = -k_1\|\mathbf{i}_o(t)\|^2 - \frac{3V_i^2}{X_{C_\Delta}} \quad . \tag{3.37}$$

The input power factor can therefore be controlled through the free parameter $k_1$ so long as there is no overmodulation. However, if $\mathbf{M} = \mathbf{M}_U + \mathbf{M}_0$ $(k_1 = k_2 = 0)$ is selected, the input reactive power will always be $q(t) = -\frac{3V_i^2}{X_{C_\Delta}}$ causing the input current to be leading. Nevertheless, the effect of this reactive current generated from the capacitor network can be compensated by adjusting the free parameter $k_1$ to make $q_i(t) = 0$ (unity power factor). In such a case,

$$k_1\|\mathbf{i}_o(t)\|^2 = -\frac{3V_i^2}{X_{C_\Delta}} \tag{3.38}$$

$$k_1 = -\frac{3V_i^2}{\|\mathbf{i}_o(t)\|^2 X_{C_\Delta}} \tag{3.39}$$

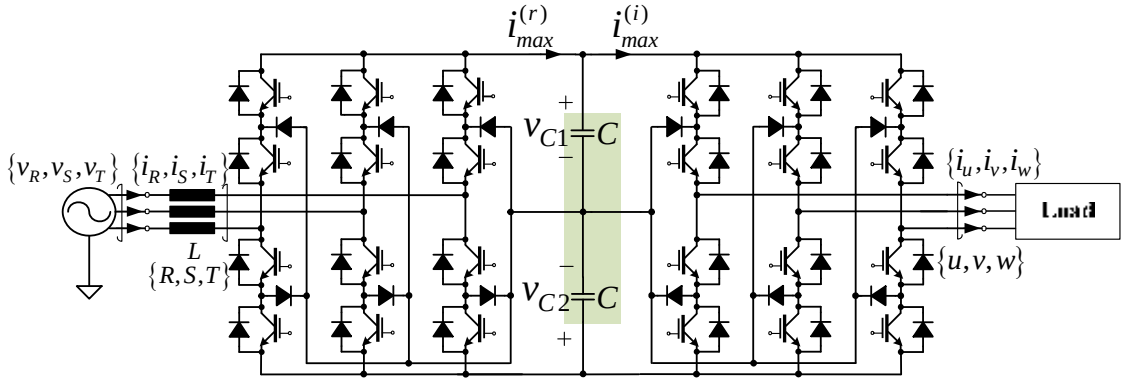
In summary, from the input-output viewpoint, the proposed 3L-BTB converters which use the modulation matrices $\mathbf{M}_r$ in Table 3.2 and $\mathbf{M}_i$ in (3.11) behave exactly like the CMC. This perfect equivalence cannot be obtained with other conventional indirect-type matrix converters, which are constructed based on the two-level BTB converters, due to the topological difference between the three-level and two-level dc links.

# CHAPTER IV
# SIMULATION RESULTS

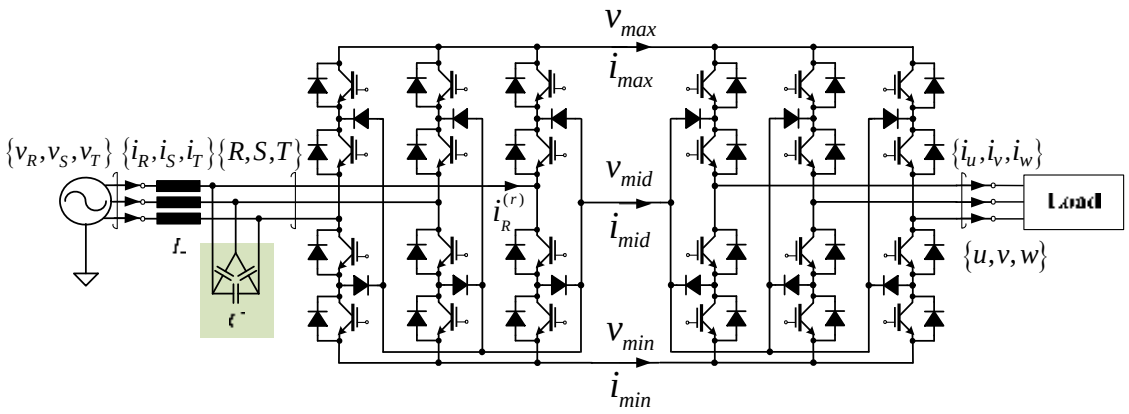
After deriving the novel topologies for 3L-BTB converters in conjunction with the corresponding modulation strategies in Chapter III, this Chapter will confirm the performances of them as AC/AC converters by simulation using MATLAB/Simulink. The performances of the conventional and the proposed 3L-BTB converters shown in Figure 4.1 are tested under several different conditions according to Table 4.1.

Table 4.1 List of simulation conditions for performance testing of the conventional and the proposed 3L-BTB converters.

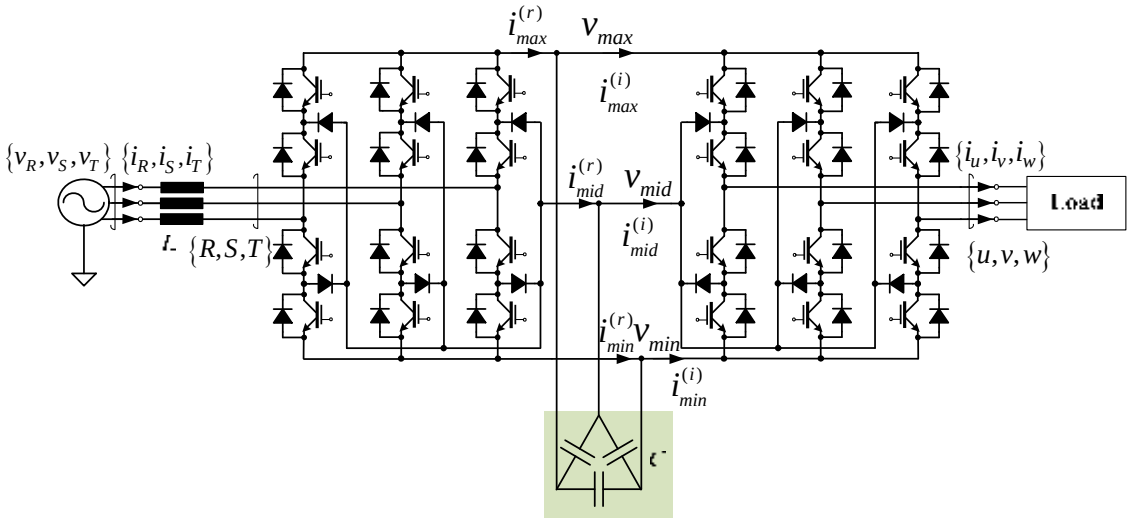
<table>
<tr><th rowspan="2">Case</th><th rowspan="2" colspan="2">Objectives</th><th colspan="3">Testing conditions</th></tr>
<tr><th>Modulation index $\left(V_o/V_i\right)$</th><th>Output frequency (Hz)</th><th>Load</th></tr>
<tr><td>1</td><td colspan="2">Comparison with the conventional 3L-BTB converter</td><td>0.5</td><td>50</td><td rowspan="9">series RL load<br>R = 24Ω<br>L = 33.3 mH</td></tr>
<tr><td>2</td><td colspan="2" rowspan="2">Output voltage variation</td><td>0.3</td><td>50</td></tr>
<tr><td>3</td><td>0.86</td><td>50</td></tr>
<tr><td>4</td><td colspan="2" rowspan="2">Output frequency variation</td><td>0.86</td><td>25</td></tr>
<tr><td>5</td><td>0.86</td><td>100</td></tr>
<tr><td>6</td><td rowspan="4">Input power factor compensation</td><td>No compensation</td><td>0.7</td><td>50</td></tr>
<tr><td>7</td><td>Unity power factor</td><td>0.7</td><td>50</td></tr>
<tr><td>8</td><td>Lagging compensation</td><td>0.7</td><td>50</td></tr>
<tr><td>9</td><td>Leading compensation</td><td>0.7</td><td>50</td></tr>
<tr><td>10</td><td rowspan="2">Regenerative operation</td><td>No compensation</td><td>0.7</td><td>25</td><td rowspan="2">series RL with back-EMF<br>R = 5 Ω<br>L = 33.3 mH</td></tr>
<tr><td>11</td><td>Unity power factor</td><td>0.7</td><td>25</td></tr>
</table>




(a)




(b)




(c)

Figure 4.1 Three-level BTB converter topologies. (a) conventional 3L-BTB converter (b) 3L-IMC (c) S3L-BTB converter

The system parameters common to all conditions used in the simulation are as follows:

Supply voltage: balanced three-phase line-to-line voltage 380 $V_{rms}$ 50 Hz

PWM switching frequency: 12.2 kHz

Delta-connected capacitors: $C$ = 4.2 μF  Line reactance: $L$ = 5 mH

The zero-voltage matrix in (3.15), (3.18) and (3.19) is chosen as:

$$x' = -\min(m_{11}'^{(i)}, m_{21}'^{(i)}, m_{31}'^{(i)}), \quad z' = -\min(m_{13}'^{(i)}, m_{23}'^{(i)}, m_{33}'^{(i)}), \qquad y' = 1 - x' - z'$$

The modulation free parameters: $k_1 = 0$ except for the cases 7, 8, 9 and 11, and $k_2 = 0$ for all conditions.

## 4.1 Behavior Comparison among the Conventional and the Proposed 3L-BTB Converters

In this section, the conventional 3L-BTB converter is simulated along with the proposed 3L-BTB converters under the same conditions to point out the differences between the conventional and the novel 3L-BTB converters. It should be noted that significant differences among these topologies are the configuration and the position of the capacitor network as highlighted in Figure 4.1.

Simulation results in Figure 4.2(b)-(c) reveal evidently that the behaviors of the 3L-IMC and S3L-BTB converters are equivalent to those of the direct matrix converter [8]. Given the balanced three-phase sinusoidal supply voltages $\{v_R, v_S, v_T\}$, they are capable of producing the PWM output voltages $\{u,v,w\}$ from the unidirectional three-level dc link without any distortion as can be observed from the resultant balanced sinusoidal output currents $\{i_u, i_v, i_w\}$. Most importantly is that the proposed converters can achieve balanced sinusoidal supply currents $\{i_R, i_S, i_T\}$ like those of the conventional 3L-BTB converter in Figure 4.2(a).

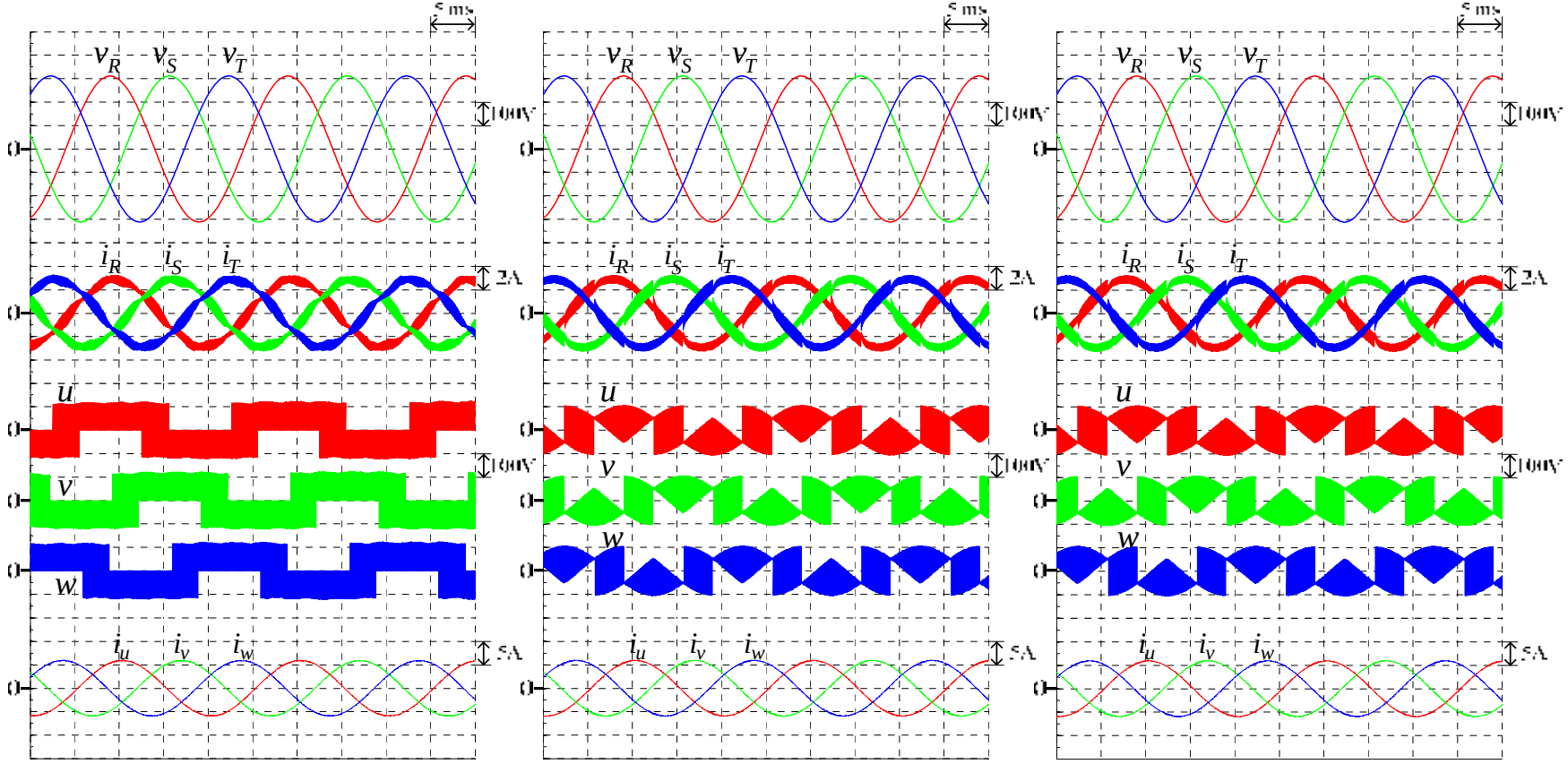
Figure 4.3(b)-(c) give some more details regarding the internal dc link voltages and currents along with the input-output voltages and currents. They clearly illustrate that the proposed 3L-BTB converters can obtain the sinusoidal supply current without PWM operation of the rectifier. The rectifier switches at the power-line frequency so that the three dc-link voltages track the max-mid-min input

voltages. Consequently, the input terminal voltage of the converter, *R*, is no longer of PWM waveform like that of the conventional 3L-BTB converter shown in Figure 4.3(a), but becomes sinusoidal instead. This confirms the low losses and low EMI properties of the proposed converters compared to the conventional converter which employs PWM operation at the rectifier stage to achieve two constant dc-link voltages.

Considering the dc-link current at the 'max' link of the 3L-IMC in Figure 4.3(b), the impulsive PWM current $i_{max}$ at the dc link is generated by the back-end inverter, and is then rearranged by the action of the rectifier to become the PWM input current $i_R^{(r)}$. The PWM input current is finally filtered to be a sinusoidal supply current $i_R$.

For the S3L-BTB converter, due to the effect of the capacitor network in the dc link, the impulsive PWM current resulting from the back-end inverter $i_{max}^{(i)}$ is filtered at the dc-link to be a smooth current $i_{max}^{(r)}$. The rectifier-side dc-link current $i_{max}^{(r)}$ flows through the anti-parallel diodes which connect the maximum input phase to the 'max' link, and its waveform is a portion of a sinusoidal function. The phase shift of the rectifier-side dc-link current $i_{max}^{(r)}$ relative to the max-link voltage $v_{max}$ can be observed. Similar results occur in the 'mid' and 'min' links as well. The three rectifier-side dc-link currents are then recombined by the rectifier to yield the sinusoidal supply current $i_R$. It is concluded then that the symmetrical dc-link capacitors together with the line reactors in the S3L-BTB converter still act as the low-pass filter similar to that of the 3L-IMC topology. This same filtering function is not possible for the conventional 3L-BTB converter topology because the dc link lacks the three-phase symmetry, i.e. it is only a symmetrical two-phase circuit. In other words, the conventional back-to-back converter cannot achieve sinusoidal supply currents without PWM operation at the front-end rectifier.

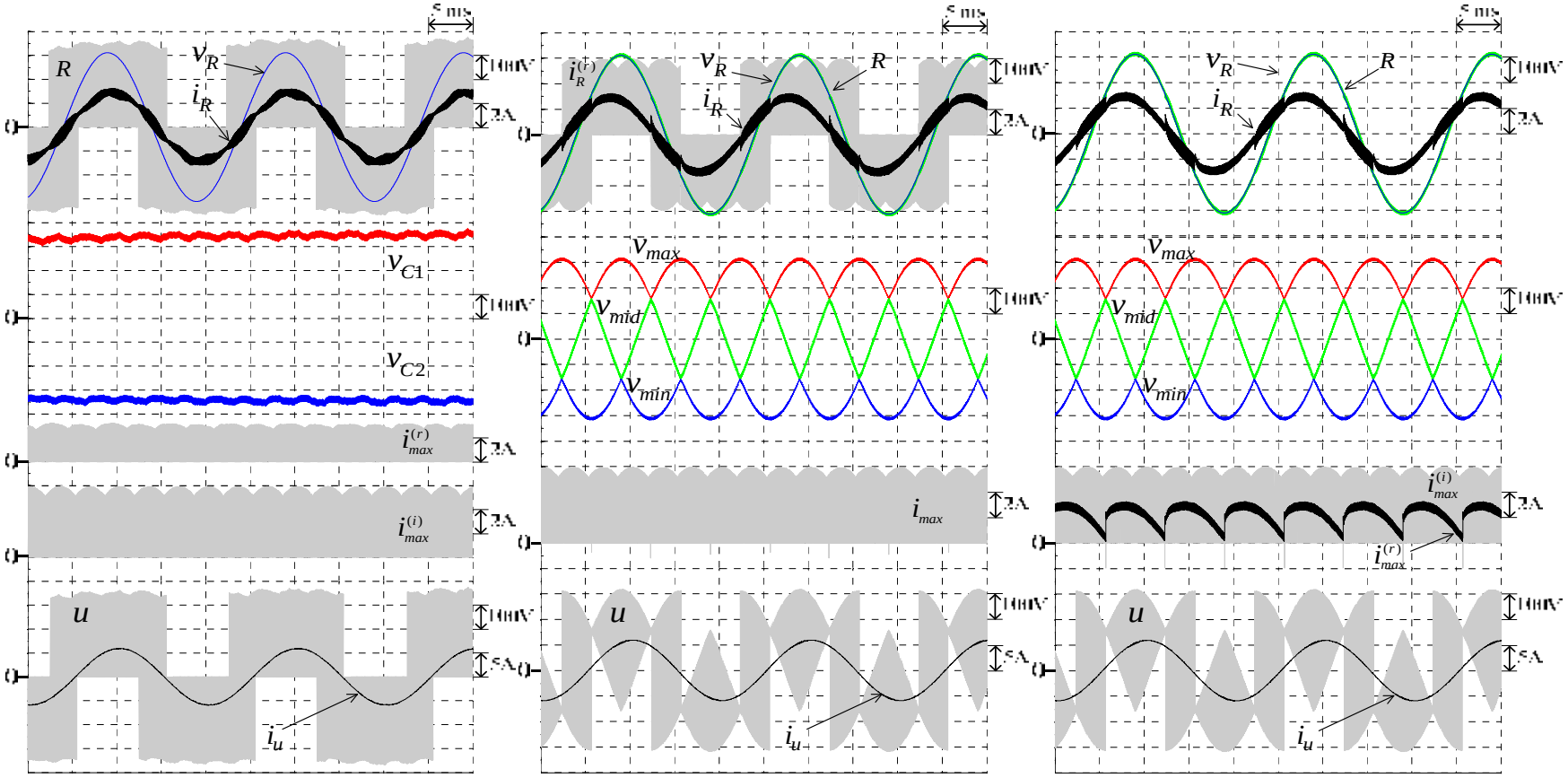
It should be pointed out that the phase leading of the supply current $i_R$ in both proposed converters is due to the capacitive currents. This effect can be alleviated by appropriately utilizing the free parameter $k_1$ for the input reactive power compensation as shown later in Section 4.4.




(a) (b) (c)

Figure 4.2 Simulated input-output waveforms of the 3L-BTB converters working under condition 1 ($M$ = 0.5, $f_o$ = 50 Hz)

(a) conventional 3L-BTB converter (b) 3L-IMC (c) S3L-BTB converter




(a) (b) (c)

Figure 4.3 External and internal waveforms of the 3L-BTB converters working under condition 1 ($M$ = 0.5, $f_o$ = 50 Hz)

(a) conventional 3L-BTB converter (b) 3L-IMC (c) S3L-BTB converter

## 4.2 **Output Voltage Variation**

Figure 4.4 - 4.7 are the simulation results of the proposed converters under conditions 2 and 3 of Table 4.1 at low and high modulation indices with fixed output frequency ($M$ = 0.3 and 0.86, $f_o$ = 50 Hz). The results confirm that the proposed 3L-BTB converters are capable of varying the magnitude of the output voltages as commanded. They can generate the balanced three-phase sinusoidal output currents, while achieving the balanced three-phase sinusoidal supply currents as shown in Figure 4.4 and 4.6.

Figure 4.5 and 4.7 present the detailed responses of the proposed 3L-BTB converters. In case of the low modulation index, it is seen that the smooth dc-link current $i_{max}^{(r)}$ may become negative in some region due to the effect of the reactive current generated by the capacitor network seen in Figure 4.5(b). That negative current flows through the IGBTs instead of the anti-parallel diodes.

Moreover, the inverter modulation functions for phase $u$, $m_{11}^{(i)}$ and $-m_{13}^{(i)}$, which are calculated from (3.18) - (3.21), are also shown in Figure 4.5 and 4.7. The larger the magnitudes of the commanded output voltages are, the higher the magnitudes of the modulation functions become. These modulation functions are compared used as references in the double-carrier-based PWM process to generate the PWM output voltage, $u$. According to [8], the output voltage $u$ is of unipolar mode if either $m_{11}^{(i)}$ or $-m_{13}^{(i)}$ is zero. Otherwise, it is in a dipolar mode and switches between the three dc-link voltages.

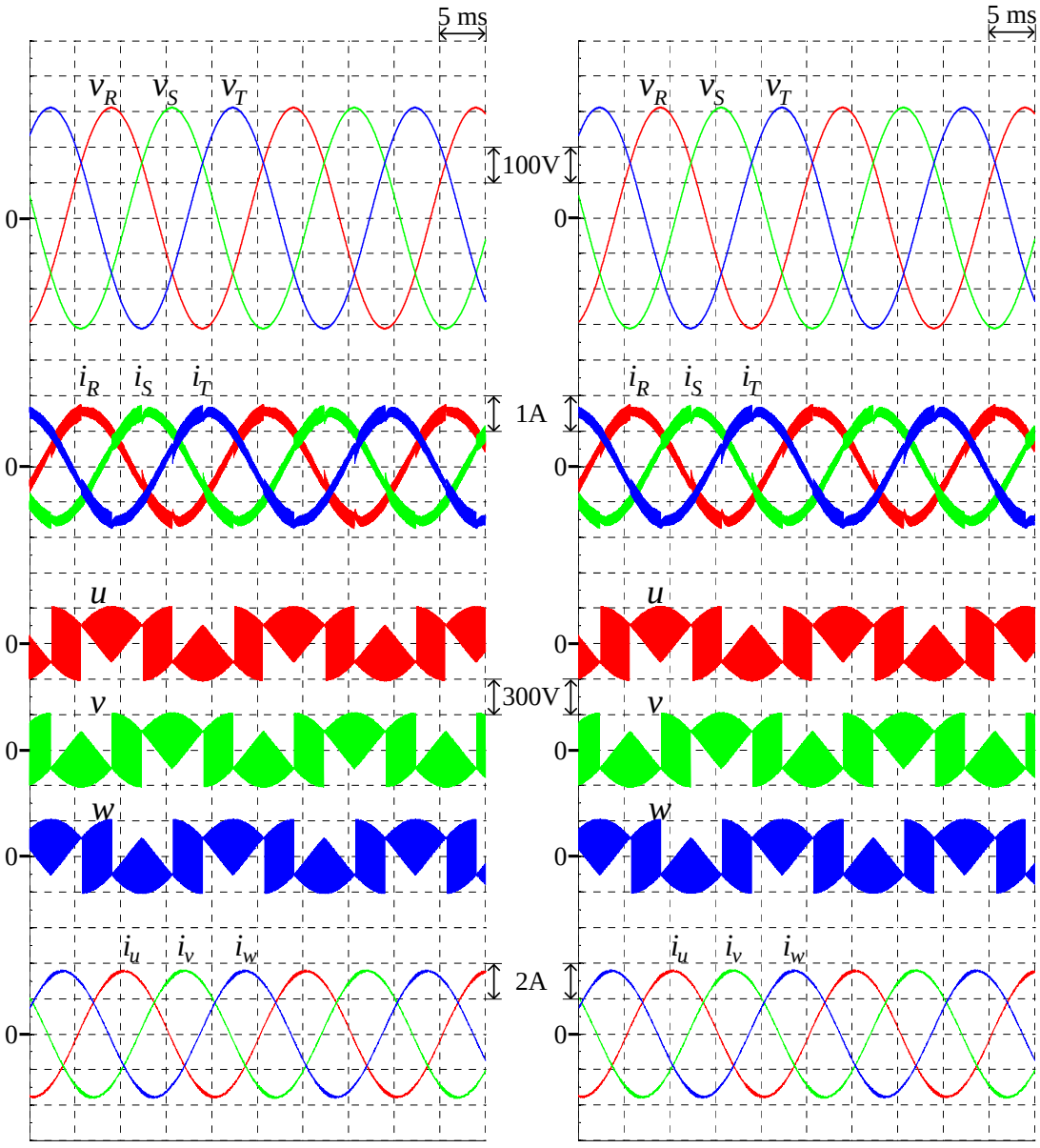



Figure 4.4 Simulated input-output waveforms of the proposed 3L-BTB converters under output voltage variation ($M$ = 0.3, $f_o$ = 50 Hz) (a) 3L-IMC (b) S3L-BTB converter

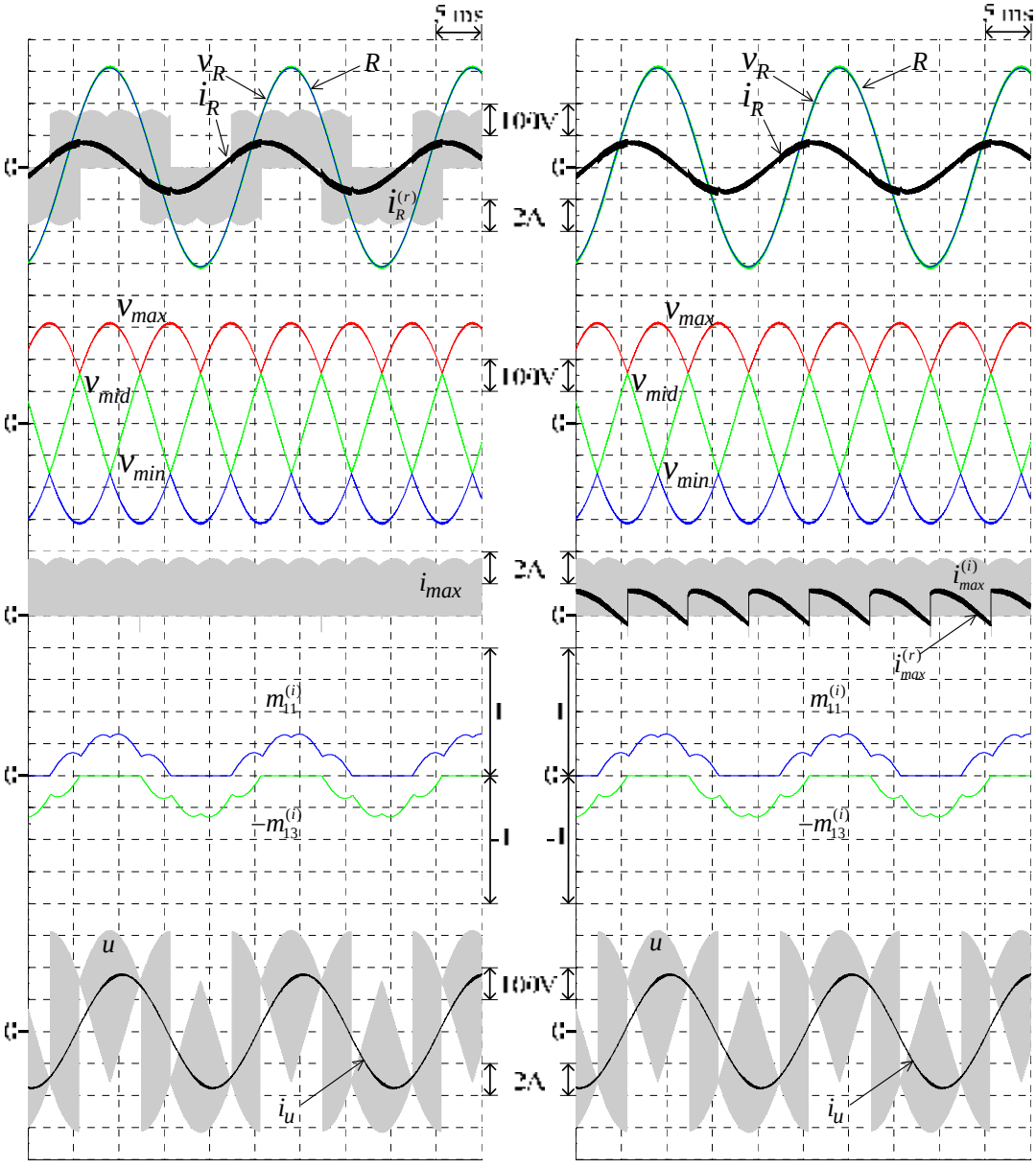



Figure 4.5 External and internal waveforms of the proposed 3L-BTB converters under output voltage variation ($M$ = 0.3, $f_o$ = 50 Hz) (a) 3L-IMC (b) S3L-BTB converter

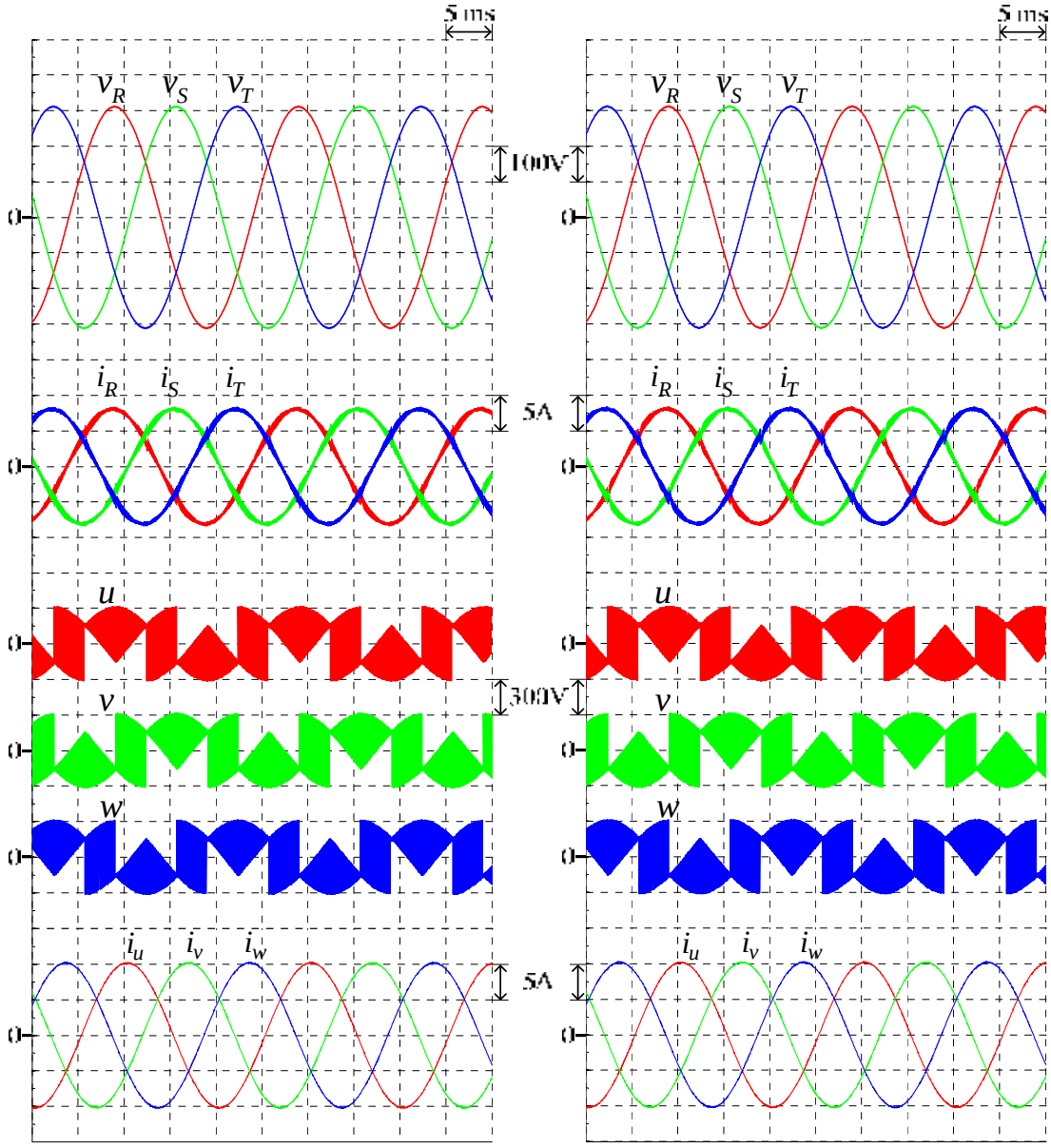



Figure 4.6 Simulated input-output waveforms of the proposed 3L-BTB converters under output voltage variation ($M$ = 0.86, $f_o$ = 50Hz) (a) 3L-IMC (b) S3L-BTB converter

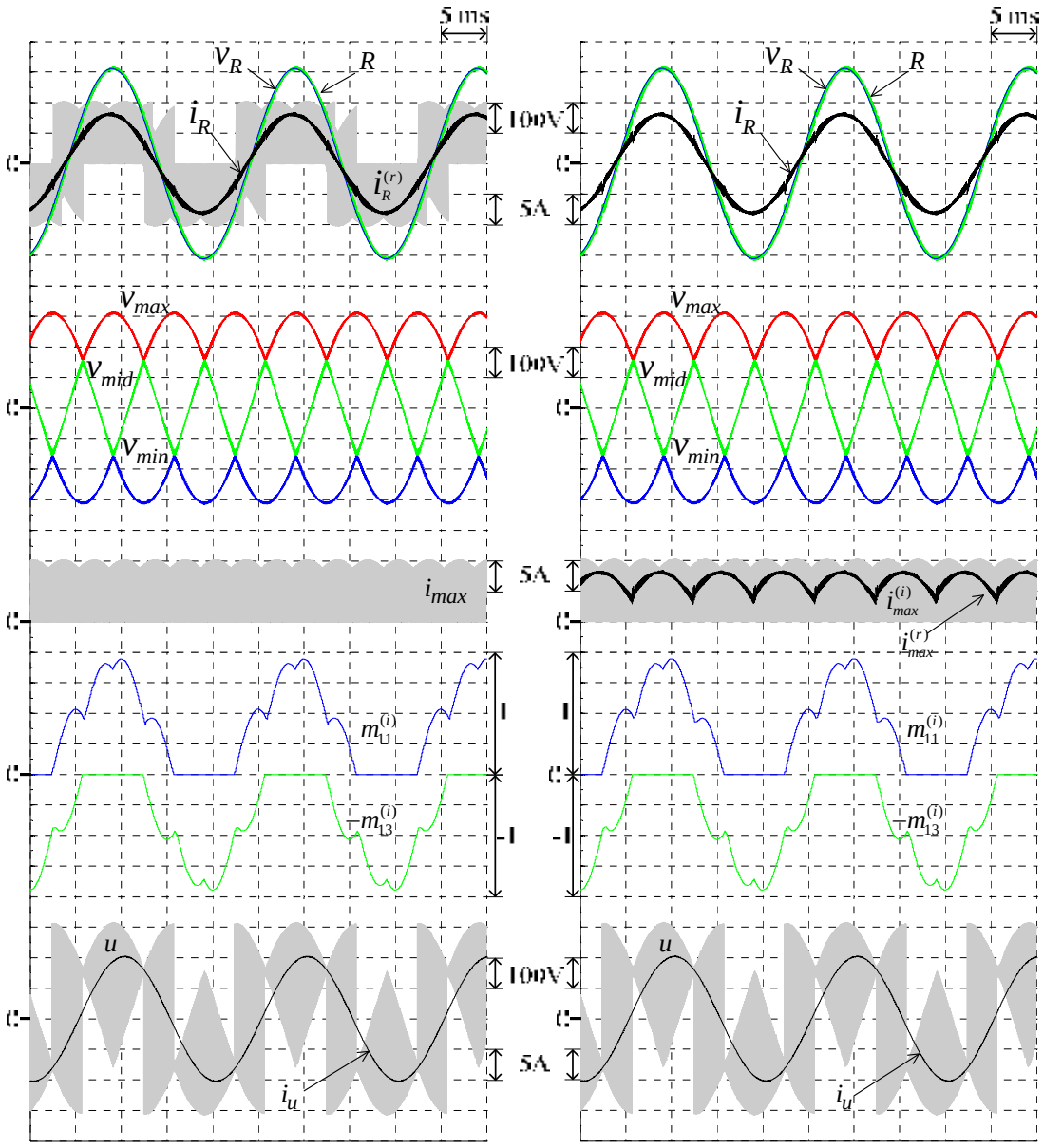
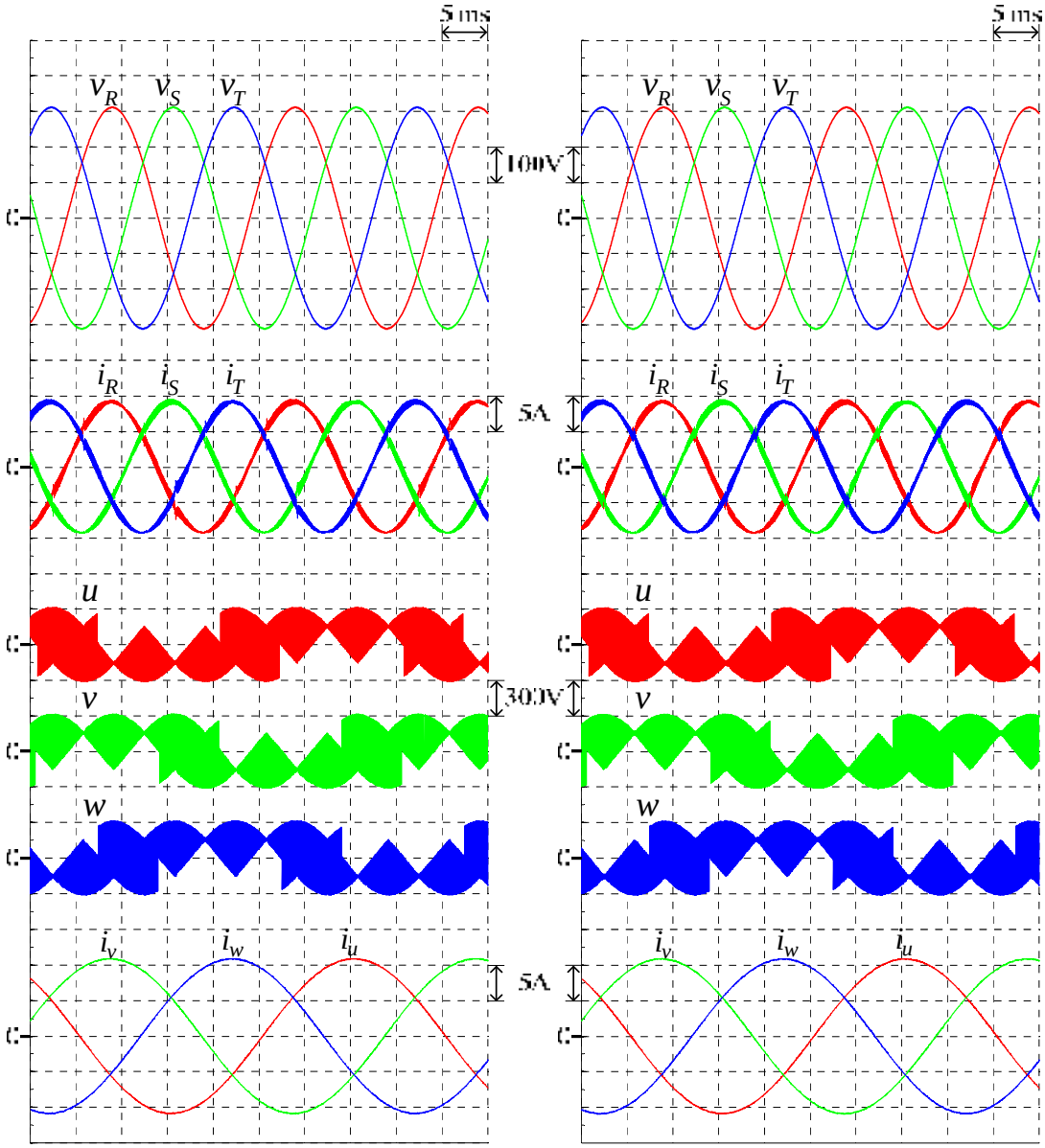



Figure 4.7 External and internal waveforms of the proposed 3L-BTB converters under output voltage variation ($M$ = 0.86, $f_o$ = 50 Hz) (a) 3L-IMC (b) S3L-BTB converter

## 4.3 **Output Frequency Variation**

Figure 4.8 - 4.11 are the simulation results of the proposed 3L-BTB converters under conditions 4 and 5 of Table 4.1, which are the operating conditions of output frequency below and above the input frequency with fixed output modulation index ($f_o$ = 25 Hz and 100 Hz, $M$ = 0.86). Figure 4.8 and 4.10 show that the proposed 3L-BTB converters can vary the output frequency freely, while preserving the balanced three-phase sinusoidal supply currents. In fact, the output power factors are also varied when varying the output frequency, so it can be said that the proposed 3L-BTB converters still function well under various output power factors.

Figure 4.9 and 4.11 show responses of some quantities of the proposed 3L-BTB converters. It can be seen that changing the frequency of the commanded output voltages has a direct effect on the inverter modulation functions, $m_{11}^{(i)}$ and $-m_{13}^{(i)}$. Their waveforms become more complicated, having the commanded output frequency superimposed on the input frequency. Another effect is on the output power factor. The increased output frequency (Figure 4.11) causes the output power factor to become $41^o$ lagging, and the negative pulse current can be observed in the dc-link currents, $i_{max}$ and $i_{max}^{(i)}$, in the 3L-IMC and S3L-BTB converters, respectively. In case of the former one, the current can flow properly through the bidirectional switch of the NPC structure, i.e. through either IGBTs or anti-parallel diodes. For the latter case, however, the symmetrical capacitor network at the dc link removes the negative impulsive currents through its filtering function. The resultant current $i_{max}^{(r)}$ becomes smooth and unidirectional, and thus flows through the anti-parallel diodes only.




(a) (b)

Figure 4.8 Simulated input-output waveforms of the proposed 3L-BTB converters under output frequency variation ($M$ = 0.86, $f_o$ = 25 Hz) (a) 3L-IMC (b) S3L-BTB converter

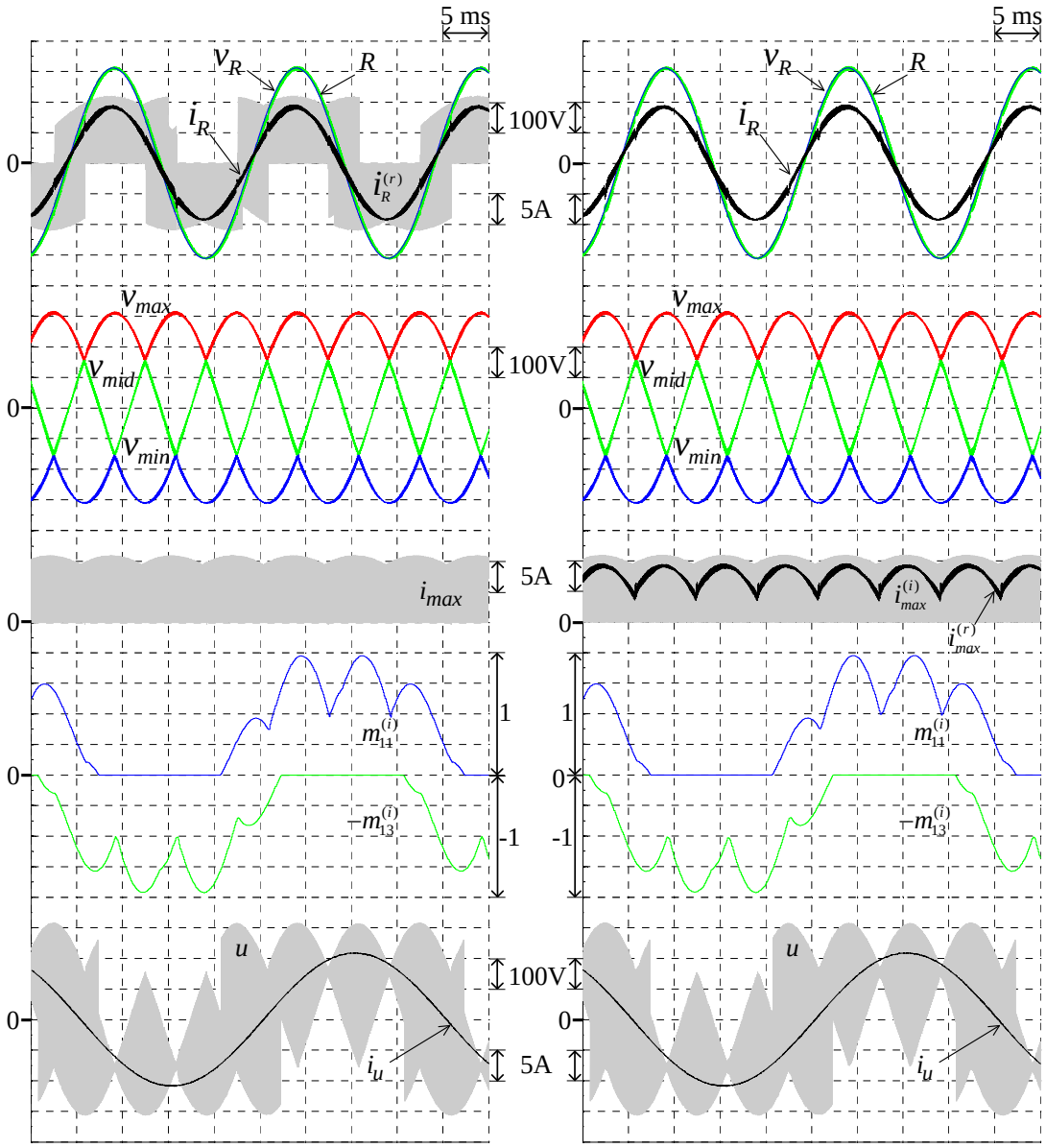



Figure 4.9 External and internal waveforms of the proposed 3L-BTB converters under output frequency variation ($M$ = 0.86, $f_o$ = 25 Hz) (a) 3L-IMC (b) S3L-BTB converter

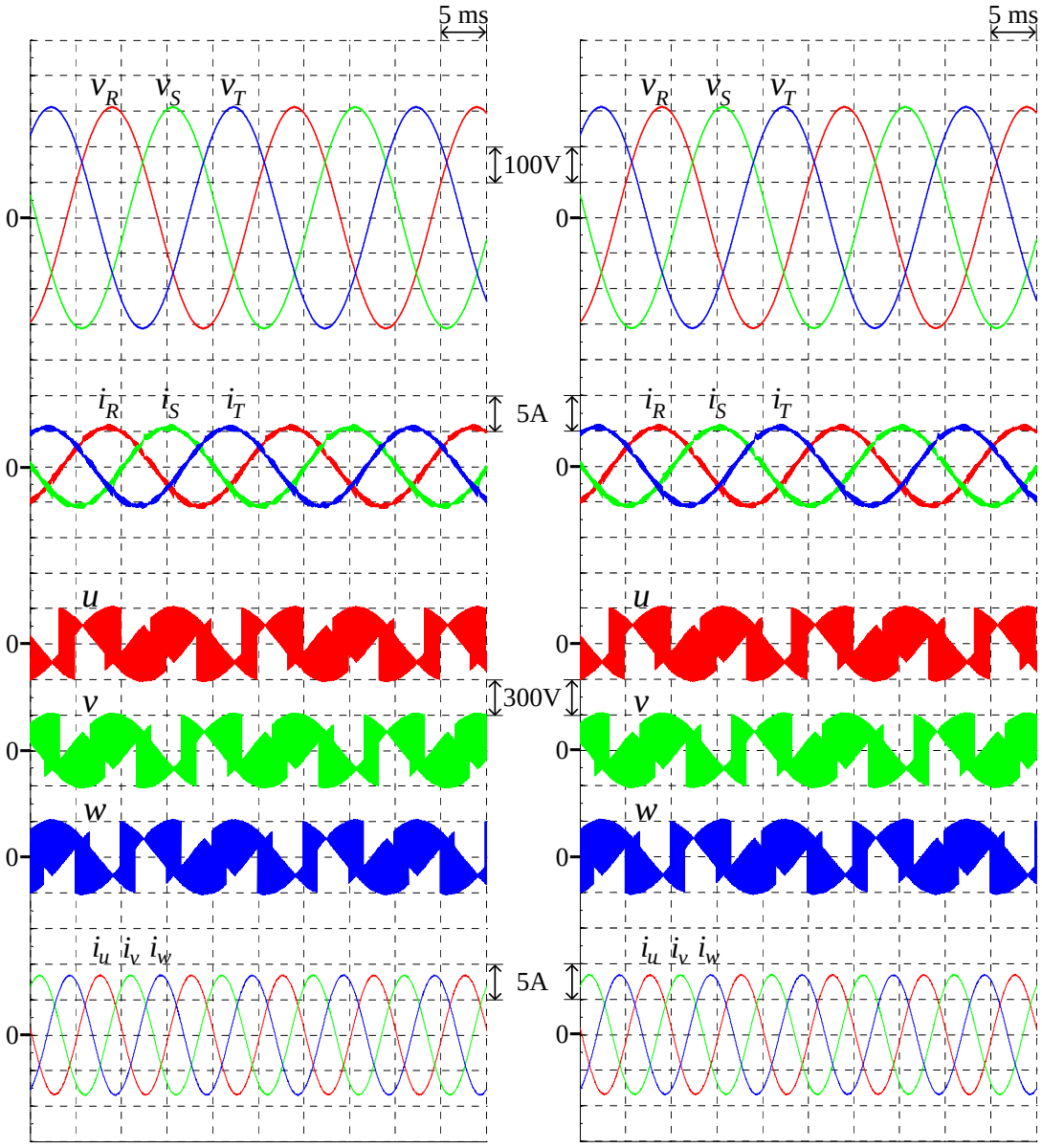



Figure 4.10 Simulated input-output waveforms of the proposed 3L-BTB converters under output frequency variation ($M$ = 0.86, $f_o$ = 100 Hz) (a) 3L-IMC (b) S3L-BTB converter

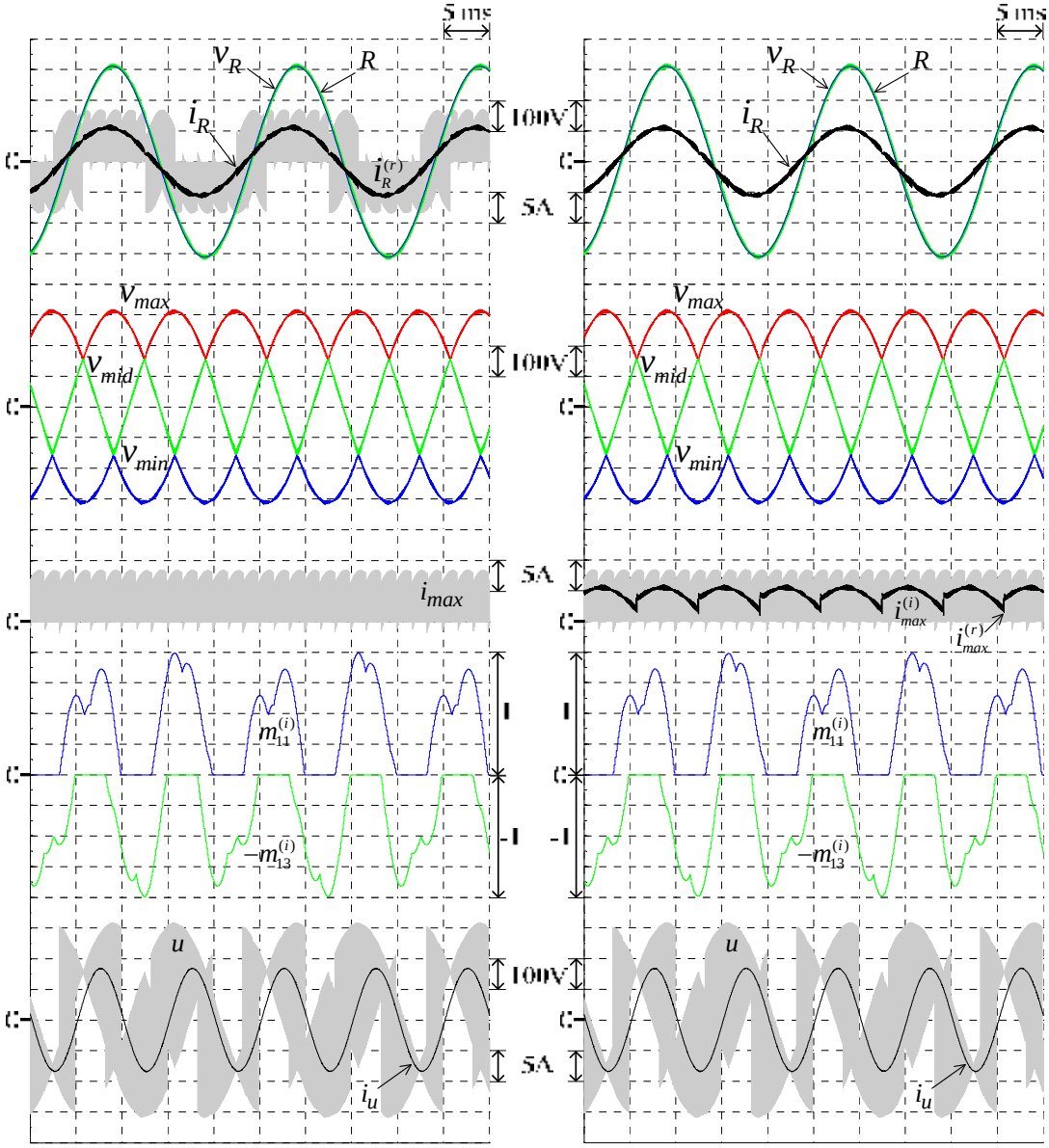


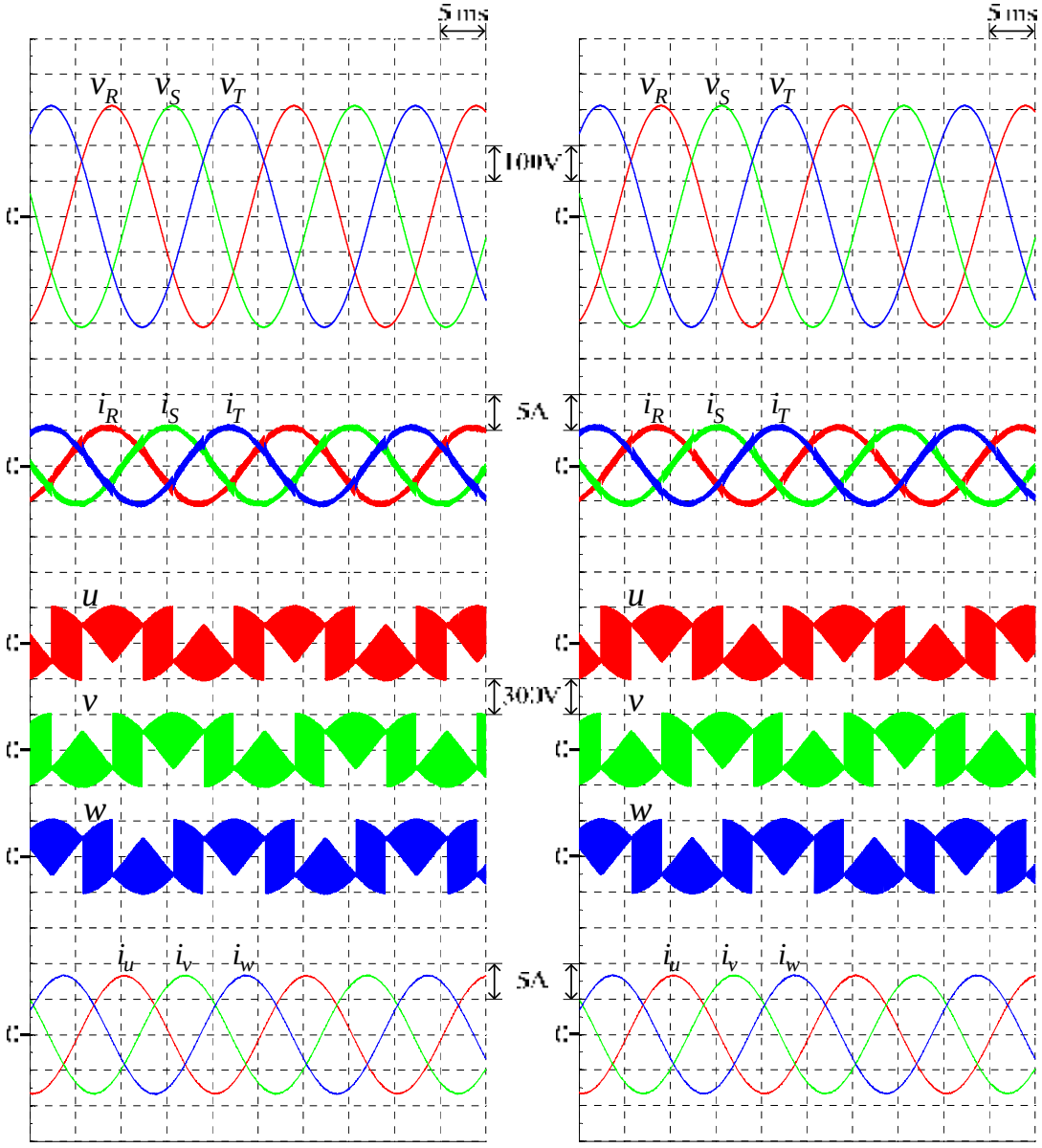

Figure 4.11 External and internal waveforms of the proposed 3L-BTB converters under output frequency variation ($M$ = 0.86, $f_o$ = 100 Hz) (a) 3L-IMC (b) S3L-BTB converter

## 4.4 Input Power Factor Compensation

The leading input power factor resulting from the reactive current of the capacitor network in the 3L-IMC and S3L-BTB converters can be compensated by adjusting the reactive component of the input current. This can be done by utilization of the free parameter '$k_1$' in the modulation matrix $\mathbf{M}_1'$ of (3.13) without affecting the required output voltage. Responses of the proposed converters with input power factor compensation are shown in Figure 4.14, 4.15 and 4.21. Besides unity power factor, a lagging or leading input power factor can also be achieved as demonstrated in Figure 4.16-4.19 and Figure 4.22-4.23, respectively. The results without input power factor compensation ($k_1 = 0$) are also displayed in Figure 4.12, Figure 4.13 and Figure 4.20 for comparison.

Under the given simulation conditions and circuit parameters, a unity input power factor is achieved with $k_1 = 5$ according to (3.37). There exist discontinuities in the modulation functions, $m_{11}^{(i)}$ and $-m_{13}^{(i)}$. This occurs at the transition of the input voltage sector which results from a sign change in the inverter modulation matrix of (3.11). The PWM pattern is then accordingly modified, and there is a phase shift occuring in the averaged dc-link currents in Figure 4.21 compared to the case without compensation in Figure 4.20. The output currents remain unchanged confirming that the averaged output voltages are unchanged by the compensation.

As an example, the case when $k_1$ is increased to obtain a lagging input power factor ($k_1 = 15$) is presented in Figure 4.16, Figure 4.17 and Figure 4.22. The drastic changes of modulation functions can be observed by the increased $k_1$ yielding higher negative pulse currents from inverter stage, $i_{max}$ and $i_{max}^{(i)}$. As a result, some distortions are found in the filtered dc-link current $i_{max}^{(r)}$ and consequentially in the input current $i_R$ in the vicinity of the discontinuities. Alternatively, $k_1$ can become negative to cause the supply currents to be more leading as shown in Figure 4.18, 4.19 and 4.23 for $k_1 = -3.3$.




(a) (b)

Figure 4.12 Simulated input-output waveforms of the proposed 3L-BTB converters without input power factor compensation ($M$ = 0.7, $f_o$ = 50 Hz, $k_1 = 0$ ) (a) 3L-IMC (b) S3L-BTB converter

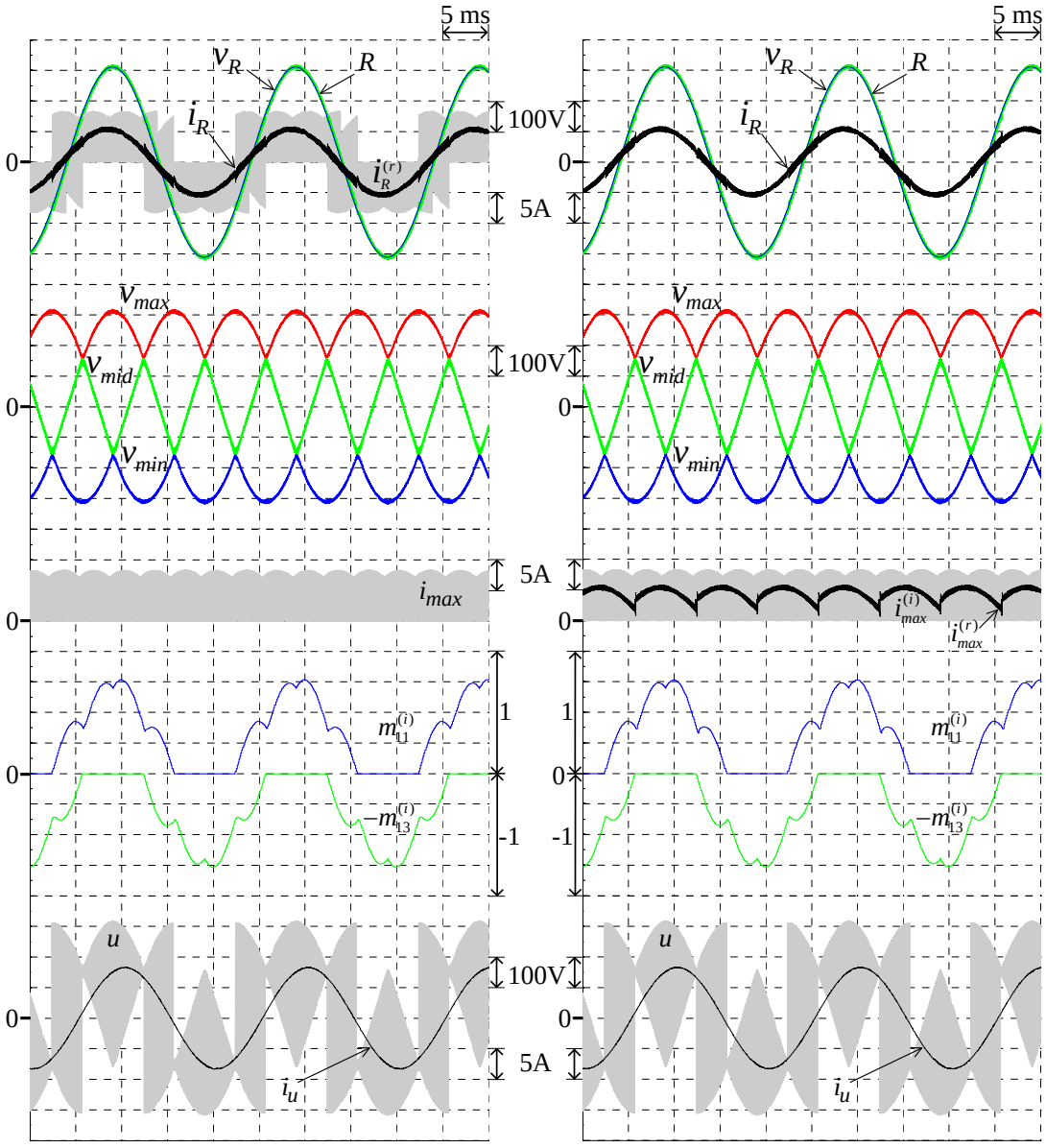
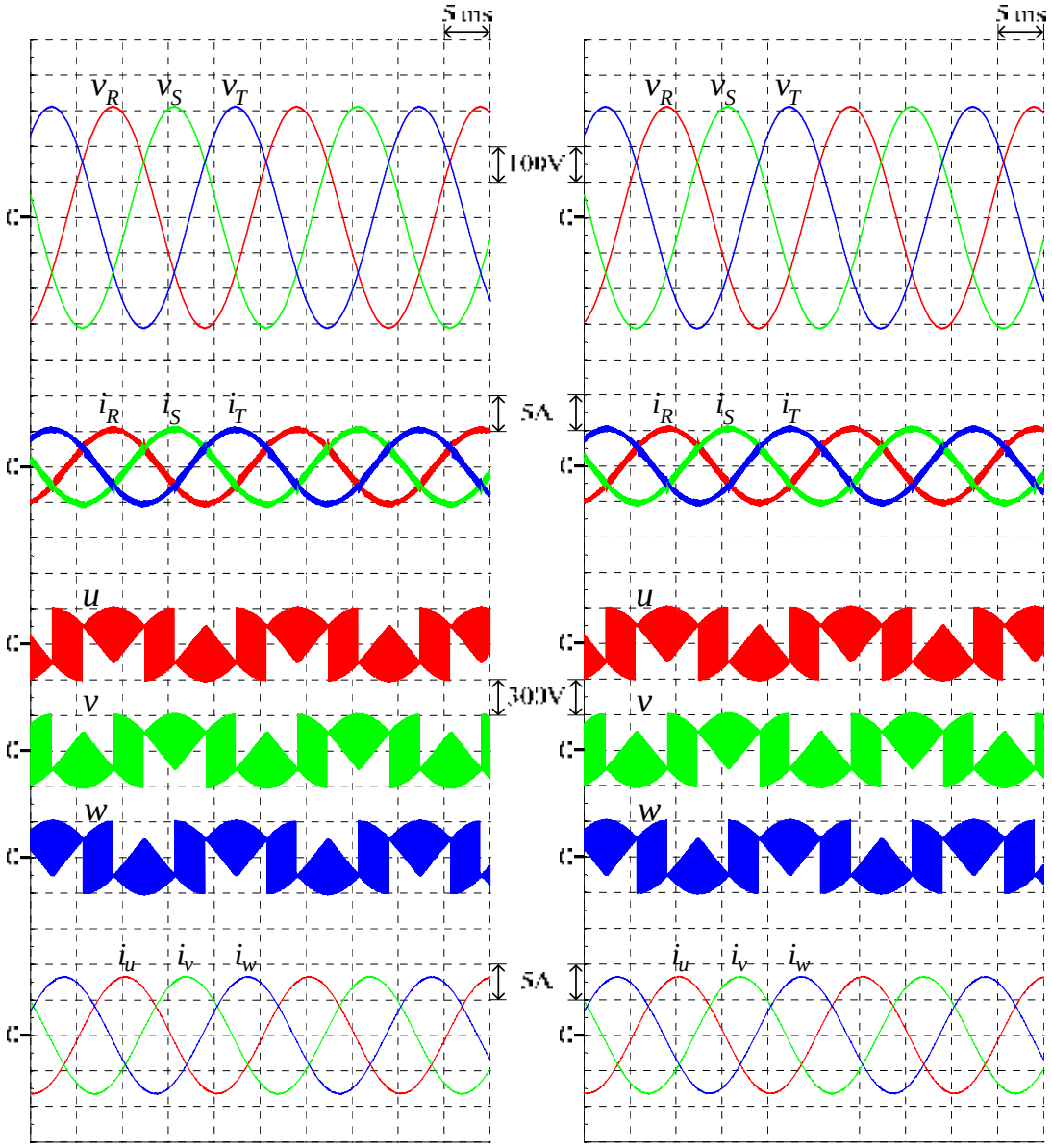



Figure 4.13 External and internal waveforms of the proposed 3L-BTB converters without input power factor compensation ($M$ = 0.7, $f_o$ = 50 Hz, $k_1 = 0$ ) (a) 3L-IMC (b) S3L-BTB converter




(a) (b)

Figure 4.14 Simulated input-output waveforms of the proposed 3L-BTB converters with unity input power factor ($M$ = 0.7, $f_o$ = 50 Hz, $k_1 = 5$) (a) 3L-IMC (b) S3L-BTB converter

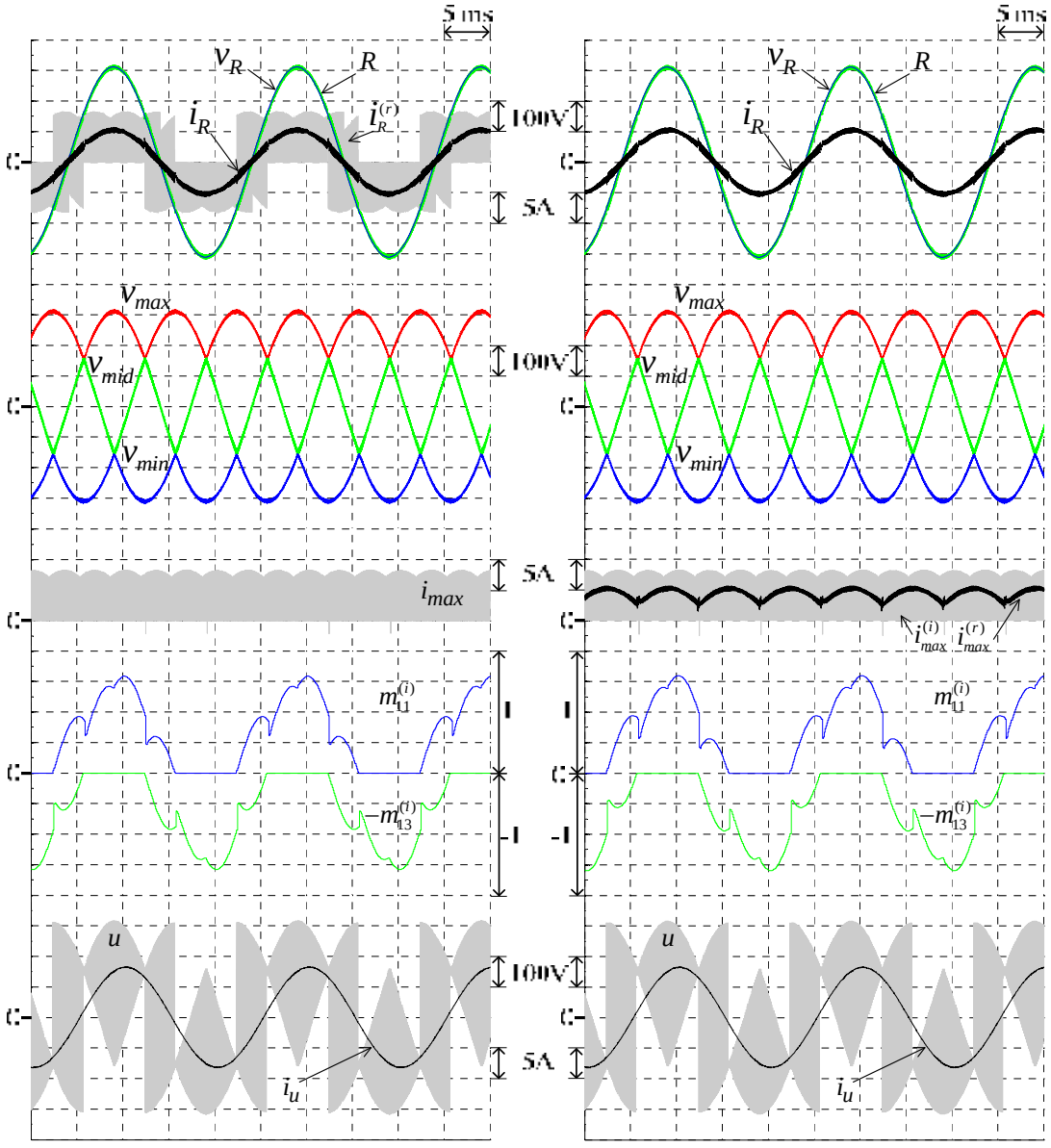
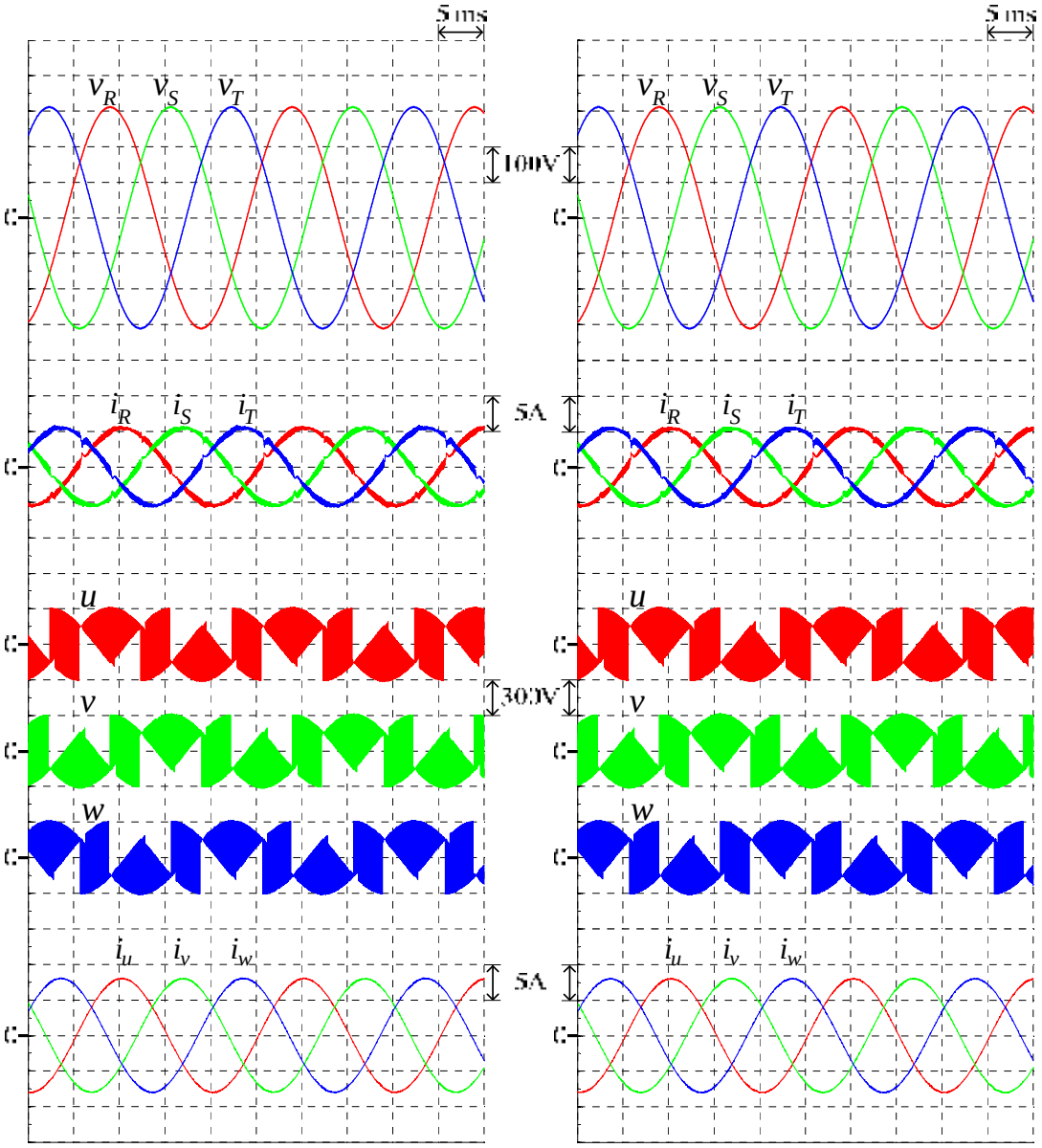



Figure 4.15 External and internal waveforms of the proposed 3L-BTB converters with unity input power factor ($M$ = 0.7, $f_o$ = 50 Hz, $k_1 = 5$) (a) 3L-IMC (b) S3L-BTB converter




(a) (b)

Figure 4.16 Simulated input-output waveforms of the proposed 3L-BTB converters with lagging input power factor ($M$ = 0.7, $f_o$ = 50 Hz, $k_1$ = 15) (a) 3L-IMC (b) S3L-BTB converter

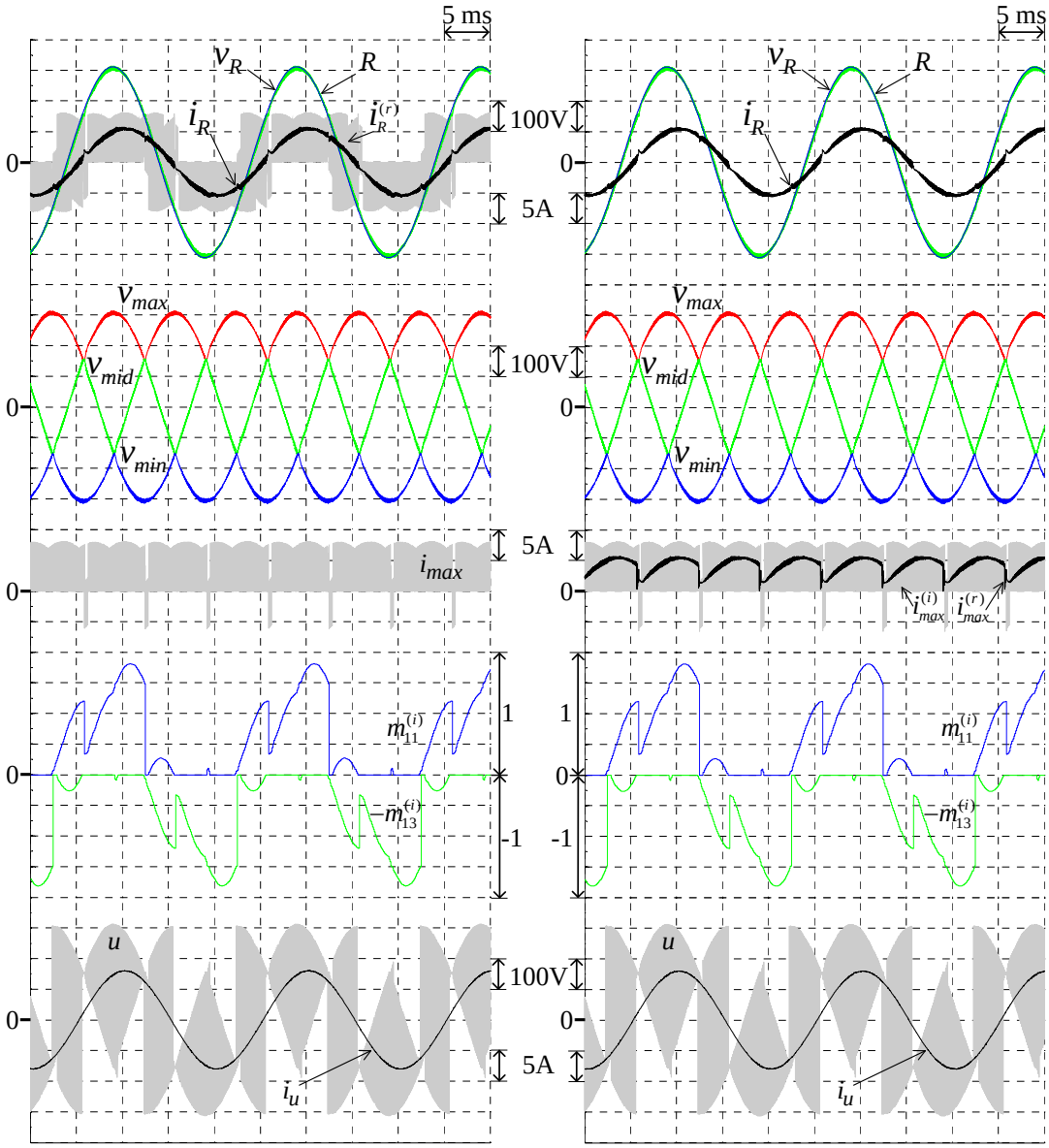
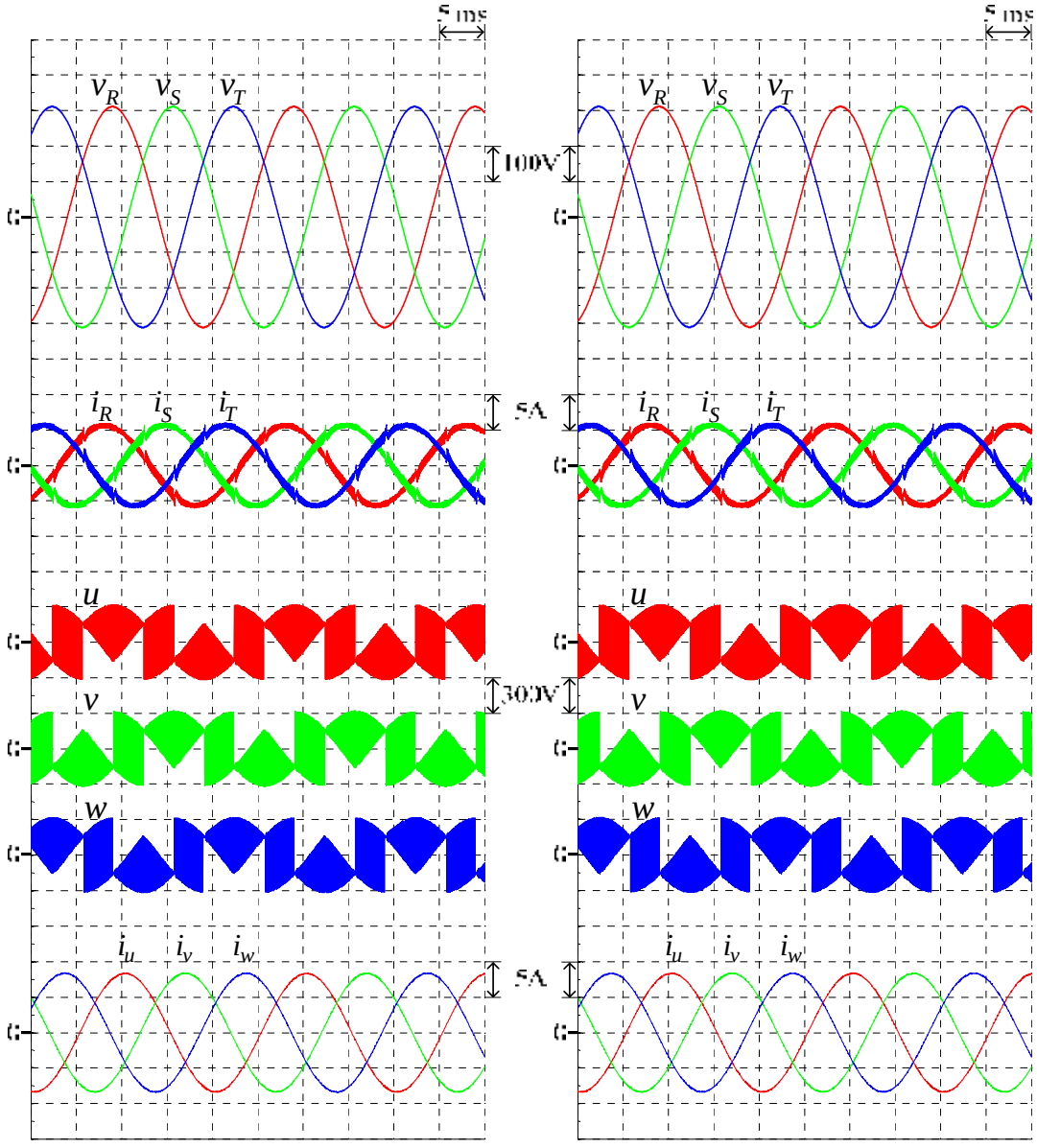



Figure 4.17 External and internal waveforms of the proposed 3L-BTB converters with lagging input power factor ($M$ = 0.7, $f_o$ = 50 Hz, $k_1$ = 15) (a) 3L-IMC (b) S3L-BTB converter




(a) (b)

Figure 4.18 Simulated input-output waveforms of the proposed 3L-BTB converters with leading input power factor ($M$ = 0.7, $f_o$ = 50 Hz, $k_1 = -3.3$ ) (a) 3L-IMC (b) S3L-BTB converter

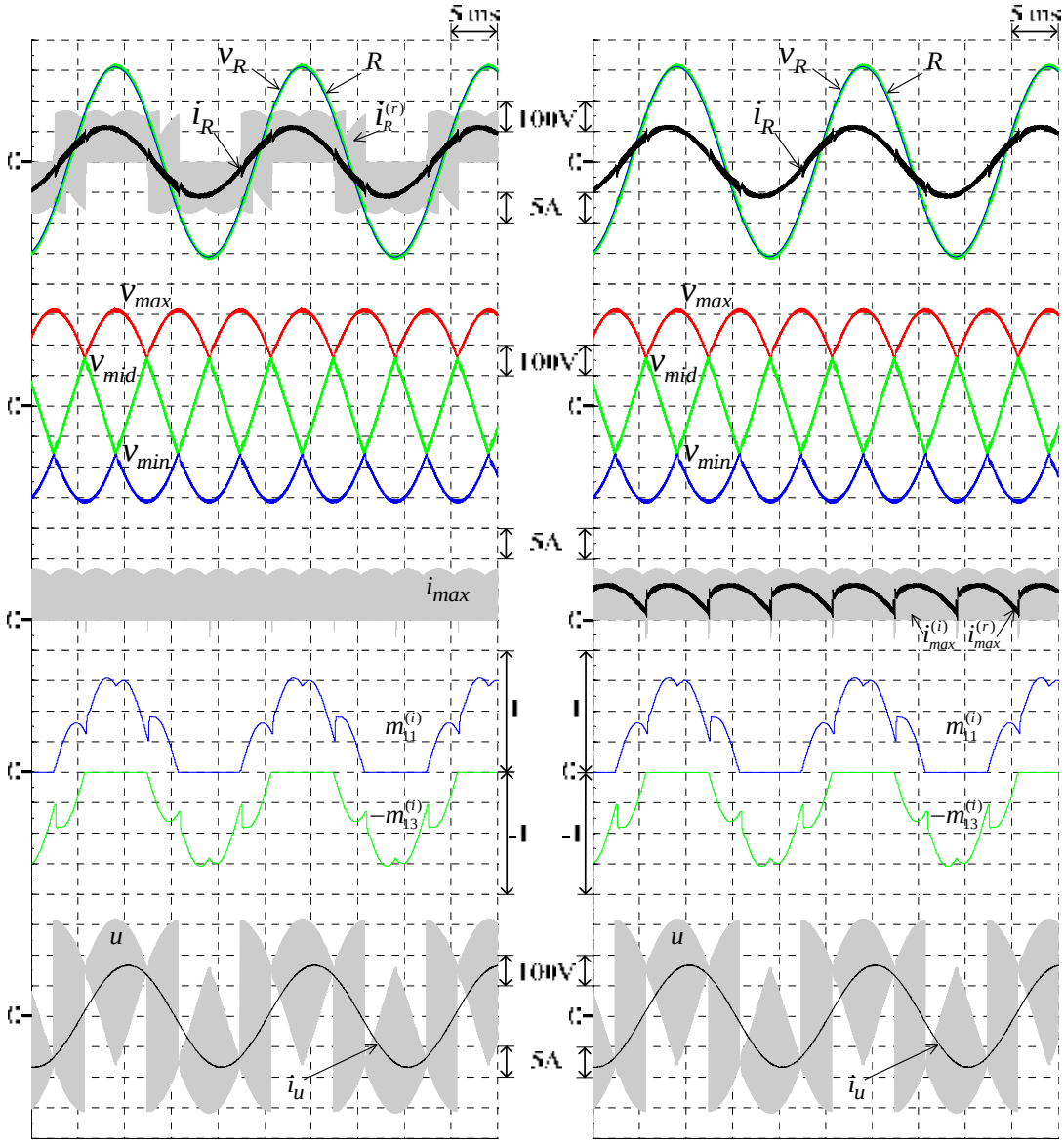



Figure 4.19 External and internal waveforms of the proposed 3L-BTB converters with leading input power factor ($M$ = 0.7, $f_o$ = 50 Hz, $k_1 = -3.3$) (a) 3L-IMC (b) S3L-BTB converter

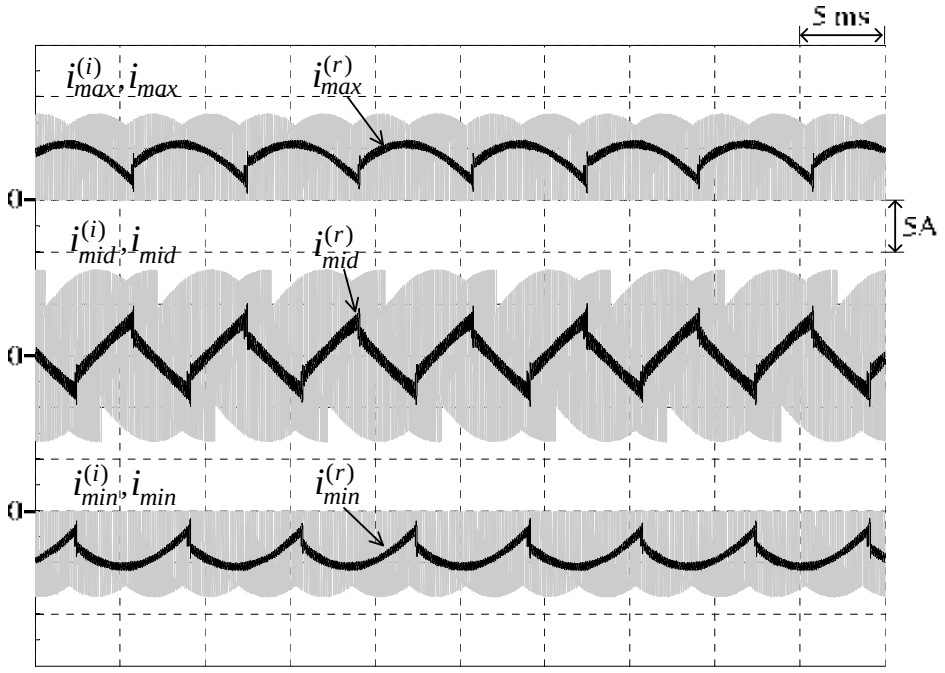



Figure 4.20 Simulated dc-link currents of the proposed 3L-BTB converters without input power factor compensation under condition ($M$ = 0.7, $f_o$ = 50 Hz, $k_1 = 0$ )

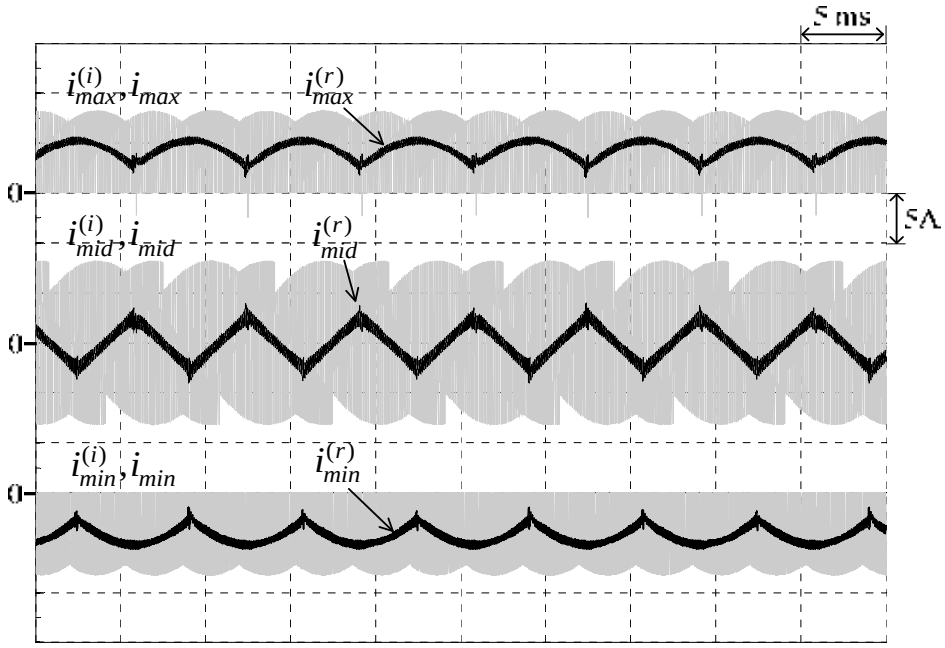



Figure 4.21 Simulated dc-link currents of the proposed 3L-BTB converters with unity input power factor under condition ($M$ = 0.7, $f_o$ = 50 Hz, $k_1 = 5$)

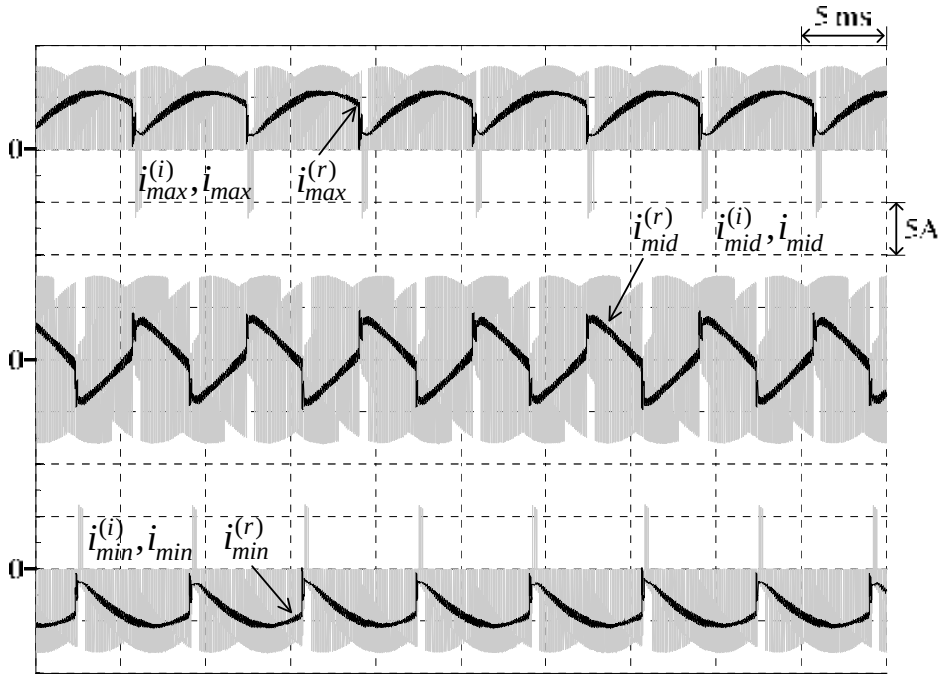



Figure 4.22 Simulated dc-link currents of the proposed 3L-BTB converters with lagging input power factor under condition ($M$ = 0.7, $f_o$ = 50 Hz, $k_1 = 15$)

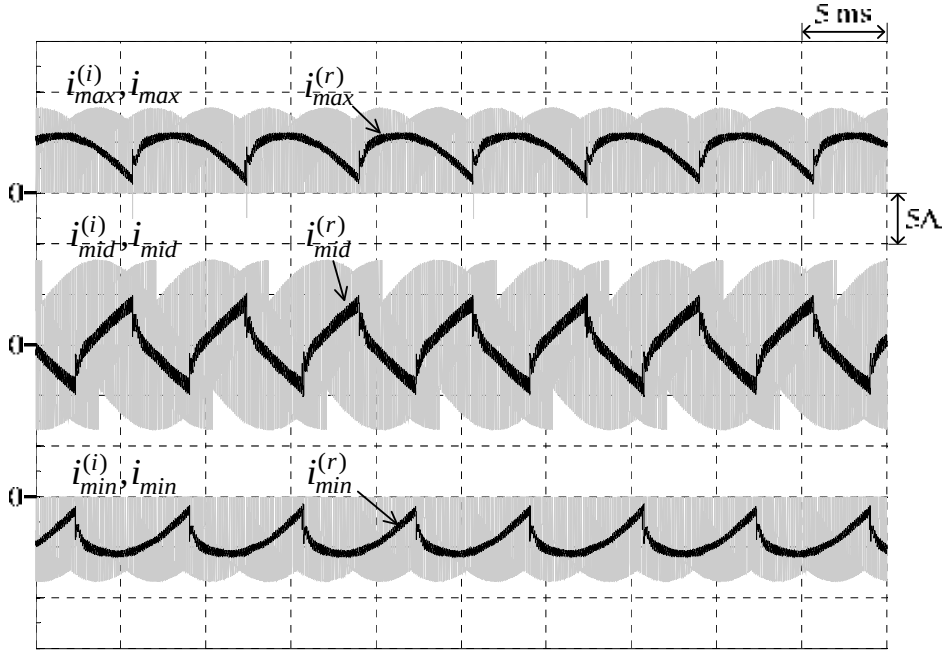
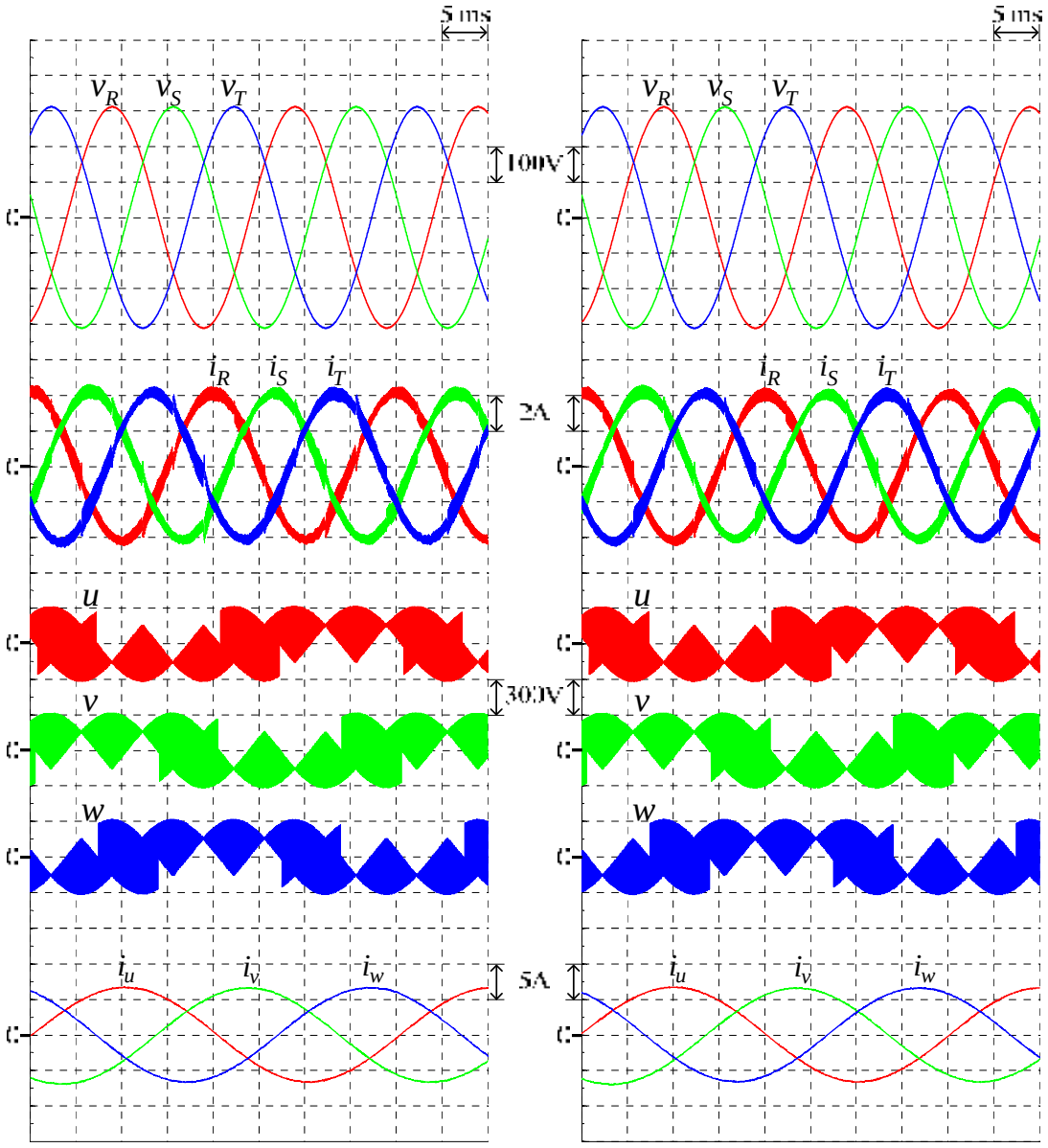



Figure 4.23 Simulated dc-link currents of the proposed 3L-BTB converters with leading input power factor under condition ($M$ = 0.7, $f_o$ = 50 Hz, $k_1 = -3.3$)

## 4.5 **Regenerative Operation**

Figure 4.24, 4.25 and 4.28 are the system responses when the proposed 3L-BTB converters operate under regenerative mode ($M$ = 0.7, $f_o$ = 25 Hz, $k_1 = 0$ ). It is evident in Figure 4.28 that the dc-link currents now flow in the opposite direction compared to those operating under non-regenerative mode as discussed so far.

Furthermore, power factor compensation can also be done correctly under regenerative mode as demonstrated in Figure 4.26, 4.27 and 4.29 ($M$ = 0.7, $f_o$ = 25 Hz, $k_1 = 12$ ). Although the dc-link currents resulting from the inverter stage at the 'min' link, $i_{min}$ and $i_{min}^{(i)}$ in Figure 4.29 become bi-directional (unlike those in Figure 4.28), the filtered current $i_{min}^{(r)}$ in the S3L-BTB converter still flows in one direction. The unidirectional flow of the filtered dc-link current, $i_{max}^{(r)}$ and $i_{min}^{(r)}$, suggests for further improvement to reduce the number of semiconductor devices in some applications.




(a) (b)

Figure 4.24 Simulated input-output waveforms of the proposed 3L-BTB converters operating under regenerative mode ($M$ = 0.7, $f_o$ = 25 Hz, $k_1 = 0$ ) (a) 3L-IMC (b) S3L-BTB converter

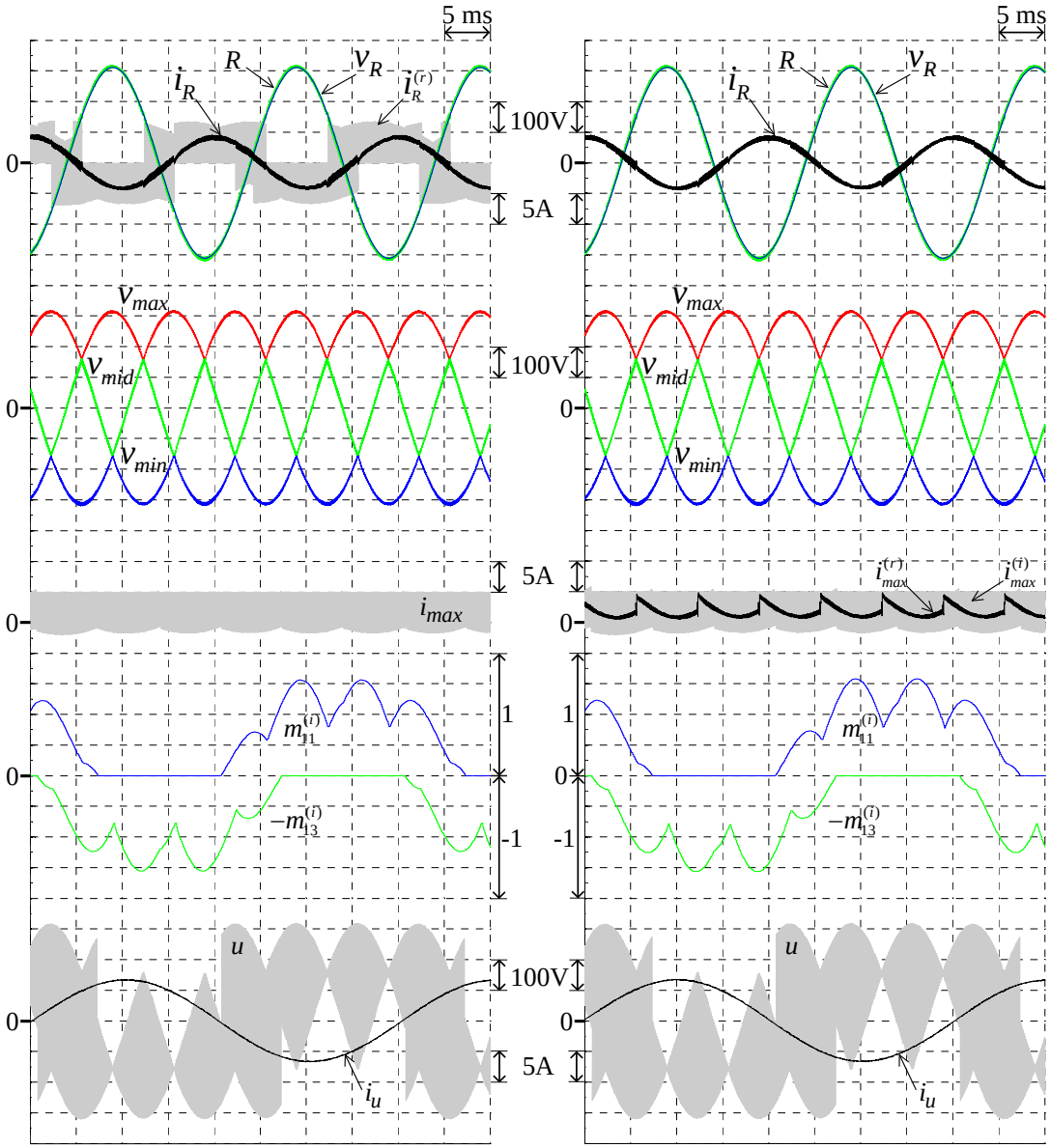



Figure 4.25 External and internal waveforms of the proposed 3L-BTB converters operating under regenerative mode ($M$ = 0.7, $f_o$ = 25 Hz, $k_1 = 0$ ) (a) 3L-IMC (b) S3L-BTB converter

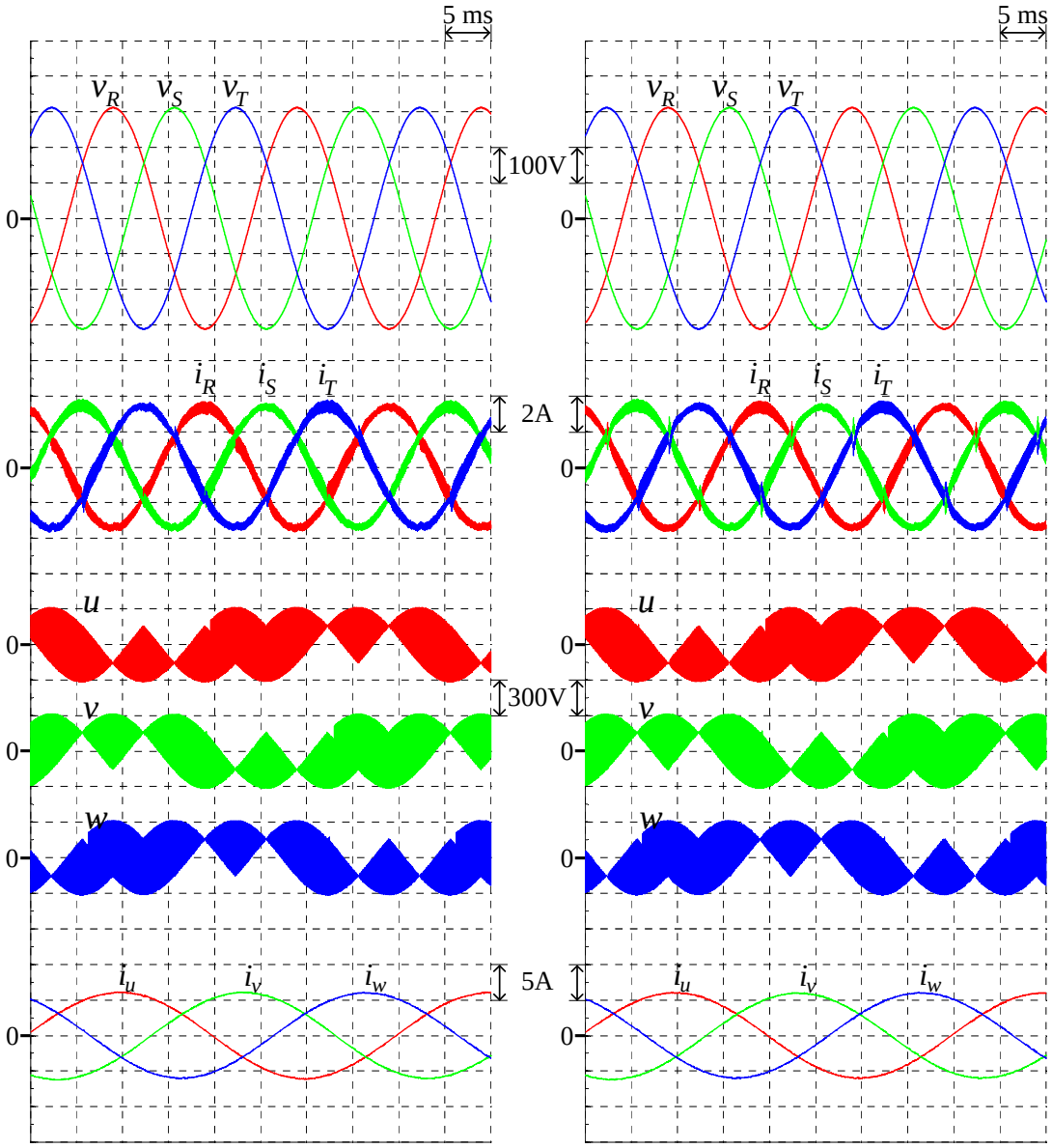
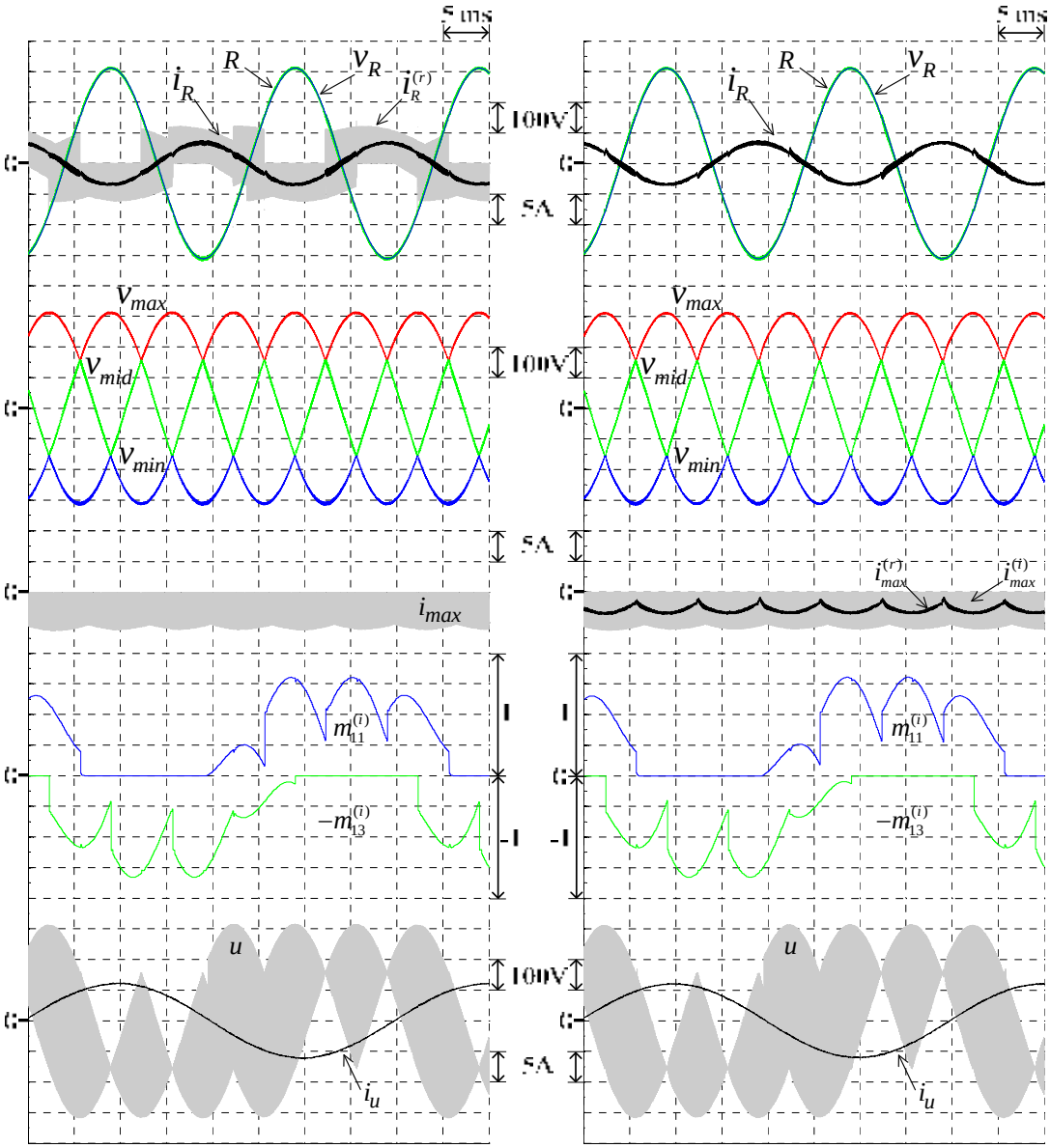



Figure 4.26 Simulated input-output waveforms of the proposed 3L-BTB converters operating at unity input power factor under regenerative mode ($M$ = 0.7, $f_o$ = 25 Hz, $k_1 = 12$ ) (a) 3L-IMC (b) S3L-BTB converter




(a) (b)

Figure 4.27 External and internal waveforms of the proposed 3L-BTB converters operating at unity input power factor under regenerative mode ($M$ = 0.7, $f_o$ = 25 Hz, $k_1 = 12$ ) (a) 3L-IMC (b) S3L-BTB converter

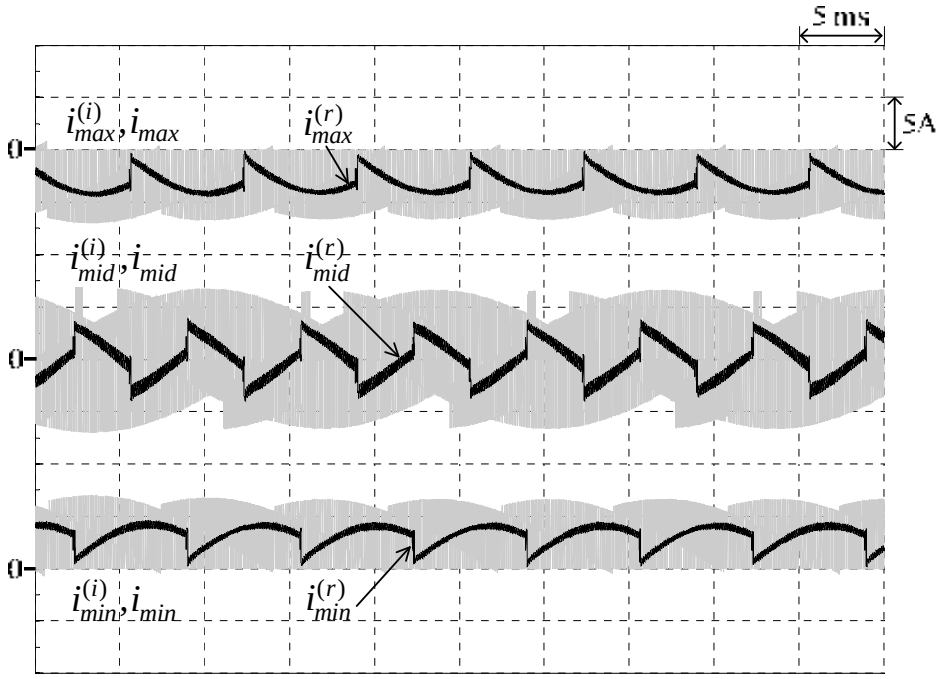



Figure 4.28 Simulated dc-link currents of the proposed 3L-BTB converters operating under regenerative mode at ($M$ = 0.7, $f_o$ = 25 Hz, $k_1 = 0$ )

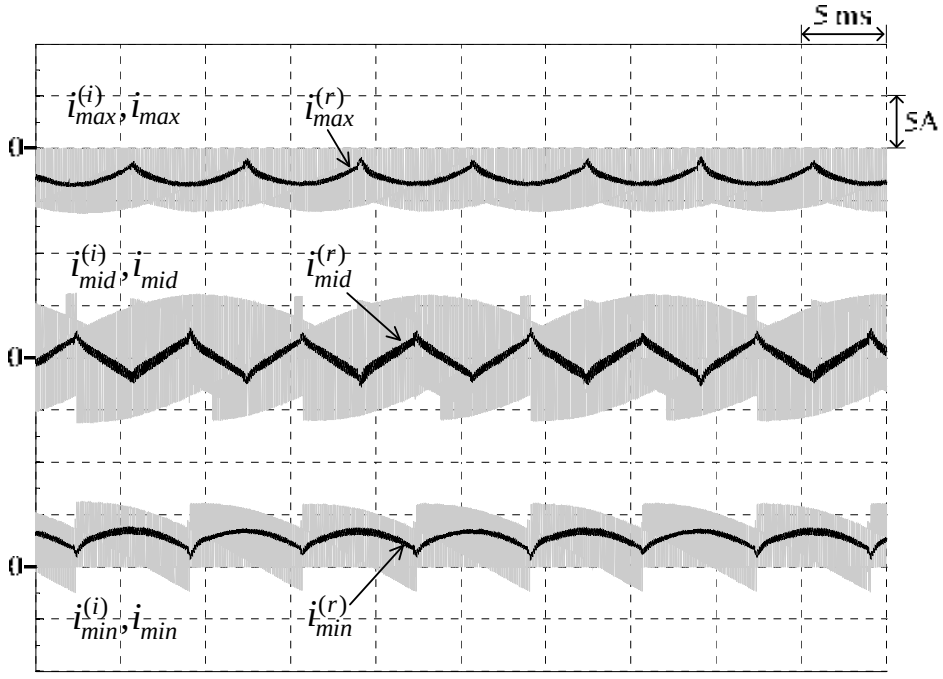



Figure 4.29 Simulated dc-link currents of the proposed 3L-BTB converters operating at unity input power factor under regenerative mode at ($M$ = 0.7, $f_o$ = 25 Hz, $k_1 = 12$ )

## 4.6 Semiconductor Losses Comparison between the S3L-BTB Converter and the Conventional 3L-BTB converter.

To exemplify the benefit of the proposed converters in switching loss reduction compared to its conventional counterpart, numerical evaluation for semiconductor losses of the S3L-BTB converter is conducted based on the simplified semiconductor loss model in [15] and [16], and with the parameters of a commercial 3L-NPC structure module SKM20ML1066. The losses evaluation for each converter is calculated at the operating conditions 4 and 11 of Table 4.1. The mean losses over a fundamental period for each semiconductor devices in Figure 4.30 also are determined and compared in Figure 4.31and 4.32. The losses in each device are displayed in a pair of bar graphs, where the left-most and the right-most bars represent the losses of the S3L-BTB and the conventional 3L-BTB converters. (The loss parameters of the SKM20ML1066 and the details of calculation approach are given in Appendix)

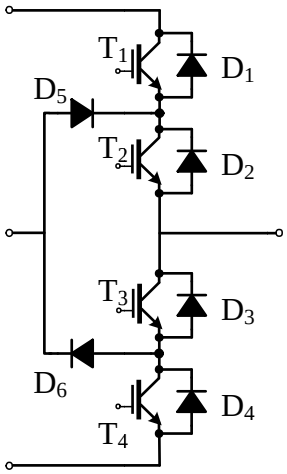



Figure 4.30 A three-level neutral-point-clamped structure used in loss evaluation

### 4.6.1 Non-Regenerative Mode

Table 4.2 summarizes the semiconductor losses in each stage of the converters working under non-regenerative mode at the operating condition 4 ($M$ =0.86, $f_o$ = 25 Hz). It is obvious that the switching losses in the rectifier stage are significantly reduced to zero due to the fundamental-frequency switching operation. The only devices contribute to switching losses according to Figure 4.31(a) are

IGBTs, $T_2$ and $T_3$, whereas the others do not because they switches at the instant the input voltage sector changes, meaning that the voltage across the switches are zero. Moreover, although both the S3L-BTB and the conventional 3L-BTB converters employ PWM technique for the inverter operation, the switching losses in the inverter stage of the former one is less for the reason that the max-mid-min dc-link voltages are lower than those of the conventional one. The whole loss reduction contributes to the improvement of efficiency from 95.7% to 97%.

The conduction losses are comparable for the S3L-BTB and the conventional converters both at the rectifier and inverter stages. It can be seen that conduction losses occurring at $T_1$ and $T_4$ in the rectifier stage of the S3L-BTB converter are zero. This is because the dc-link currents $i_{max}^{(r)}$ and $i_{min}^{(r)}$ in Figure 4.9 are unidirectional and flow only through anti-parallel diodes $D_1$ and $D_4$; the IGBTs, $T_1$ and $T_4$, can thus switch under zero voltage without significant losses at that moment.

Table 4.2 Comparison of the mean semiconductor losses between S3L-BTB and conventional 3L-BTB converters operating under non-regenerative mode at condition ($M$ = 0.86, $f_o$ = 25 Hz)

| **Stage** | **Losses** | **S3L-BTB converter (Watt)** | | **Conventional 3L-BTB converter (Watt)** | |
|---|---|---|---|---|---|
| Rectifier | Conduction Losses | 54.28 | 54.32 | 52.18 | 91.29 |
| | Switching Losses | 0.039 | | 39.11 | |
| Inverter | Conduction Losses | 41.47 | 75.89 | 43.49 | 90.35 |
| | Switching Losses | 34.42 | | 46.86 | |
| Total Losses | | 130.21 | | 181.64 | |
| Efficiency | | 97% | | 95.7% | |

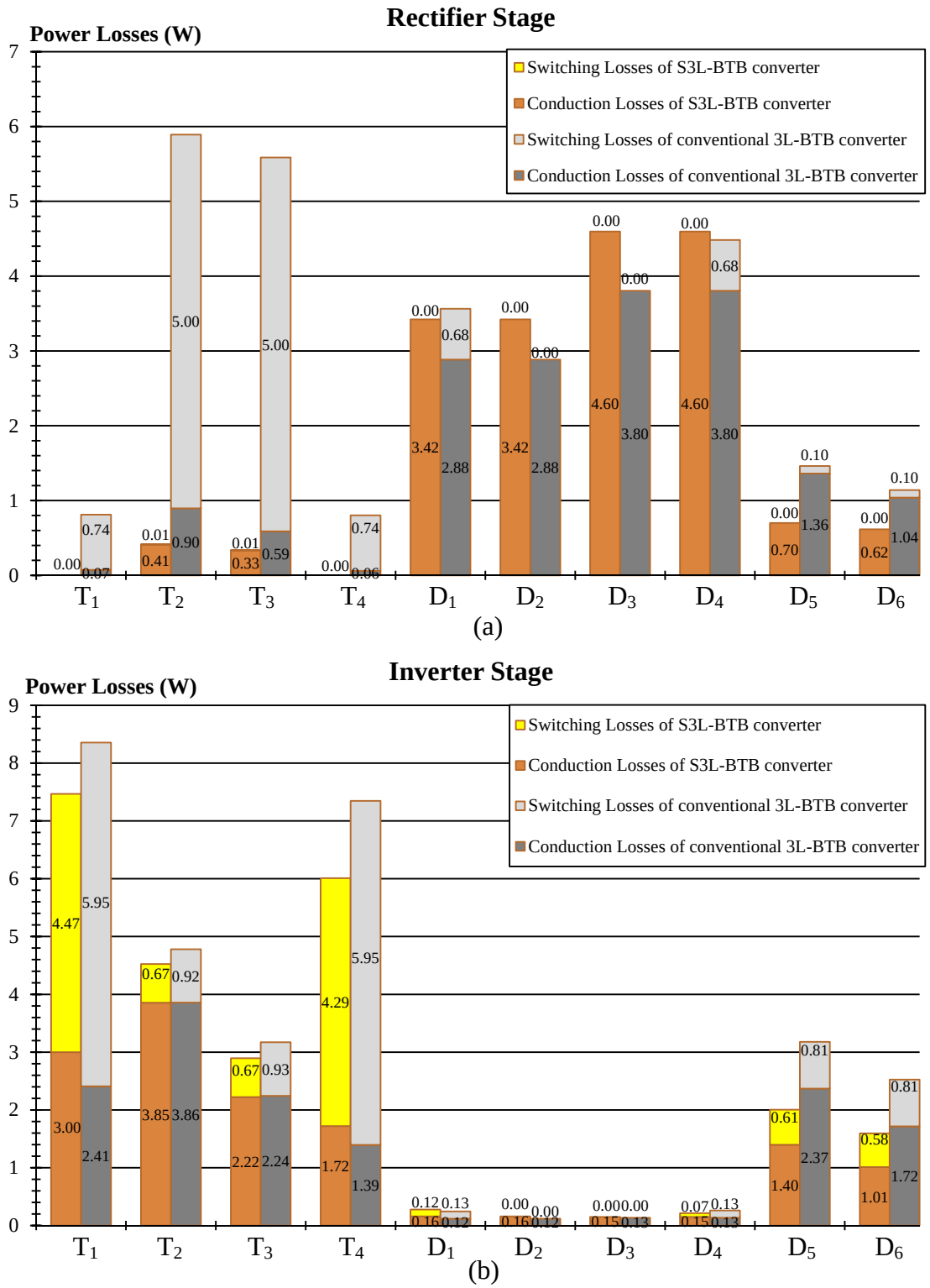



Figure 4.31 Comparison of the mean semiconductor losses between S3L-BTB and conventional 3L-BTB converters operating under condition ($M$ = 0.86, $f_o$ = 25 Hz) (a) rectifier stage (b) inverter stage

### 4.6.2 Regenerative Mode

The semiconductor losses of the S3L-BTB converter are compared with those of the conventional 3L-BTB converter working at input unity power factor under regenerative mode in Table 4.3. The results are in good agreement with those of Table 4.2. Since the input currents are in phase with the input voltage, the IGBTs, $T_2$ and $T_3$, in the rectifier stage of the S3L-BTB converter now change their states nearly under zero voltage switching at the same time as the input voltages change their sector. As a result, the switching losses in all of the devices in the rectifier stage are practically diminished to zero in this condition as depicted in Figure 4.32(a). Apart from the dramatic drop in the rectifier stage losses, the same reduction in the switching losses in the inverter stage can also be noticed. This leads to 96.9% in efficiency compared to 95.8% of the conventional one.

The conduction losses in both converters are comparable. In contrast to the non-generative mode case, the dc-link currents $i_{max}^{(r)}$ and $i_{min}^{(r)}$ in the S3L-BTB converter in Figure 4.29 now flow in the opposite direction of Figure 4.9 through the IGBTs. Therefore, the conduction losses in the rectifier stage distribute unevenly to the IGBTs, and the conduction losses in the anti-parallel diodes become zero.

Table 4.3 Comparison of the mean semiconductor losses between S3L-BTB and conventional 3L-BTB converters operating under regenerative mode at condition ($M$ = 0.7, $f_o$ = 25 Hz)

| **Stage** | **Losses** | **S3L-BTB converter (Watt)** | | **Conventional 3L-BTB converter (Watt)** | |
|---|---|---|---|---|---|
| Rectifier | Conduction Losses | 11.59 | 11.59 | 12.29 | 27.18 |
| | Switching Losses | 0 | | 14.89 | |
| Inverter | Conduction Losses | 32.84 | 53.54 | 32.02 | 60.24 |
| | Switching Losses | 20.70 | | 28.22 | |
| Total Losses | | 65.13 | | 87.32 | |
| Efficiency | | 96.9% | | 95.8% | |

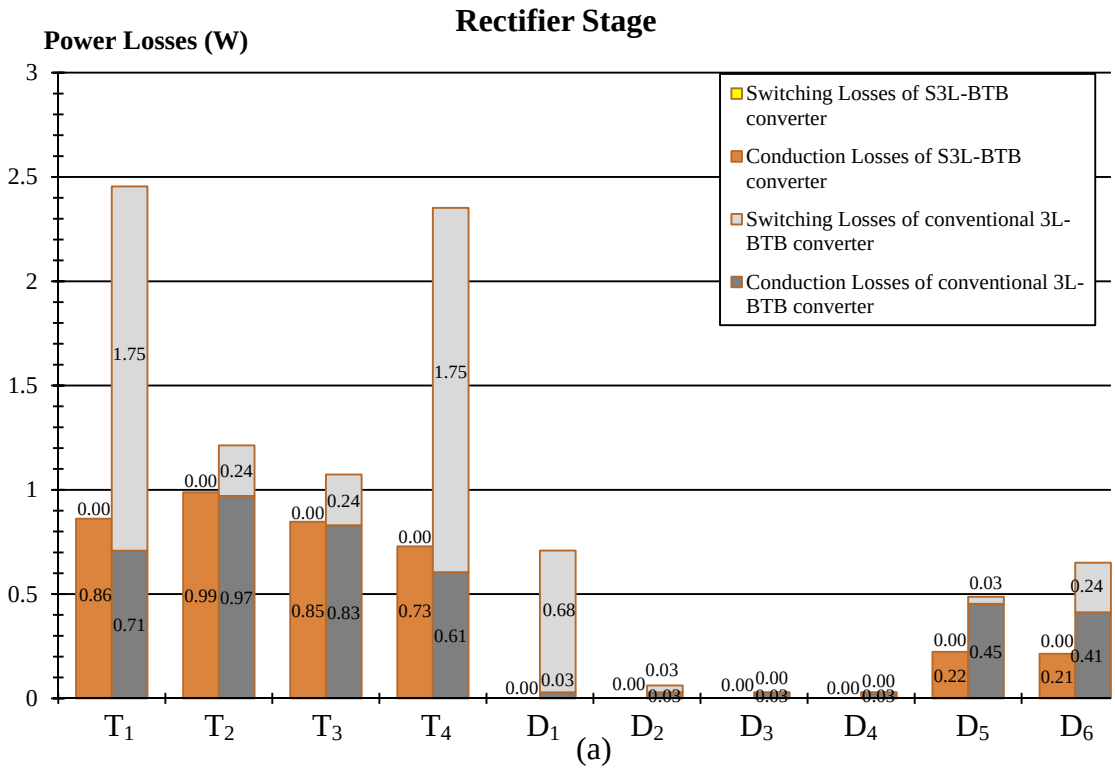



Figure 4.32 Comparison of the mean semiconductor losses between S3L-BTB and conventional 3L-BTB converters operating at unity input power factor under regenerative mode at condition ($M$ = 0.7, $f_o$ = 25 Hz) (a) rectifier stage (b) inverter stage

In conclusion, the proper operation and the performances of the proposed novel topologies, 3L-IMC and S3L-BTB converters, are simulated and confirmed. They operate the three-level front-end rectifier at fundamental-frequency switching (non-PWM), and operate the three-level back-end inverter stage with PWM technique. Their capabilities to i) vary the output voltages and output frequency, ii) to obtain the sinusoidal supply currents together with adjustable input power factor, and iii) to work under regenerative mode are all verified. Also, the benefits of the S3L-BTB converter in losses reduction at the rectifier stage are numerically evaluated.

# CHAPTER V
# IMPLEMENTATION AND EXPERIMENTAL RESULTS

Since the performances of the proposed 3L-BTB converters have been confirmed successfully by simulation in Chapter IV, in this Chapter a laboratory prototype of the S3L-BTB converter will be constructed and tested in order to verify the performances in real implementation. Compared to the 3L-IMC, the S3L-BTB converter is preferable because it is easy to be implemented without constraints on commutation timing between the rectifier and inverter, and is more practical due to the close similarity to the conventional 3L-BTB converter. The constructed prototype is digitally controlled by a single Field Programmable Gate Array (FPGA). The targeted specifications of the prototype are:

Apparent power rating: 5 kVA

Source voltages: balanced three-phase line-to-line voltage 380 $V_{rms}$ 50 Hz

Inverter switching frequency: 12.2 kHz

## 5.1 Hardware Design

From Figure 5.1, the hardware of the prototype system can be divided into high-power circuits and measurement circuits.

### 5.1.1 High-Power Circuits

#### 5.1.1.1 Voltage Stresses on Devices

One important factor that must be taken into account when selecting power devices is the voltage stresses. In back-to-back converters, the voltage stresses can be determined directly from the dc-link voltages. However, the dc-link voltages of the S3L-BTB converter are not constant as usually found in the conventional back-to-back converters. The peak of the dc-link voltages of the S3L-BTB converter are firstly determined and used as a guideline for selecting suitable power devices.

According to Figure 5.2, the upper or lower half of the dc-link voltage has its peak at the transition of the input voltage sector with the value given in (5.1). In

addition, the peak voltage between the ‘max’ and ‘min’ links is equal to the peak of the line-to-line input voltage shown in (5.2).

$$\left(v_{max} - v_{mid}\right)_{peak} = \left(v_{mid} - v_{min}\right)_{peak} = \sqrt{\frac{3}{2}} V_i \tag{5.1}$$

$$\left(v_{max} - v_{min}\right)_{peak} = \sqrt{2} V_i \tag{5.2}$$

Here $V_i$ is the RMS value of the input line-to-line voltage.

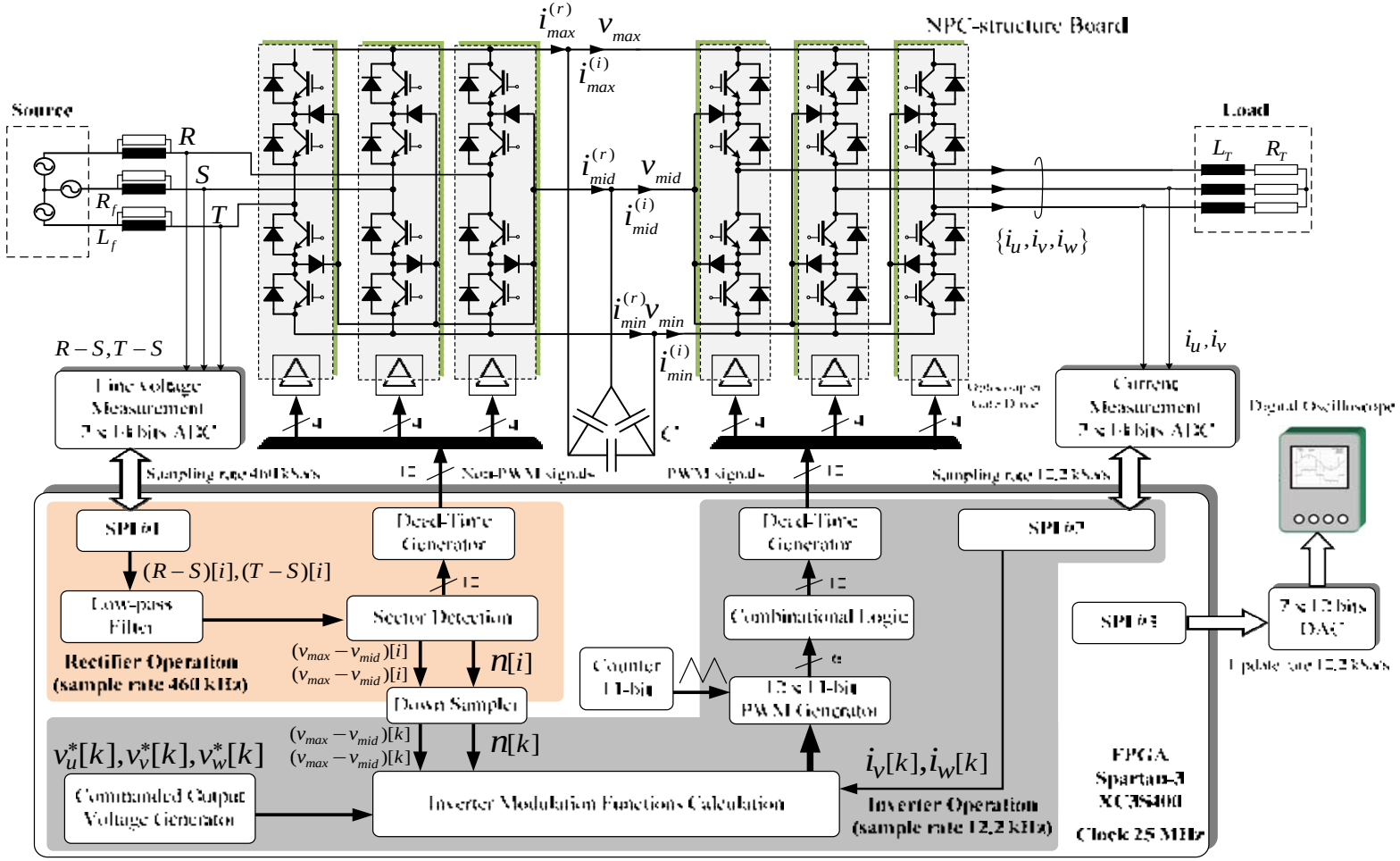



Figure 5.1 Schematic of laboratory prototype including functional diagram of the controller implemented on a FPGA.

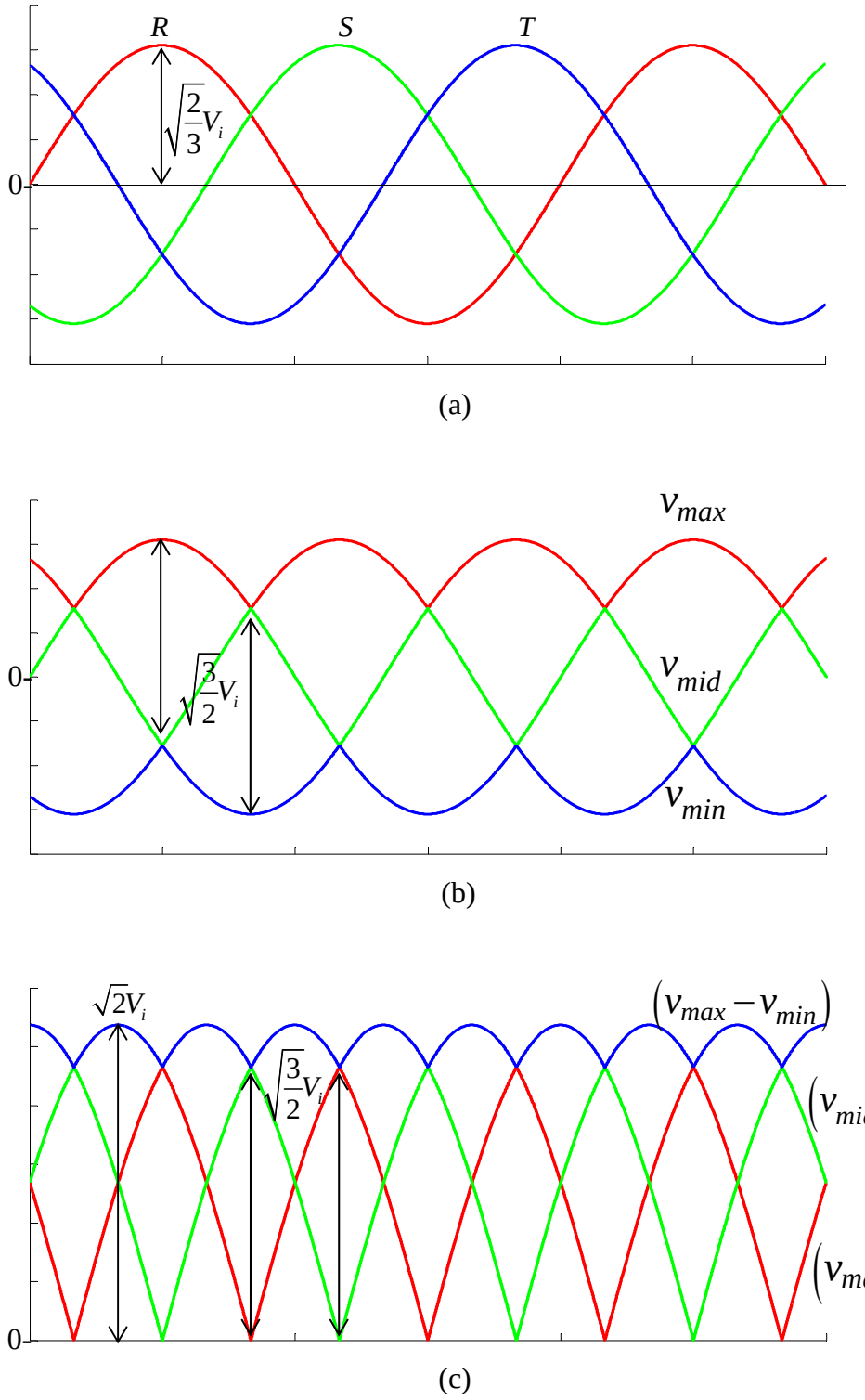



Figure 5.2 Voltages in S3L-BTB converters displayed with their peaks value (a) input voltages (b) dc-link bus voltages (c) dc-link line-to-line voltages.

With the 380-$V_{rms}$ (line-to-line) sinusoidal supply voltage used in the experiment, the input line voltage at the rectifier terminals will then be approximately equal to 380 V, or $V_i \approx 380$ V. Therefore,

$$\left(v_{max} - v_{mid}\right)_{peak} = \left(v_{mid} - v_{min}\right)_{peak} \approx 467 \text{ V} \tag{5.3}$$

$$\left(v_{max} - v_{min}\right)_{peak} \approx 540 \text{ V} \tag{5.4}$$

#### 5.1.1.2 **NPC Structure**

The three-level NPC structures used in the experiment are assembled from discrete semiconductor devices. The printed circuit board is designed to be a single-phase NPC structure module consisting of four IGBTs together with four corresponding gate drivers. Accordingly, six boards in total are used to construct the whole three-level back-to-back circuit. To select the semiconductor devices, voltage and current stresses as well as switching frequency should be taken into consideration.

From the characteristic of the three-level NPC structure that the voltage stresses on each semiconductor device is equal to the upper or lower half dc-link voltage, the rated voltage for the power devices must be at least 467 V according to (5.3). With some safety margin, the voltage rating for the chosen semiconductor devices are thus set at 1200 V.

Without detailed analysis of the current flowing through each semiconductor devices, the current rating for the power devices can be figured out from the 5-kVA specification, which is approximately 7.6 A. The current rating of the selected devices is finally determined to be 15-20 A taking into account the current ripples and some additional margin.

Apart from the component stresses, the switching frequency is also taken into consideration. Since the employed switching frequency of 12.2 kHz is moderately high, the fast-switching devices with low-losses available from several manufacturers are recommended. The chosen power devices are listed in Table 5.1.

Table 5.1 Discrete semiconductor devices used in three-level NPC structure.

| | Part Number | Manufacturer | Rating Voltage | Rating Current |
|---|---|---|---|---|
| IGBT with anti-parallel diode | IRG7PH35UD1PbF | International Rectifier | 1200 V | 20 A |
| Clamping diode | Hyperfast diode RHRP15120 | Fairchild Semiconductor | 1200 V | 15 A |

### 5.1.1.3 **Gate Drive Circuits**

A single-channel optocoupler gate driver, HCPL-316J from AVAGO, is used for transmitting the PWM signals from the FPGA to turn on and off the IGBTs. The gate-drive output voltage is +15V for turn-on and -15V for turn-off. Figure 5.3 shows the schematic of the gate drive circuit.

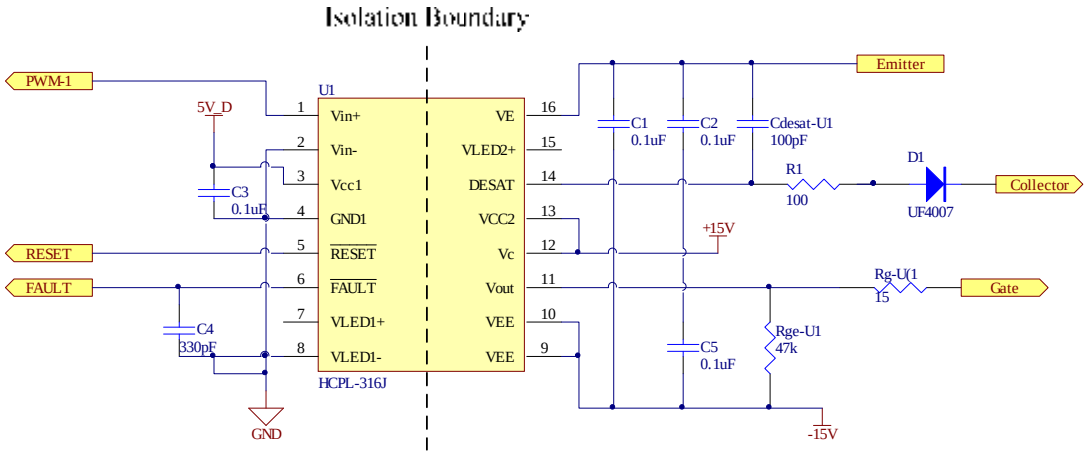



Figure 5.3 Schematic of a gate drive circuit.

The advantages of this gate driver are that it has optical-isolation property, relatively high switching speed, and fault protection features. Firstly, the optical isolation can make the FPGA to control the IGBTs without the physical connection

between the ground point of the FPGA board and the emitter pins of the IGBTs, otherwise that connection may result in a short circuit condition. Moreover, the electrical faults on the power circuit side will be impeded from damaging the controller if they are optically isolated. Secondly, because the PWM frequency is at 12.2 kHz and that the switching speed of gate drivers should be ensured to avoid a long delay in gate-drive signals, 900-ns switching speed of HCPL316J is applicable. Thirdly, this gate driver features good fault protection which can softly turn off the IGBT itself and feedback the fault-alarm signal to the controller to be handled when faults occur.

Due to HCPL316J single channel input-output limitation, one IC is used per one IGBT, and in total 24 gate driver ICs are used for the whole system. Also, the 24 isolated auxiliary +15/-15 power supplies from linear regulators are provided separately for each of gate driver ICs.

#### 5.1.1.4 **Passive Elements**

Theoretically, the required passive elements in the S3L-BTB converter are line reactors and delta-connected capacitors which form an input low-pass filter. Since the S3L-BTB converter is truly equivalent to the matrix converter, it is well-known that the pure *LC* input low-pass filter in the matrix converter can result in oscillation and the stability problem as reported in [17] and [18]. The results of the research in [17] suggests the approach to improve the damping in the *LC* filter without causing excessive losses by paralleling each line reactor with the resistors as depicted in Figure 5.1. For parameter calculation, the guidelines are also given in [17].

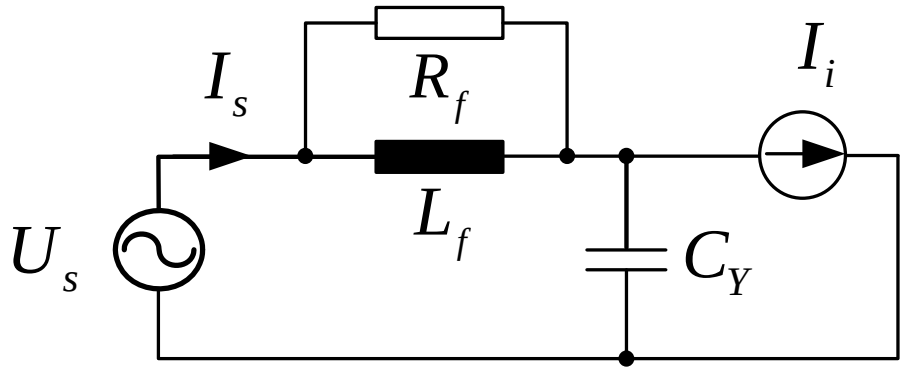



Figure 5.4 Simple per-phase equivalent circuit used for filter design

As the S3L-BTB converter is composed of the symmetry three-phase balanced circuits and is equivalent to the 3L-IMC, a simple per-phase equivalent circuit of the S3L-BTB converter can be drawn as shown in Figure 5.4. The impulsive PWM currents generated by the inverter stage are therein represented by the current source, $I_i$. It will flow through the *LC* low-pass filter and becomes the input supply current, $I_s$. To obtain a sinusoidal supply current with low distortion, the values of the line reactors and capacitors must be carefully selected. The transfer function from the output currents to the input currents is derived in (5.5), with the cut-off frequency, $f_n$, and the damping factor, $\zeta$, of the filter expressed in (5.6) and (5.7), respectively.

$$\frac{I_i(s)}{I_s(s)} = \frac{sL_f + R_f}{s^2 R_f L_f C_Y + sL_f + R_f} \tag{5.5}$$

$$f_n = \frac{1}{2\pi\sqrt{L_f C_Y}} \tag{5.6}$$

$$\zeta = \frac{1}{2R_f}\sqrt{\frac{L_f}{C_Y}} \tag{5.7}$$

For 12.2-kHz PWM frequency, the cut-off frequency is designed to be around one-tenth of the PWM frequency. As a result, $C_Y = 12.5\ \mu\text{F}$ (or for delta-connected capacitors, $C = 4.2\ \mu\text{F}$), and $L_f = 5\ \text{mH}$ are chosen for the cut-off frequency at

637 Hz ( $f_n = 637$ Hz ). And, $R_f = 15\ \Omega$ is selected for damping factor of 0.67 ( $\zeta = 0.67$ ). The corresponding frequency response is shown in Figure 5.5. It can be noticed that the effect of a zero of the transfer functions in (5.5) moves the cut-off frequency further to 1.28 kHz, which nevertheless is still acceptable.

Film capacitors are the good choices for filter applications owing to low ESR and ESL characteristics. In addition, the voltage rating of the capacitors must be consistent with (5.3) and (5.4), which is at least 540 V. Two 350V-capacitors must, therefore, be used in series. The film capacitors of 8-μF are finally chosen to construct the capacitor network at the dc link of the prototype.

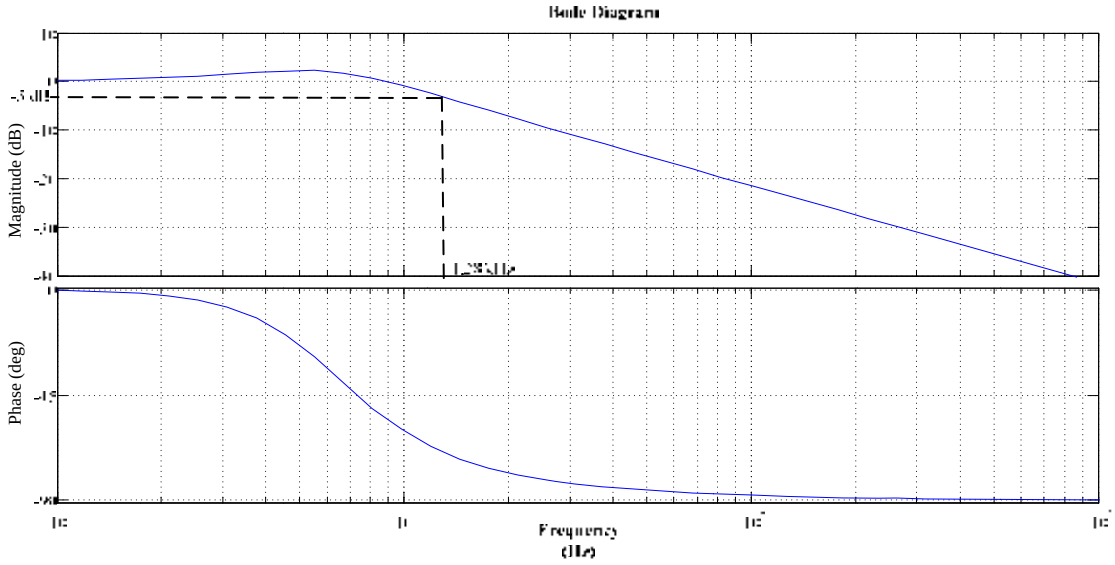



Figure 5.5 Frequency response of the designed input filter of the system

## 5.1.2 **Measurement Circuits**

### 5.1.2.1 **Input Line-To-Line Voltage Measurement**

To isolate the power circuits from the digital controller circuits, the optical isolation with high bandwidth is required in the measurement of the input line-to-line voltages. Isolation amplifier AVAGO ACPL-C790C with 200-kHz bandwidth in Figure 5.6 is selected to sense the two line-to-line voltages at the input terminals of the converter as shown in Figure 5.1. The voltage is attenuated before entering the

isolation amplifier with a voltage-divider circuit to the level that is suitable for the isolation amplifier as depicted in Figure 5.7. In addition, both input and output are of differential types which assist in rejection of common-mode noises.

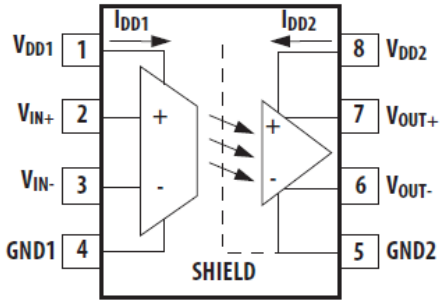



Figure 5.6 Schematic of the optical-isolation amplifier ACPL-C790C.

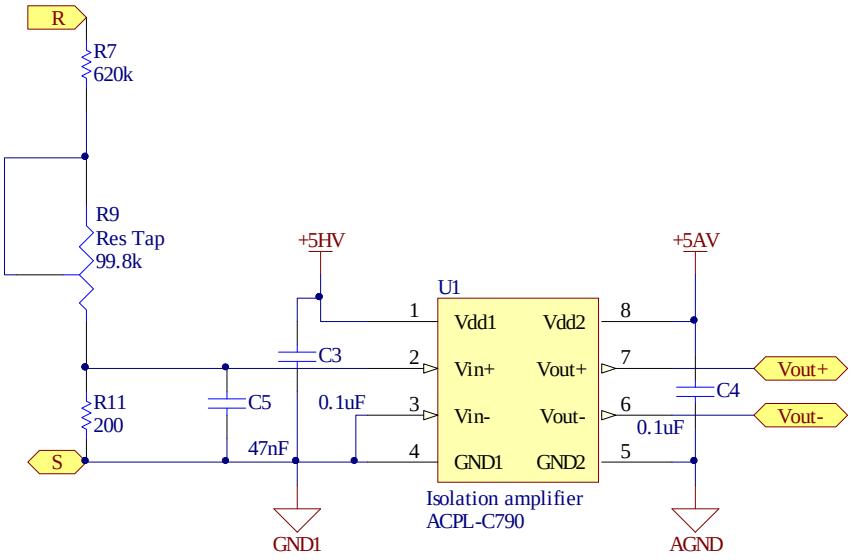



Figure 5.7 Schematic of the line-to-line voltage sensing circuit.

### 5.1.2.2 **Load Current Measurement**

The current transducer HX10-NP from LEM is adopted for measuring two load currents as shown in Figure 5.1. This transducer works on the Hall effect principle, and thus the grounds of the measurement board and the power circuit are isolated. Also, the bandwidth of this current transducer is 50 kHz which is fairly high enough to sense the load currents with 12.2-kHz switching ripples. The rating current of the selected transducer is $10A_{rms}$, which is about twice as high as the rating current of the system.

#### 5.1.2.3 **Analog-to-Digital Converter**

To guarantee the unidirectional polarity of the dc-link voltages, the rectifier operation to be implemented on the FPGA has to detect the transition of the input voltage sector as fast as possible. The sampling rate of the A/D converter used in the line-to-line measurement must be relatively high. Moreover, the 2-channel simultaneous sampling mode is needed for current measurement of PWM converters. Accordingly, the AD7367 A/D converter from Analog Devices which have a high sampling rate up to 1 MSa/s and 2 channels for simultaneous sampling can fulfill the requirements and is employed in the system.

The A/D converter is built on each of the voltage measurement and current measurement boards, and the boards are installed near the measurement points. These steps are done in order to overcome the problem that analog signals are easily interfered by noises during operation due to excessively long wiring. The analog output signals from the sensing ICs, ACPL-C790C and HX10-NP, are amplified with operational amplifiers and converted into 14-bits digital data with AD7367 on the boards. The processes of conversion and obtaining converted digital data are controlled by the FPGA through Serial Peripheral Interface (SPI) as shown in Figure 5.1.

#### 5.1.2.4 **Digital-to-Analog Converter**

To monitor some digital quantities inside the FPGA for debugging purpose, a D/A converter is required. The 12-bit 8-channel TLV5630, D/A converter from Texas Instrument, is used for this task. According to Figure 5.1, it receives the digital data from the FPGA through SPI and outputs the analog signal which is observed by a digital oscilloscope.

## 5.2 **Digital Controller Design**

Digital controllers nowadays are sophisticated and powerful enough to accomplish complicated tasks not possible in the past. Candidates for digital controller implementation of power converter applications are Digital Signal Processors (DSPs) and Field Programmable Gate Arrays (FPGAs). Each of them has

its own superiority over the other in some aspects. In the constructed prototype system, the FPGA is preferable for the following reasons:

- Many resources, e.g. PWM modules, required to operate the three-level back-to-back converter are not available in a single inexpensive DSP.
- Although two DSPs may provide enough resources needed, using two DSPs for each rectifier and inverter stages is a complicated task. Because for the S3L-BTB the rectifier must cooperate with the inverter in generation of the PWM, so they cannot operate independently like in the conventional 3L-BTB converter. For example, the inverter stage needs to know the current sector of the input voltages that the rectifier is working on. Using a single device will be much simpler than using two DSPs, otherwise cumbersome synchronization task is necessary.
- For the S3L-BTB converter, the rectifier stage has to sample the input line-to-line voltage as fast as possible to determine instantaneously the sector of the input voltages, and to generate the corresponding switching signals for the front-end rectifier, while the inverter stage operates on the PWM technique with a fixed and slower sampling frequency. Therefore, the rectifier stage and the inverter stage operate in parallel but at different system sampling rates. This nature is not suitable for implementation with a DSP. On the contrary, with the Hardware Description Language (HDL) an FPGA allows users to flexibly synthesize and implement any desired hardware modules which can work in parallel on their own sampling rate.

Therefore, an inexpensive FPGA from Xilinx (Spartan-3 XC3S400) with 400,000-gate resources is selected for implementation of the digital controller. The modulation strategy for the rectifier and inverter stages is divided into several hardware modules for synthesis as shown in Figure 5.8. The modules are developed with the very-high-speed integrated circuits Description Language (VHDL). It can be seen from Figure 5.8 that the rectifier control modules and the inverter control modules synthesized and implemented on the FPGA work in parallel with its own sampling system frequency. The base clock for the whole system is 25 MHz generated from an on-board oscillator. Due to the different sampling rates, the cooperation between the two stages is done using a down-sampler as shown in Figure

5.8. The inverter stage needs to know the sector of the input voltages and the dc-link line-to-line voltages determined by the rectifier.

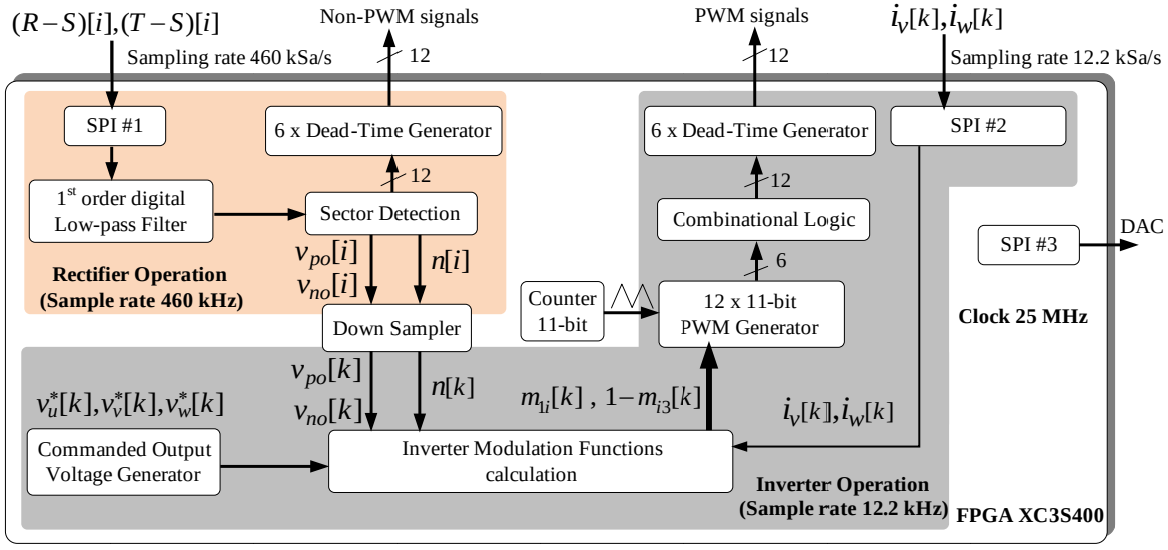



Figure 5.8 Hardware Modules synthesized and implemented on the FPGA.

### 5.2.1 **The Rectifier Operation**

The modulation algorithm for the rectifier stage at the $k^{th}$ sampling time is shown in Figure 5.9. An SPI module is synthesized and used to communicate with the A/D converter on the voltage measurement board for acquiring the samples of the two input line-to-line voltages denoted as $(R-S)[k]$ and $(T-S)[k]$. The sampling rate used is 460 kSa/s. Two sampled input line-to-line voltages are passed through a digital first-order low-pass filter to reduce noises so as to prevent any error on sector determination of the input voltages.

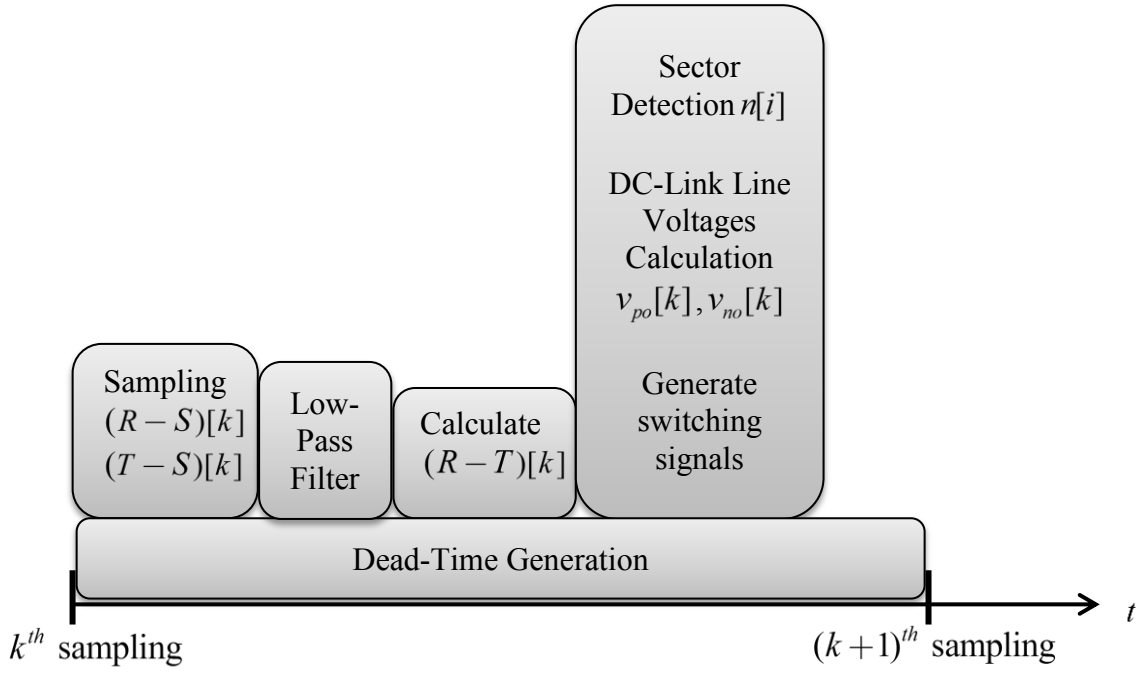



Figure 5.9 Timing diagram of the rectifier operation implemented on the FPGA. (The length of the boxes does not represent the actual time interval being used.)

#### 5.2.1.1 **Digital first-order low-pass filter**

For the continuous-time system, the transfer function between the output voltage and the input voltage of the first-order low pass filter can be written as (5.8).

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{s/\omega_{cutoff} + 1} \tag{5.8}$$

With the backward Euler method, the difference equation for simple digital IIR filter implementation is expressed in (5.9).

$$v_{out}[k] = a v_{in}[k] + (1-a) v_{out}[k-1] \tag{5.9}$$

where $$a = \frac{\omega_{cutoff}}{\omega_{cutoff} + f_{samplling}} \quad . \tag{5.10}$$

To avoid a delay in the filtered output signal, the cut-off frequency is chosen at 5 kHz, and the sampling frequency is at 460 kHz.

### 5.2.1.2 **Sector Detection**

In Figure 5.8, after the block 'Sector Detection' obtains the two line-to-line voltages from the low-pass filter block, the remaining line-to-line voltage $(R-T)[i]$ is calculated using a simple adder. Given three line-to-line voltages, the sector of the input voltages and two dc-link line-to-line voltages ($v_{po} \triangleq v_{max} - v_{mid}$ and $v_{no} \triangleq v_{min} - v_{mid}$) can then be determined. However, the delay caused by the low-pass filter must be taken into account. The effect will be explained in the following for the sinusoidal line-to-line voltage *R*-*S* in the continuous-time system for simplicity.

Given
$$R - S = v_1(t) = V_1 \sin(\omega_1 t) \tag{5.11}$$

After passing through the low-pass filter, the output signal becomes
$$v_2(t) = V_2 \sin(\omega_1 t - \phi) \tag{5.12}$$

with
$$V_2 = \frac{V_1}{\sqrt{1 + \left( \omega_1 / \omega_{cutoff} \right)^2}} \tag{5.13}$$

and
$$\phi = \arctan\left( \frac{\omega_1}{\omega_{cutoff}} \right). \tag{5.14}$$

Since the sector transition occurs when $R = S$ at $\omega_1 t = 0, \pi$ rad, the filtered output signal at that timing is
$$v_o(\pi) = V_{delay} = V_o \sin(\phi) \tag{5.15}$$
$$v_o(0) = -V_{delay} = -V_o \sin(\phi). \tag{5.16}$$

For the supply frequency of 50 Hz and the cut-off frequency at 5 kHz, the delayed voltage $V_{delay}$ becomes
$$V_{delay} = (309)\sin(0.573^\circ) = 3.09 \quad . \tag{5.17}$$

This indicates that the sector transition should be found by comparing the filtered output signal with $V_{delay}$. Likewise, the same is true for the other two line-to-line voltages *T*-*S* and *R*-*T*. The resultant conditions for sector and dc-link voltage determination are summarized in Table 5.2. After knowing the input voltage sector, the switching signals for the front-end rectifier are then generated. At the same time,

the dc-link line-to-line voltages $v_{po}[k]$, $v_{no}[k]$ and the input voltage sector $n[k]$ are stored in registers waiting for the inverter stage to read. Six pairs of the complementary switching signals are finally adjusted by a dead-time generator to avoid shoot through in the phase leg.

Table 5.2 The determination of the input voltage sector and calculation of the dc-link line-to-line voltages.

| Sector | $R-S$ | $S-T$ | $R-T$ | $v_{po}$ | $v_{no}$ |
|---|---|---|---|---|---|
| 1 $(R \geq S \geq T)$ | $\geq -V_{delay}$ | $\geq -V_{delay}$ | $\geq -V_{delay}$ | $(R-S)$ | $T-S$ |
| 2 $(S \geq R \geq T)$ | $\leq V_{delay}$ | $\geq -V_{delay}$ | $\geq -V_{delay}$ | $-(R-S)$ | $-(R-T)$ |
| 3 $(S \geq T \geq R)$ | $\leq V_{delay}$ | $\geq -V_{delay}$ | $\leq V_{delay}$ | $-(T-S)$ | $(R-T)$ |
| 4 $(T \geq S \geq R)$ | $\leq V_{delay}$ | $\leq V_{delay}$ | $\leq V_{delay}$ | $(T-S)$ | $(R-S)$ |
| 5 $(T \geq R \geq S)$ | $\geq -V_{delay}$ | $\leq V_{delay}$ | $\leq V_{delay}$ | $-(R-T)$ | $-(R-S)$ |
| 6 $(R \geq T \geq S)$ | $\geq -V_{delay}$ | $\leq V_{delay}$ | $\geq -V_{delay}$ | $(R-T)$ | $-(T-S)$ |

### 5.2.2 **The Inverter Operation**

The modulation algorithm for the inverter stage at $k^{th}$ sampling is shown in Figure 5.10. The sampling frequency is set equal to the PWM switching frequency of 12.2 kHz. At the beginning of the sampling period, the two load currents, $i_v[k]$ and $i_w[k]$, are acquired from the current measurement boards through SPI, and the values of the modulation functions calculated in the previous period are loaded to the PWM generator as references. The reference values of modulation functions are then compared with the triangular carrier generated by a 11-bit counter. Synchronously,

the dc-link line-to-line voltages $v_{po}$ , $v_{no}$ and the input voltage sector $n$ stored in the registers mentioned in the rectifier operation are read as $v_{po}[k]$ , $v_{no}[k]$ and $n[k]$. Also, the balanced three-phase sinusoidal commanded output voltages $u^*[k]$, $v^*[k]$ and $w^*[k]$ are generated from a look-up table.

### 5.2.2.1 **Modulation Function Calculation**

All the quantities obtained in the previous Sections are used to calculate the modulation functions for the double-carrier-based PWM. With the measured voltages and currents, the equations for the modulation functions given (3.18) and (3.19) in Chapter III are rewritten in (5.18)-(5.19).

From
$$\begin{bmatrix} m_{11}^{(i)} \\ m_{21}^{(i)} \\ m_{31}^{(i)} \end{bmatrix} = \begin{bmatrix} m_{11}'^{(i)} + x' \\ m_{21}'^{(i)} + x' \\ m_{31}'^{(i)} + x' \end{bmatrix} \tag{5.18}$$

and
$$\begin{bmatrix} m_{13}^{(i)} \\ m_{23}^{(i)} \\ m_{33}^{(i)} \end{bmatrix} = \begin{bmatrix} m_{13}'^{(i)} + z' \\ m_{23}'^{(i)} + z' \\ m_{33}'^{(i)} + z' \end{bmatrix} \tag{5.19}$$

where
$$\begin{bmatrix} m_{11}'^{(i)} \\ m_{12}'^{(i)} \\ m_{13}'^{(i)} \end{bmatrix} = \frac{1}{\left(v_{max}^2 + v_{mid}^2 + v_{min}^2\right)} \begin{pmatrix} v_{max} \begin{bmatrix} u^* \\ v^* \\ w^* \end{bmatrix} + (-1)^{n+1} \frac{k_1}{\sqrt{3}} \left(v_{mid} - v_{min}\right) \begin{bmatrix} i_u \\ i_v \\ i_w \end{bmatrix} + \\ (-1)^{n+1} \frac{k_2}{3} \left(v_{mid} - v_{min}\right) \begin{bmatrix} i_v - i_w \\ i_w - i_u \\ i_u - i_v \end{bmatrix} \end{pmatrix} \tag{5.20}$$

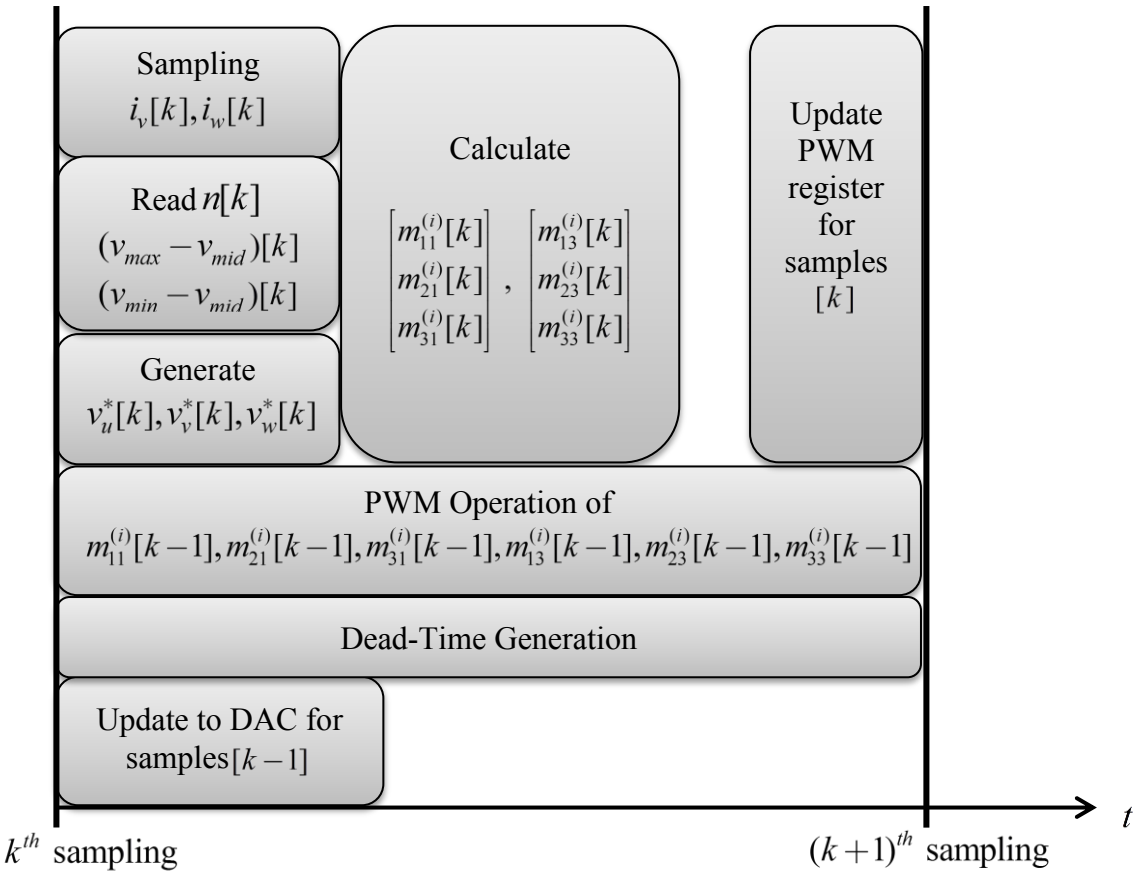



Figure 5.10 Timing diagram of the inverter operation implemented on the FPGA
(The length of the boxes does not represent the actual time interval being used)

and

$$\begin{bmatrix} m_{13}'^{(i)} \\ m_{23}'^{(i)} \\ m_{33}'^{(i)} \end{bmatrix} = \frac{1}{\left(v_{max}^2 + v_{mid}^2 + v_{min}^2\right)} \left( \begin{aligned} & v_{min} \begin{bmatrix} u^* \\ v^* \\ w^* \end{bmatrix} + (-1)^{n+1} \frac{k_1}{\sqrt{3}} (v_{max} - v_{mid}) \begin{bmatrix} i_u \\ i_v \\ i_w \end{bmatrix} \\ & + (-1)^{n+1} \frac{k_2}{3} (v_{max} - v_{mid}) \begin{bmatrix} i_v - i_w \\ i_w - i_u \\ i_u - i_v \end{bmatrix} \end{aligned} \right) \tag{5.21}$$

The measured line quantities, $v_{po}$ , $v_{no}$ , $i_v$ , $i_w$, can be expressed as phase quantities referred to a virtual neutral point as:

$$v_{max} = \frac{2v_{po} - v_{no}}{3} \tag{5.22}$$

$$v_{mid} = -\frac{v_{po} + v_{no}}{3} \tag{5.23}$$

$$v_{min} = \frac{2v_{no} - v_{po}}{3} \tag{5.24}$$

with
$$v_{max}^2 + v_{mid}^2 + v_{min}^2 = \frac{2}{3}\left(v_{po}^2 - v_{po}v_{no} + v_{no}^2\right) \tag{5.25}$$

$$i_u = -\left(i_v + i_w\right). \tag{5.26}$$

Substituting (5.22) - (5.26) into (5.20) and (5.21), the required modulation functions can be obtained in terms of line quantities as shown in (5.27) and (5.28).

$$\begin{bmatrix} m_{11}'^{(i)} \\ m_{12}'^{(i)} \\ m_{13}'^{(i)} \end{bmatrix} = \frac{1}{2\left(v_{po}^2 - v_{po}v_{no} + v_{no}^2\right)} \left( \left(2v_{no} - v_{po}\right) \begin{bmatrix} u^* \\ v^* \\ w^* \end{bmatrix} + \sqrt{3}\left(-1\right)^n k_1 v_{no} \begin{bmatrix} -(i_v + i_w) \\ i_v \\ i_w \end{bmatrix} \right) \tag{5.27}$$

$$\begin{bmatrix} m_{13}'^{(i)} \\ m_{23}'^{(i)} \\ m_{33}'^{(i)} \end{bmatrix} = \frac{1}{2\left(v_{po}^2 - v_{po}v_{no} + v_{no}^2\right)} \left( \left(2v_{no} - v_{po}\right) \begin{bmatrix} u^* \\ v^* \\ w^* \end{bmatrix} - \sqrt{3}\left(-1\right)^n k_1 v_{po} \begin{bmatrix} -(i_v + i_w) \\ i_v \\ i_w \end{bmatrix} \right) \tag{5.28}$$

Note that since utilization of $k_2$ is out of scope of this thesis, $k_2$ then is set to zero for all experiments, and is not implemented at this time.

The zero voltage components *x'* and *z'* remain the same as:

$$x' = -\min\left(m_{11}'^{(i)}, m_{12}'^{(i)}, m_{13}'^{(i)}\right) \tag{5.29}$$

$$z' = -\min\left(m_{13}'^{(i)}, m_{23}'^{(i)}, m_{33}'^{(i)}\right). \tag{5.30}$$

Consequently, calculation of (5.27)-(5.30) is synthesized based on fixed-point calculation with 14 fractional bits and 3 signed-integer bits. The digital signal processing tasks, such as multiplication and division, are carried out with built-in hardware multipliers and a single synthesized divisor.

#### 5.2.2.2 **PWM Generator**

After the six modulation functions are calculated, they are normalized to 11-bit numbers for comparing with the 11-bit counter. In the implementation of the double-carrier PWM, for simplicity only one counter is shared by both the upper and lower triangular carriers. Therefore, the 11-bit negative modulation functions

$\left[-m_{13}^{(i)} \quad -m_{23}^{(i)} \quad -m_{33}^{(i)}\right]^T$ will be shifted up by $2^{10}$ (the amplitude of the carrier waveform) to be the final positive reference values. According to Figure 5.8, the output PWM signals obtained from the comparators will be passed to a combinational logic circuit in Figure 5.11 and subsequently to the dead-time generators, in order to generate the gate drive signals for each IGBT in each phase leg of the S3L-BTB converter.

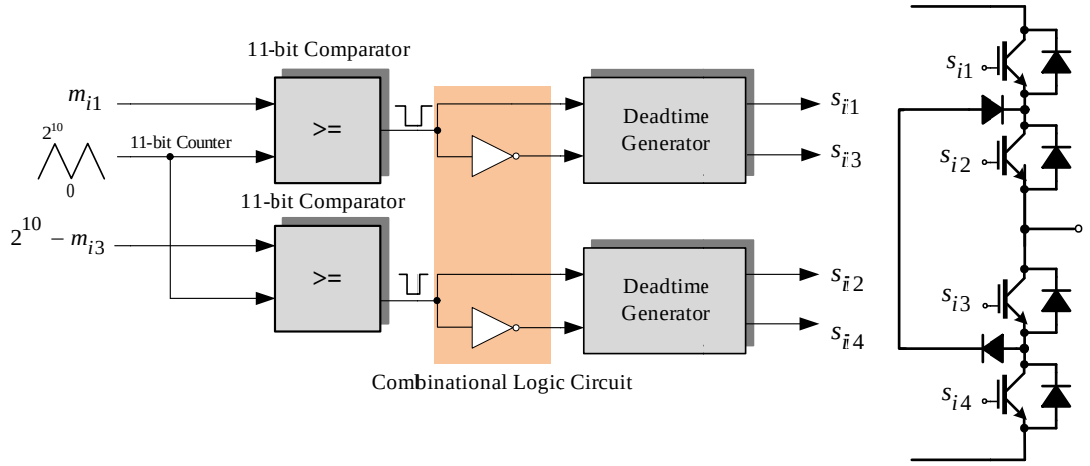



Figure 5.11 Simplified diagram of double-carrier-based PWM and the combinational logic circuit for generating the gate drive signals.

## 5.3 **Experimental Results**

To verify the performances of the S3L-BTB converter on the laboratory prototype together with the operation of the controller, the system in Figure 5.12 is set up and tested under several conditions according to the conditions in Table 5.3, which are the same as those of the simulation in Table 4.1 for the sake of comparison. The objectives of the experiments are to confirm the performances regarding output voltage variation, output frequency variation, and input power factor compensation. All the voltages monitored in the system are measured relative to the neutral point *N* at the supply side. The modulation free parameters $k_1$ is set to zero except for the cases 7, 8, 9.

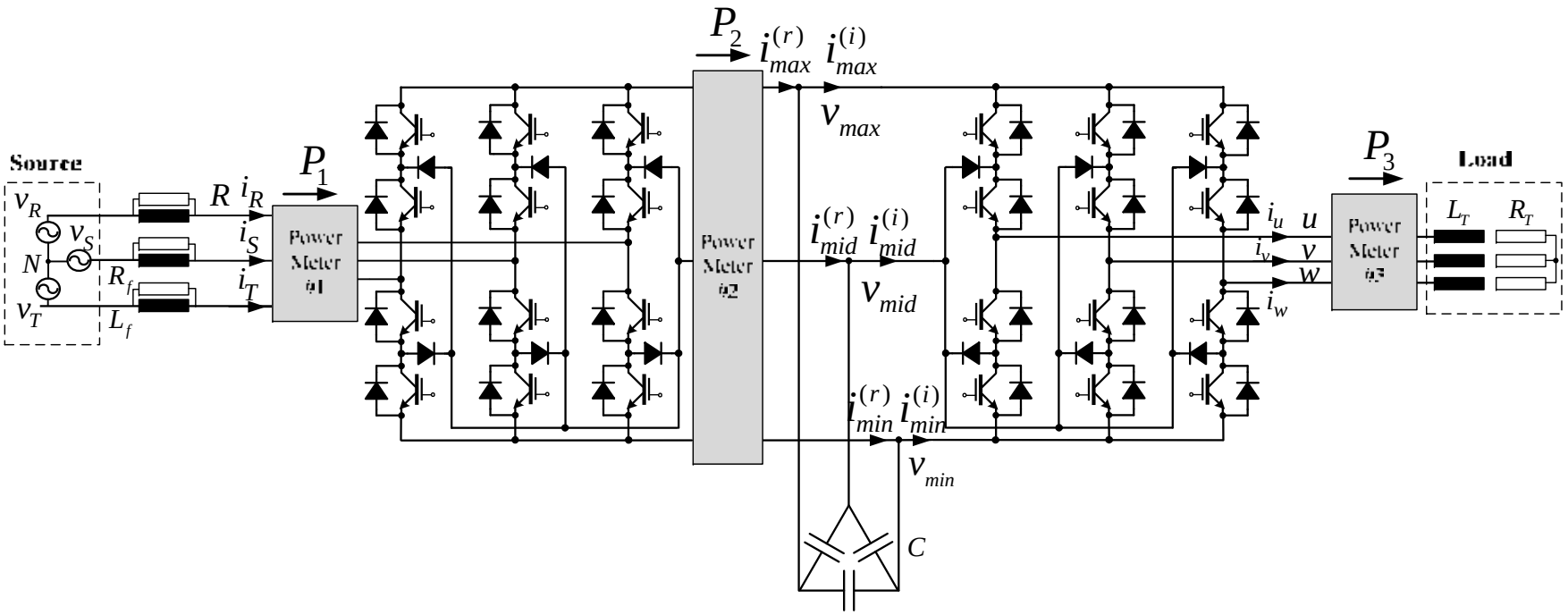



Figure 5.12 Schematic of the experimental setup for testing of the S3L-BTB converter.

The system parameters of Figure 5.12 are summarized as follows:

Supply voltage: balanced three-phase sinusoidal line-to-line voltage 380 $V_{rms}$ 50 Hz

Source frequency: 50 Hz

PWM switching frequency: 12.2 kHz

Delta-connected capacitor: $C$ = 4.2 μF

Input line reactance: $L_f$ = 5 mH

Damping resistor: $R_f$ = 15 Ω

Series *RL* load : $R_T$ = 24 Ω and $L_T$ = 33.3 mH.

Table 5.3 Experimental conditions for performance testing of the prototyped S3L-BTB converter.

| **Case** | **Objectives** | | **Test conditions** | | |
|---|---|---|---|---|---|
| | | | **Modulation index** $\left(V_o/V_i\right)$ | **Output frequency (Hz)** | **Figure** |
| 1 | Output voltage variation | | 0.3 | 50 | 5.13<br>5.14 |
| 2 | | | 0.5 | 50 | 5.15<br>5.16 |
| 3 | | | 0.86 | 50 | 5.17<br>5.18 |
| 4 | Output frequency variation | | 0.86 | 25 | 5.19<br>5.20 |
| 5 | | | 0.86 | 100 | 5.21<br>5.22 |
| 6 | Input power factor compensation | No Compensation | 0.7 | 50 | 5.23<br>5.24<br>5.31 |
| 7 | | Unity power factor | 0.7 | 50 | 5.25<br>5.26<br>5.32 |
| 8 | | Lagging compensation | 0.7 | 50 | 5.27<br>5.28<br>5.33 |
| 9 | | Leading compensation | 0.7 | 50 | 5.29<br>5.30<br>5.34 |

### 5.3.1 **Output Voltage Variation**

To have a capability of output voltage variation, the prototyped converter must be able to freely produce the output voltage in a wide range of magnitude. With a fixed output frequency of 50 Hz, three modulation indices, 0.3, 0.5 and 0.86 corresponding to low, moderate, and high modulation indices are selected as commanded output voltages. All the results in Figures 5.13-5.18 are in good agreement with the simulation results in Chapter IV.

For the balanced three-phase sinusoidal supply voltages $\{v_R, v_S, v_T\}$, the converter can generate the PWM output voltages {*u*,*v*,*w*} yielding the balanced sinusoidal load currents $\{i_u, i_v, i_w\}$ and simultaneously the balanced sinusoidal supply currents $\{i_R, i_S, i_T\}$. The results are presented in Figure 5.13, 5.15 and 5.17.

Figure 5.14, 5.16 and 5.18 present the detailed responses of the prototyped system. They clearly illustrate that the S3L-BTB converter can obtain the sinusoidal supply current with the non-PWM operation of the rectifier. The front-end rectifier switches at the power-line frequency to form the max-mid-min dc-link voltages, and the input terminal voltage of the converter, *R*, is sinusoidal. This obviously indicates the low losses and low EMI properties at the front-end rectifier of this prototype. The proper operation of the rectifier stage implemented on the FPGA is thus confirmed.

Considering the dc-link currents, the impulsive PWM current resulting from the back-end inverter $i_{max}^{(i)}$ is filtered by the capacitor network and become the smooth current $i_{max}^{(r)}$, whose waveform is a portion of a sinusoidal waveform. The current is then rearranged by the action of the rectifier and combined with the other two dc-link currents $i_{mid}^{(r)}$ and $i_{min}^{(r)}$ to become a sinusoidal current $i_R$ at the input.

The modulation functions of phase *u*, $m_{11}^{(i)}$ and $-m_{13}^{(i)}$, and the resulting PWM output voltage are shown in Figure 5.14, 5.16 and 5.18. The results are consistent with those obtained in the simulation results. The magnitude of the modulation functions increases when the modulation index gets higher. The unipolar PWM can be observed during the period when either $m_{11}^{(i)}$ or $-m_{13}^{(i)}$ is zero, while the remaining period is in the dipolar mode. This indicates the perfect operation of the synthesized inverter

operation. All the results point out that the cooperation between the rectifier and the inverter operations is perfectly achieved with a single FPGA.

Without input power factor compensation, the supply currents with leading phase can be observed because of the reactive current from the capacitor network at the dc link. The effect becomes more obvious in the condition of low modulation index under which the active power is low.

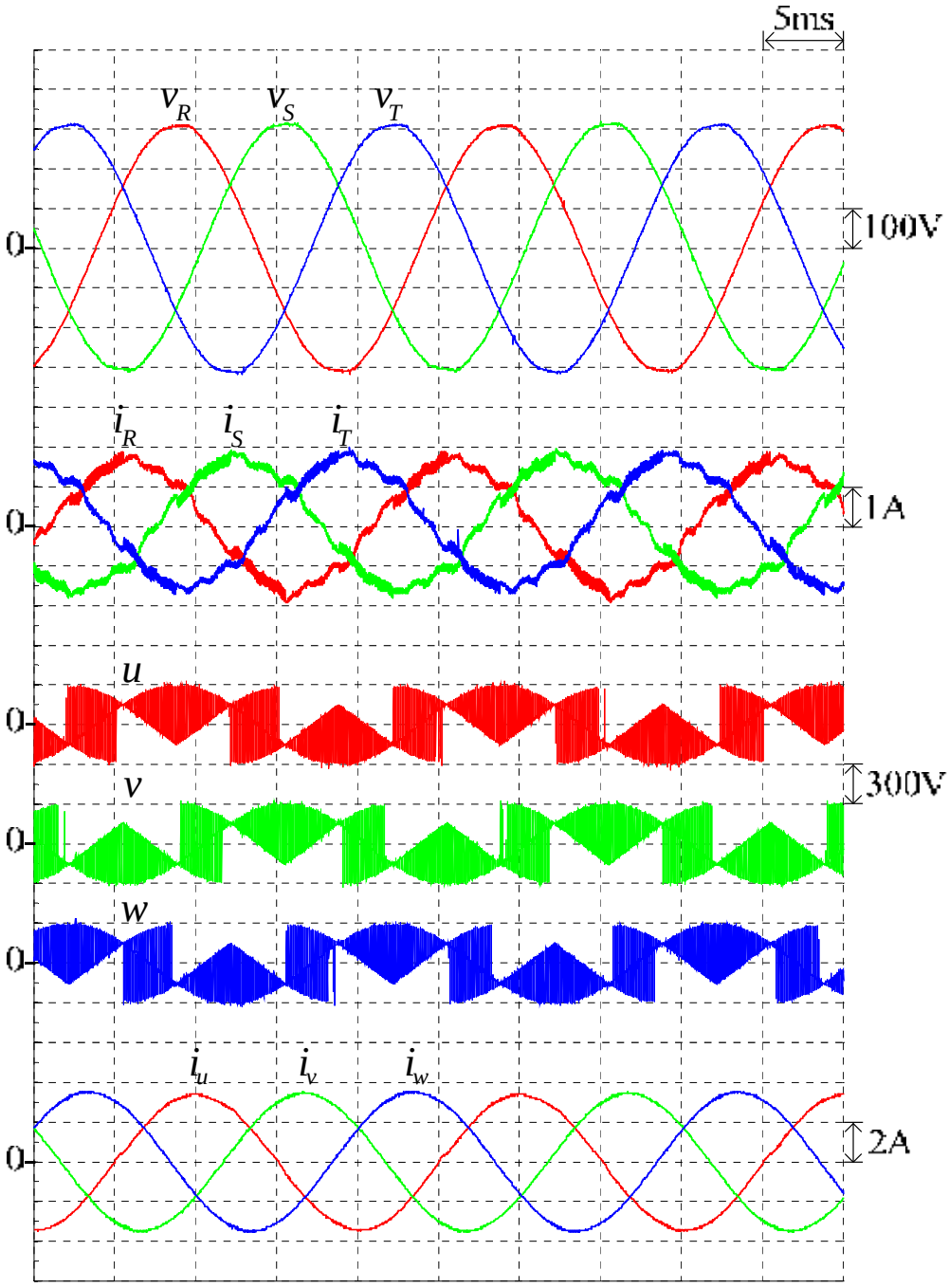



Figure 5.13 Measured input-output waveforms of the prototyped S3L-BTB converter under output voltage variation at ($M$ = 0.3, $f_o$ = 50 Hz)

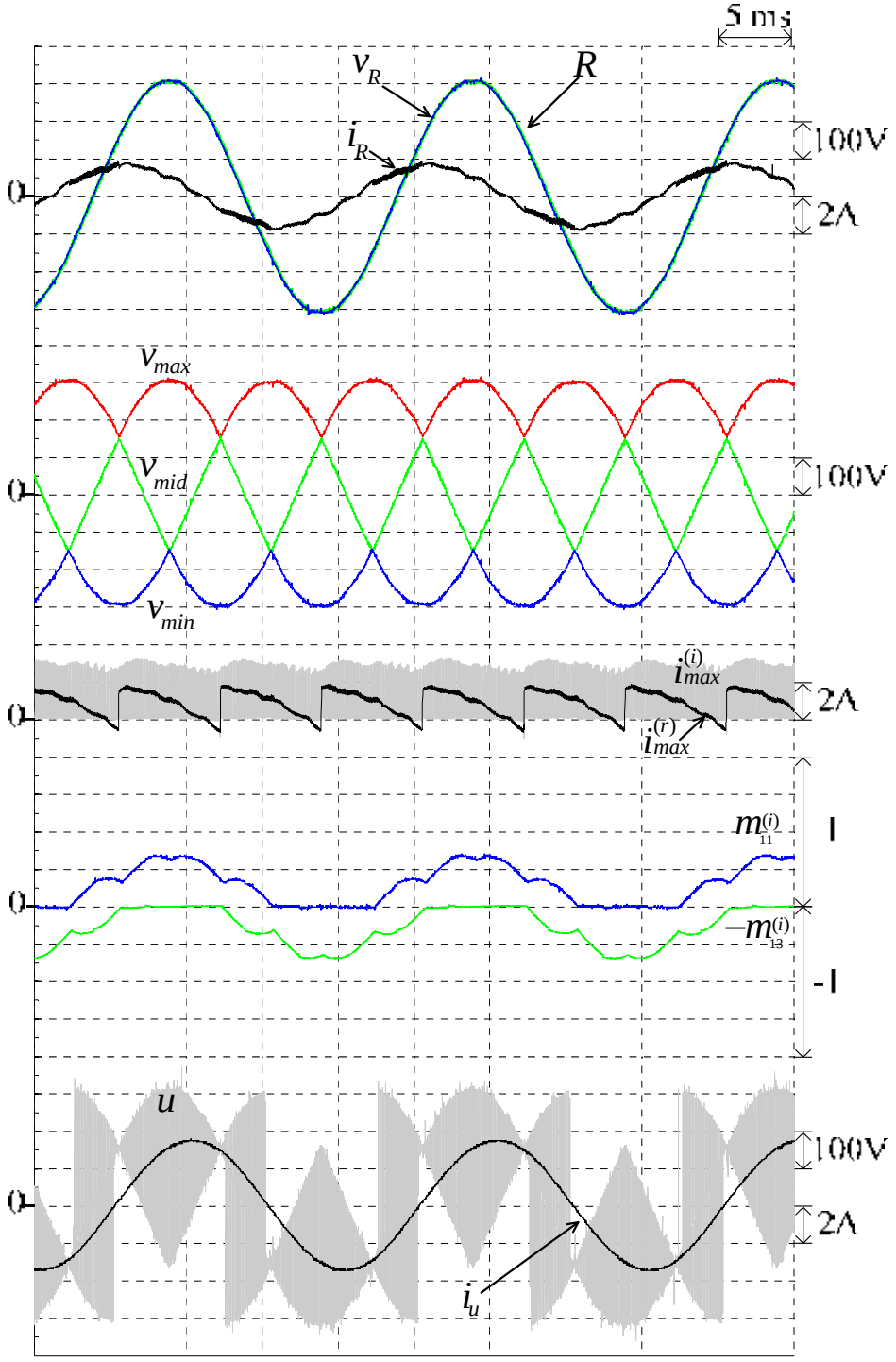



Figure 5.14 Measured waveforms of the prototyped S3L-BTB converter under output voltage variation at ($M$ = 0.3, $f_o$ = 50 Hz)

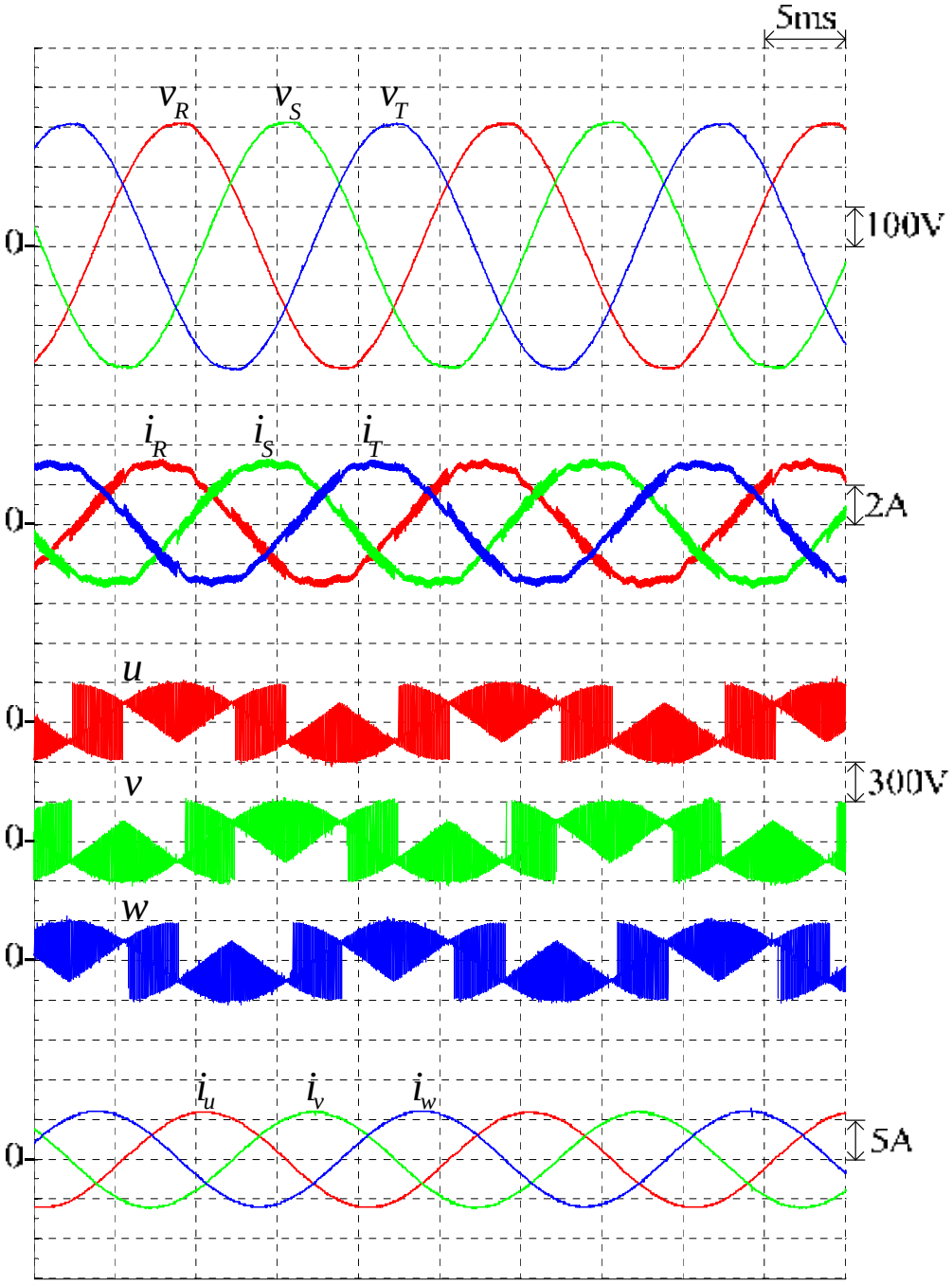



Figure 5.15 Measured input-output waveforms of the prototyped S3L-BTB converter under output voltage variation at ($M$ = 0.5, $f_o$ = 50 Hz)

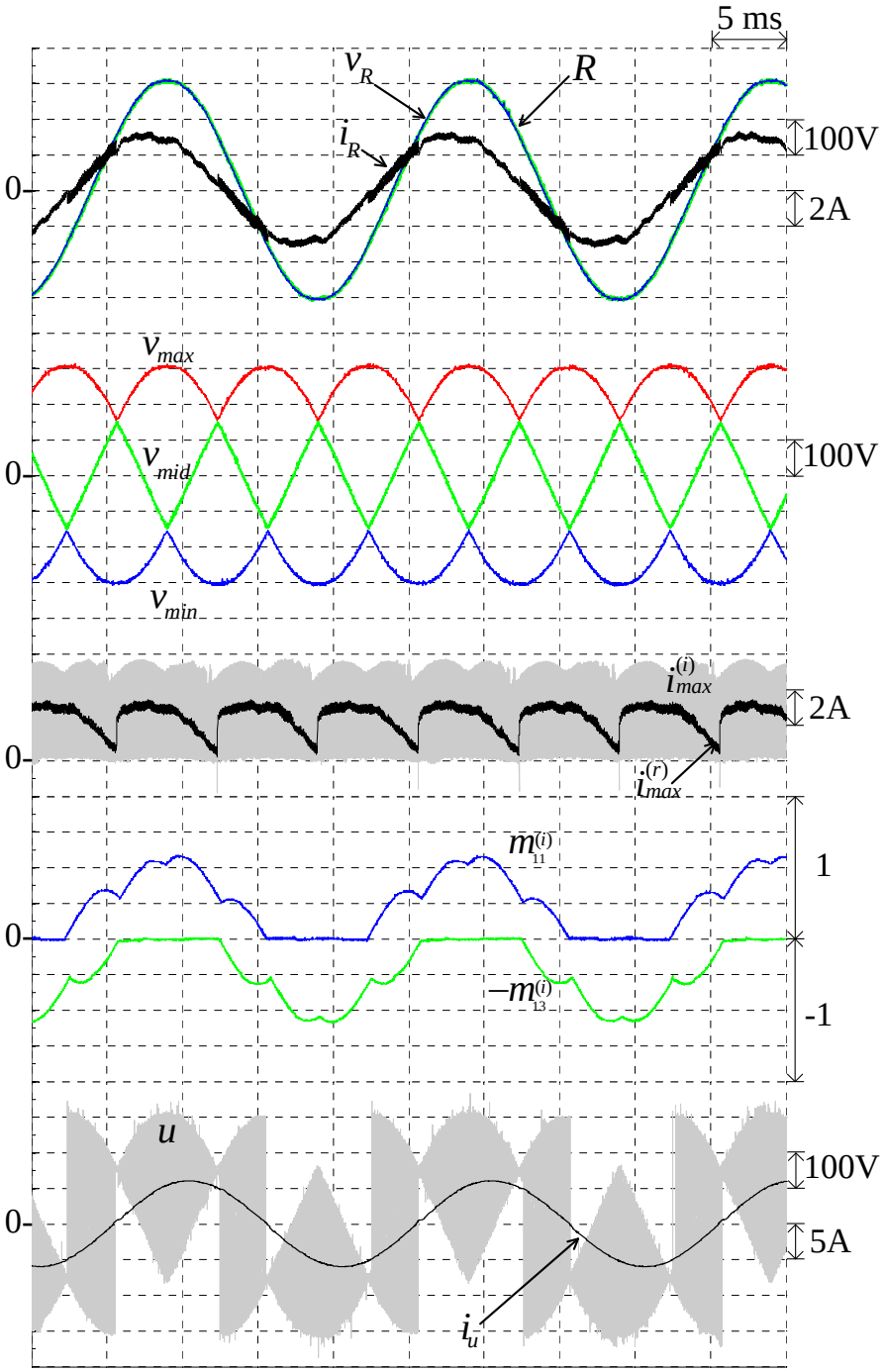



Figure 5.16 Measured waveforms of the prototyped S3L-BTB converter under output voltage variation at ($M$ = 0.5, $f_o$ = 50 Hz)

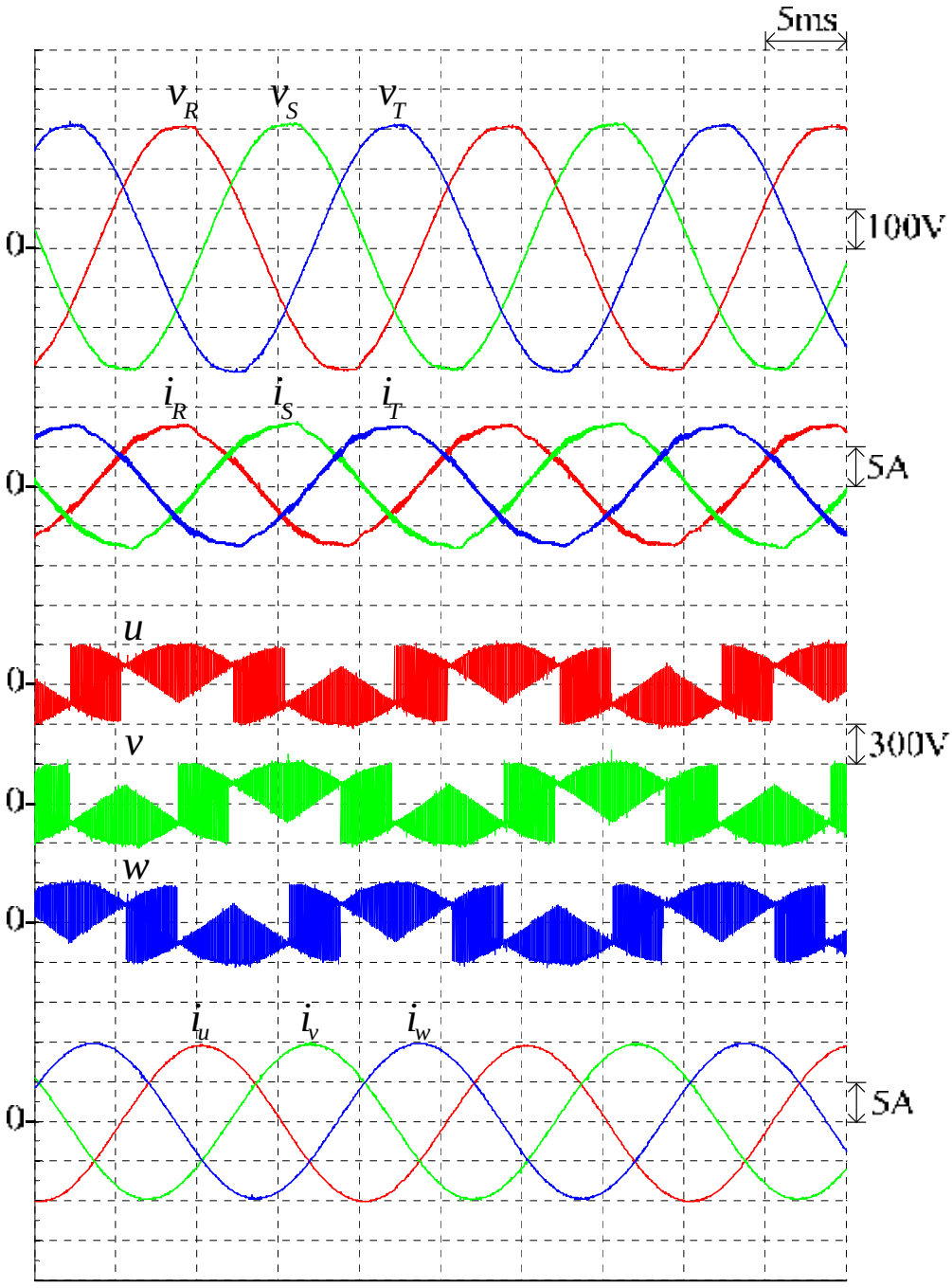



Figure 5.17 Measured input-output waveforms of the prototyped S3L-BTB converter under output voltage variation at ($M$ = 0.86, $f_o$ = 50 Hz)

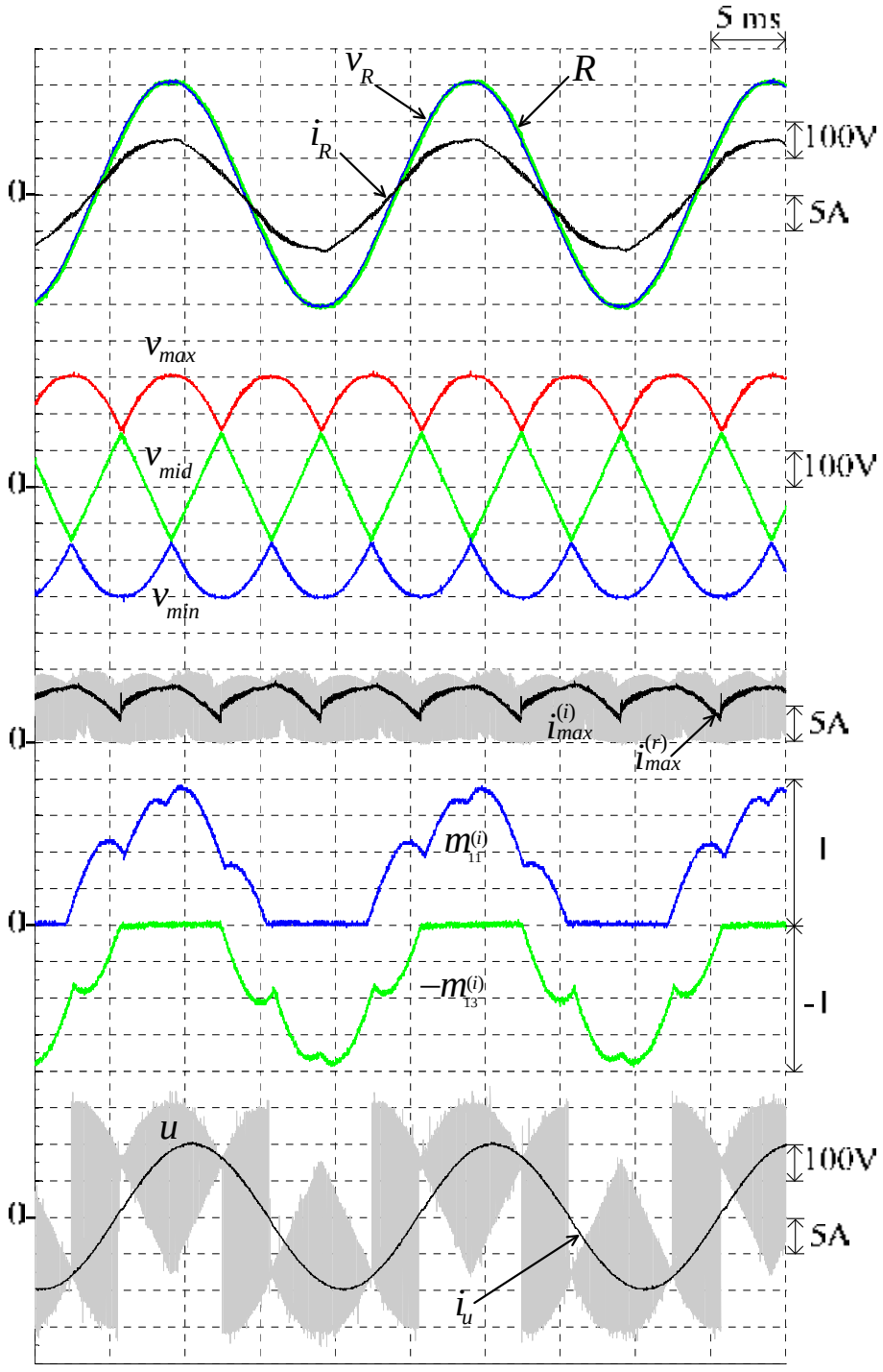



Figure 5.18 Measured waveforms of the prototyped S3L-BTB converter under output voltage variation at ($M$ = 0.86, $f_o$ = 50 Hz)

### 5.3.2 **Output Frequency Variation**

The experiments on output frequency variation for the prototyped S3L-BTB converter are carried out by changing the frequency of the commanded output voltage to be below and above the supply power-line frequency of 50 Hz. Figure 5.19 - 5.22 are the experimental results according to the conditions 4 and 5 of Table 5.4, under which the 25-Hz and 100-Hz sinusoidal output voltages are commanded while the modulation index is kept at its maximum of 0.86.

Figure 5.19 and 5.21 reveal the capability of the converter to change the frequency of the output voltages while still achieving the balanced three-phase sinusoidal supply currents.

Figure 5.20 and 5.22 display the detailed responses of the prototyped S3L-BTB converter, which are generally the same as the simulation results. It can be seen that the waveforms of the modulation functions, $m_{11}^{(i)}$ and $-m_{13}^{(i)}$ are modulated with the commanded output frequency in order to generate the required output voltages.

Also, the output power factor is affected from the change of frequency. The output power factor increases to 0.977 at 25 Hz and decreases to 0.754 at 100 Hz Nonetheless, the constructed prototype is able to work properly. Although the changing of output power factor has a direct effect on the dc-link currents generated by the inverter stage, the capacitor network together with the line reactors forming as a low-pass filter can filtered the impulsive currents out. The results are the smooth currents with the same frequency as the dc-link voltages as depicted in Figure 5.20 and 5.22.

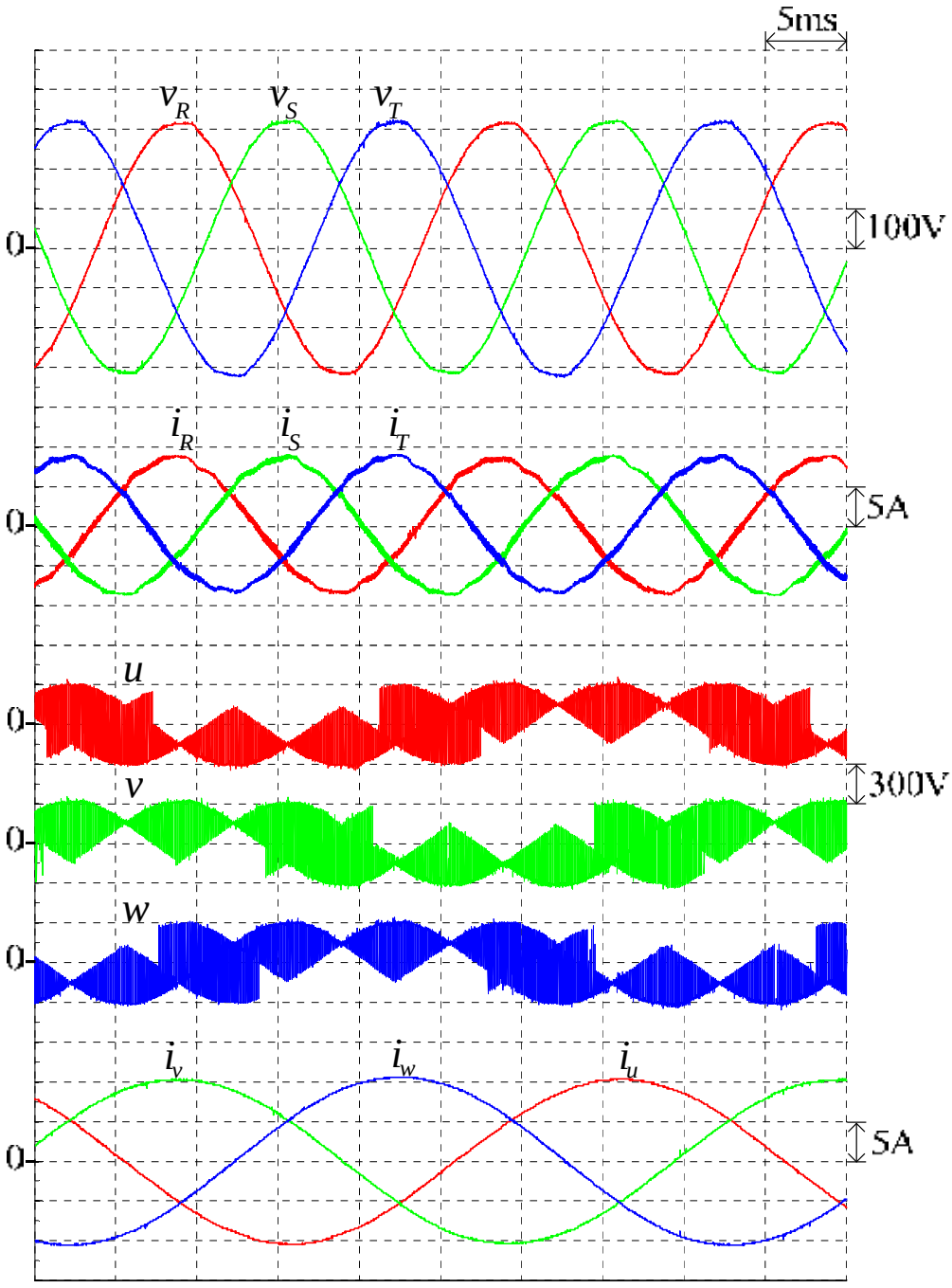



Figure 5.19 Measured input-output waveforms of the prototyped S3L-BTB converter under output frequency variation at ($M$ = 0.86, $f_o$ = 25 Hz)

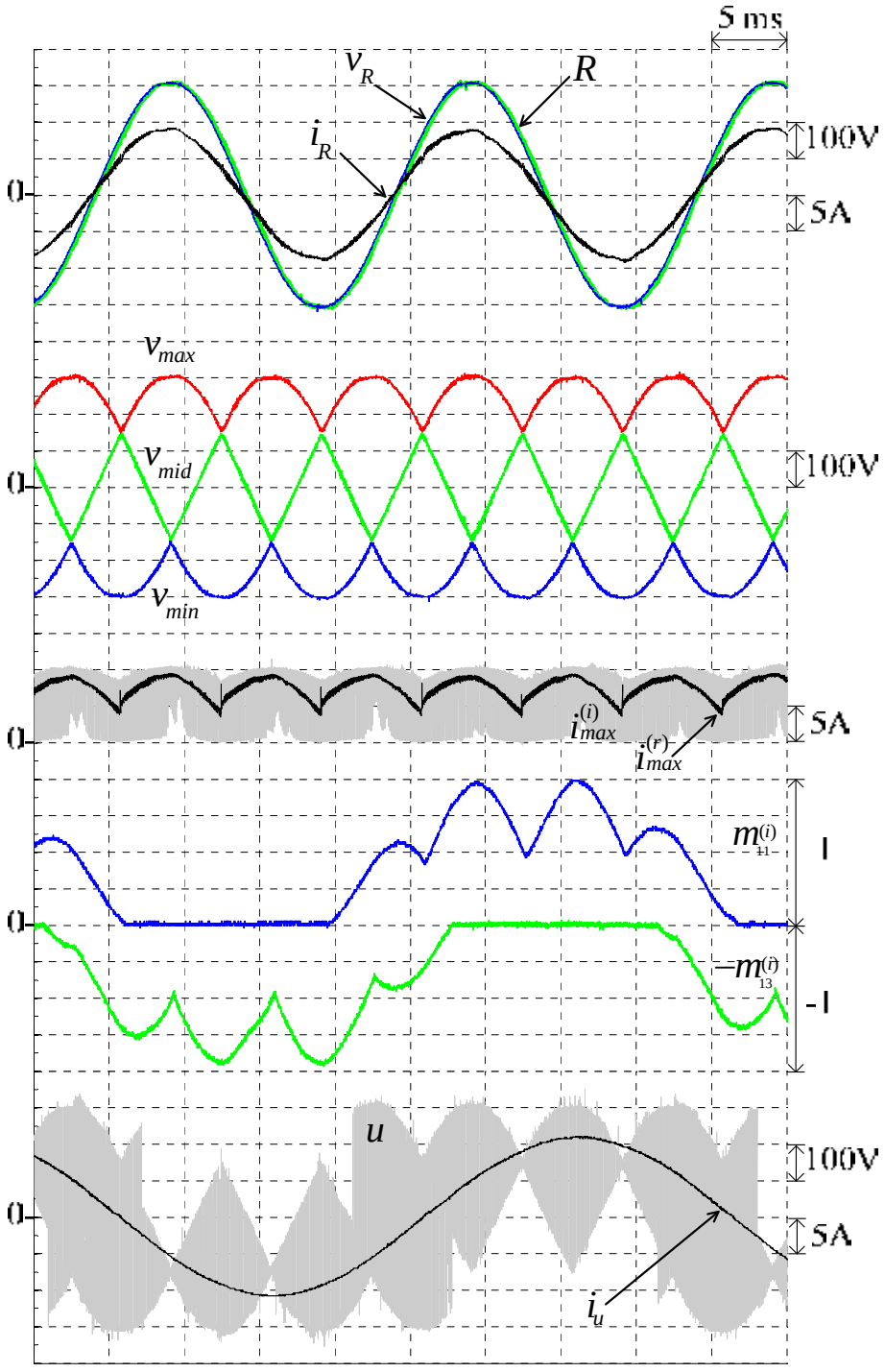



Figure 5.20 Measured waveforms of the prototyped S3L-BTB converter under output frequency variation at ($M$ = 0.86, $f_o$ = 25 Hz)

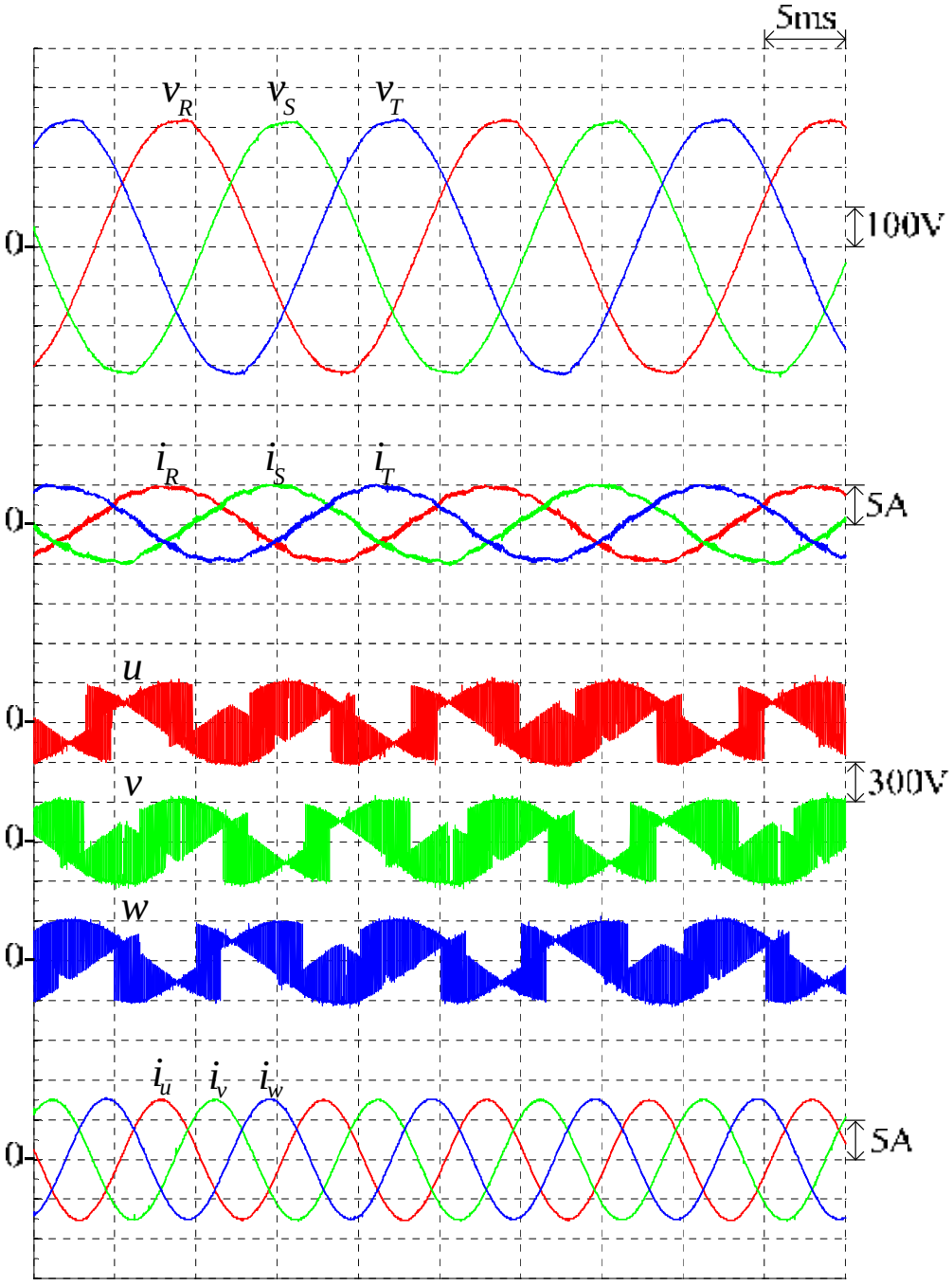



Figure 5.21 Measured input-output waveforms of the prototyped S3L-BTB converter under output frequency variation at ($M$ = 0.86, $f_o$ = 100 Hz)

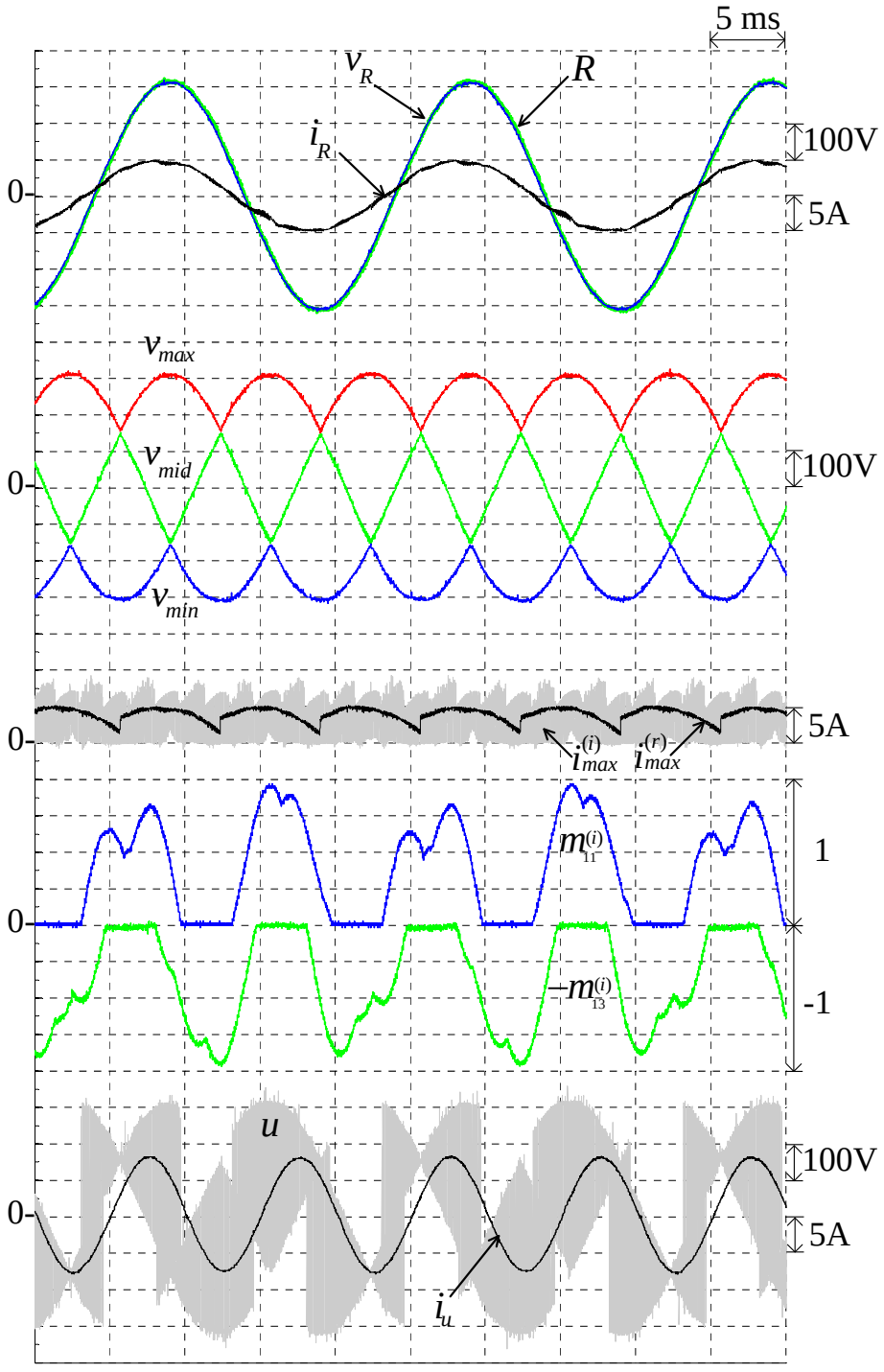



Figure 5.22 Measured waveforms of the prototyped S3L-BTB converter under output frequency variation at ($M$ = 0.86, $f_o$ = 100 Hz)

### 5.3.3 **Input Power Factor Compensation**

As presented in the simulation results of input power factor compensation, the S3L-BTB converter can theoretically compensates the unwanted reactive power from the capacitor network. The experiment conducted on the hardware prototype of the S3L-BTB converter confirms this capability as can be seen from Figures 5.23 - 5.34. The conditions of the experiments on power factor correction are identical to those of the simulation. The commanded modulation index is set to 0.7 to leave some margin to compensate the input reactive power without overmodulation. Figure 5.23, 5.24 and 5.31, which are the results when operating without input power factor compensation ($k_1 = 0$), are given for comparison.

The good cooperation between the rectifier and the inverter operations designed in the FPGA is verified by this experiment also because for the converter to work properly the inverter stage has to know the input voltage sector determined by the rectifier stage to be able to employ the free parameter $k_1$ correctly according to (5.27) and (5.28).

Figure 5.25 and 5.26 show the responses of the system for unity input power factor compensation. The results are in good agreement with those of the simulations. The load currents remain unaffected by the utilization of the free parameter $k_1$. However, the discontinuities in modulation functions, $m_{11}^{(i)}$ and $-m_{13}^{(i)}$ due to the transition of the input voltage sector can be noticed, and the changing of the modulation functions leads to additional phase shift in the filtered dc-link currents in Figure 5.32 compared to those of Figure 5.31. If the unity power factor compensation is to be accomplished, the filtered dc-link currents must be proportional or in phase with the dc-link voltages, and be recombined to become the sinusoidal current in phase with the supply voltages.

Figure 5.27 and 5.28 present the responses of the system when lagging input power factor is obtained with $k_1 = 15$. Similar to the simulation, increasing the free parameter $k_1$ results in drastic changes in the modulation function waveforms and also in the dc-link current $i_{max}^{(i)}$. As a result, the phase shift of $i_{max}^{(r)}$ is obviously seen, with

which the recombined supply currents become lagging in Figure 5.27. However, some distortions appear in the filtered dc-link current as seen in $i_{max}^{(r)}$ and in the resultant supply current $i_R$ in the vicinity of the discontinuities.

The prototyped S3L-BTB converter can make the supply currents more leading by using a negative value for $k_1$. The experimental results of this phenomenon are shown in Figure 5.29, 5.30 and 5.34 for $k_1 = -3.3$. The results are also consistent with the simulation ones.

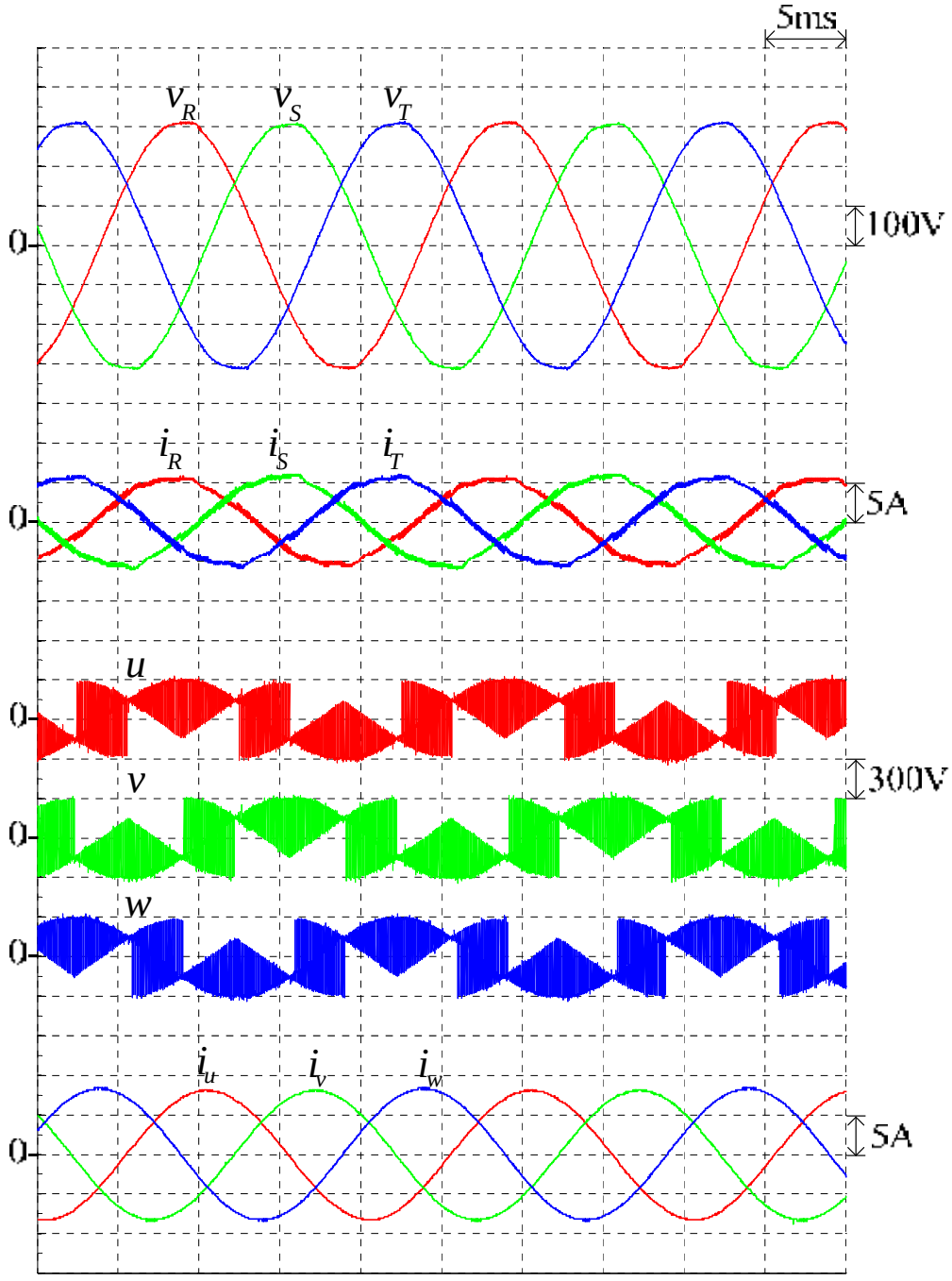



Figure 5.23 Measured input-output waveforms of the prototyped S3L-BTB converter without input power factor compensation at ($M$ = 0.7, $f_o$ = 50 Hz, $k_1 = 0$ )

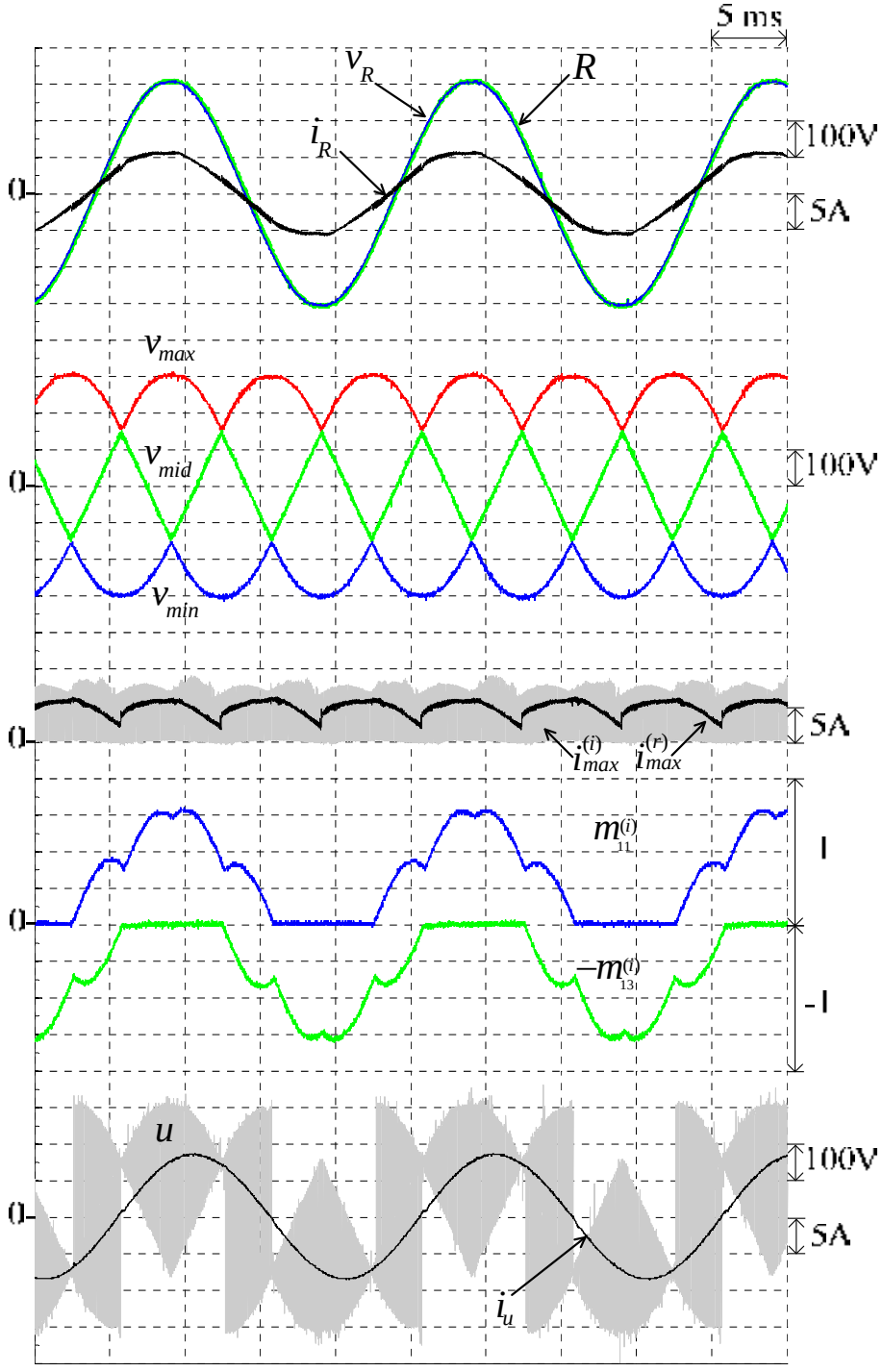



Figure 5.24 Measured waveforms of the prototyped S3L-BTB converter without input power factor compensation at ($M$ = 0.7, $f_o$ = 50 Hz, $k_1 = 0$ )

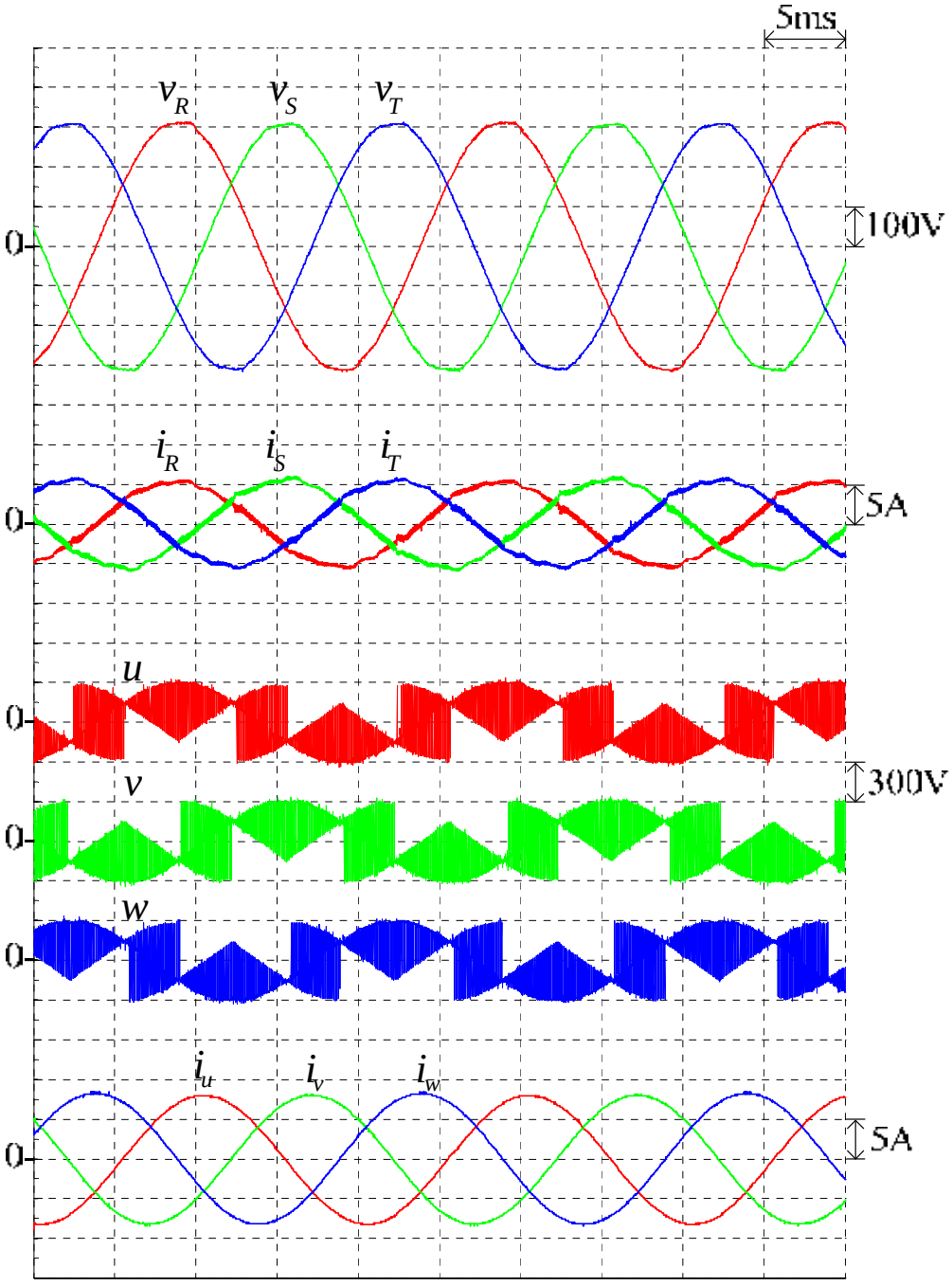



Figure 5.25 Measured input-output waveforms of the prototyped S3L-BTB converter with unity input power factor compensation at ($M$ = 0.7, $f_o$ = 50 Hz, $k_1 = 5$)

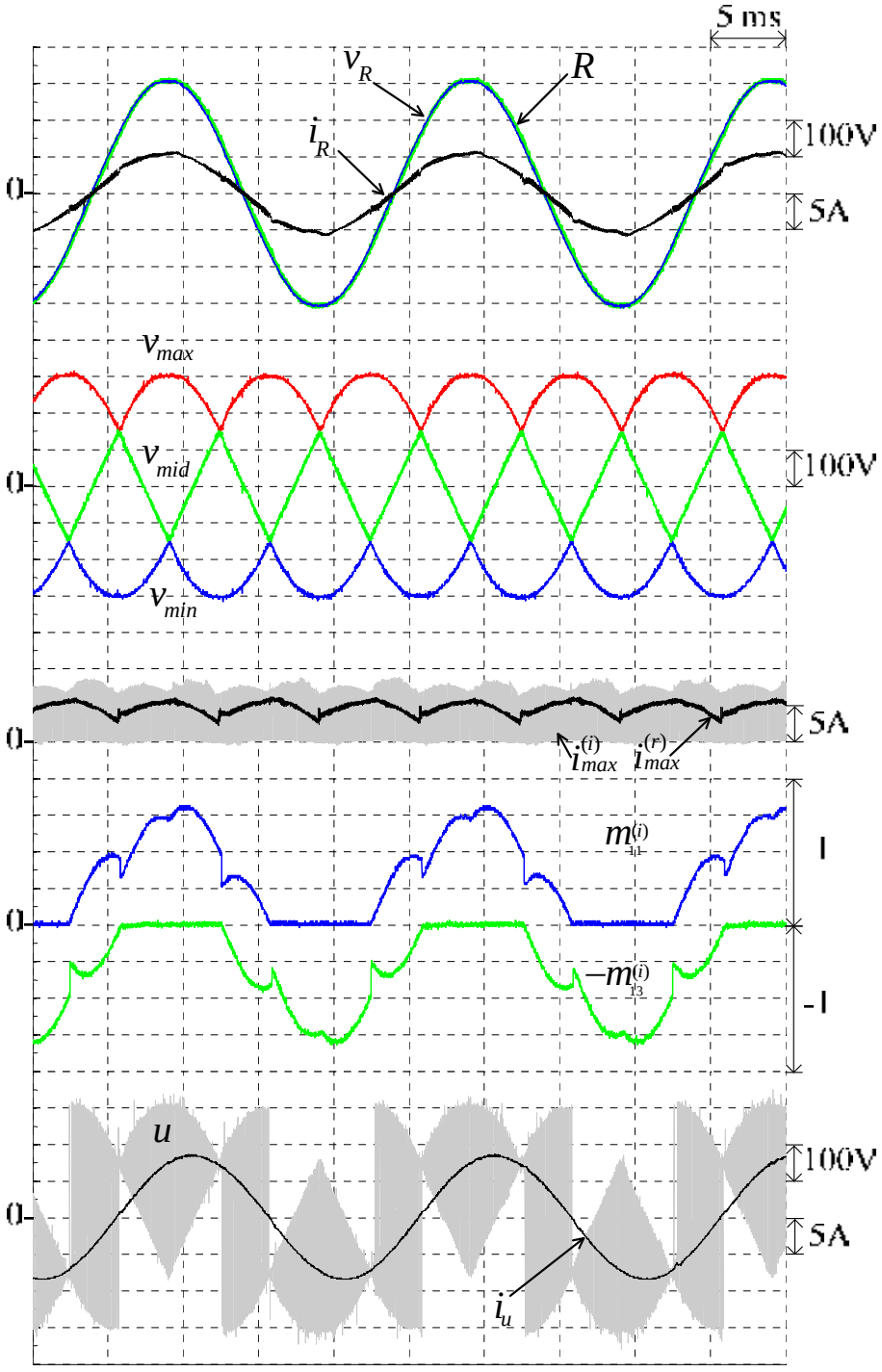



Figure 5.26 Measured waveforms of the prototype S3L-BTB converter with unity input power factor compensation at ($M$ = 0.7, $f_o$ = 50 Hz, $k_1 = 5$)

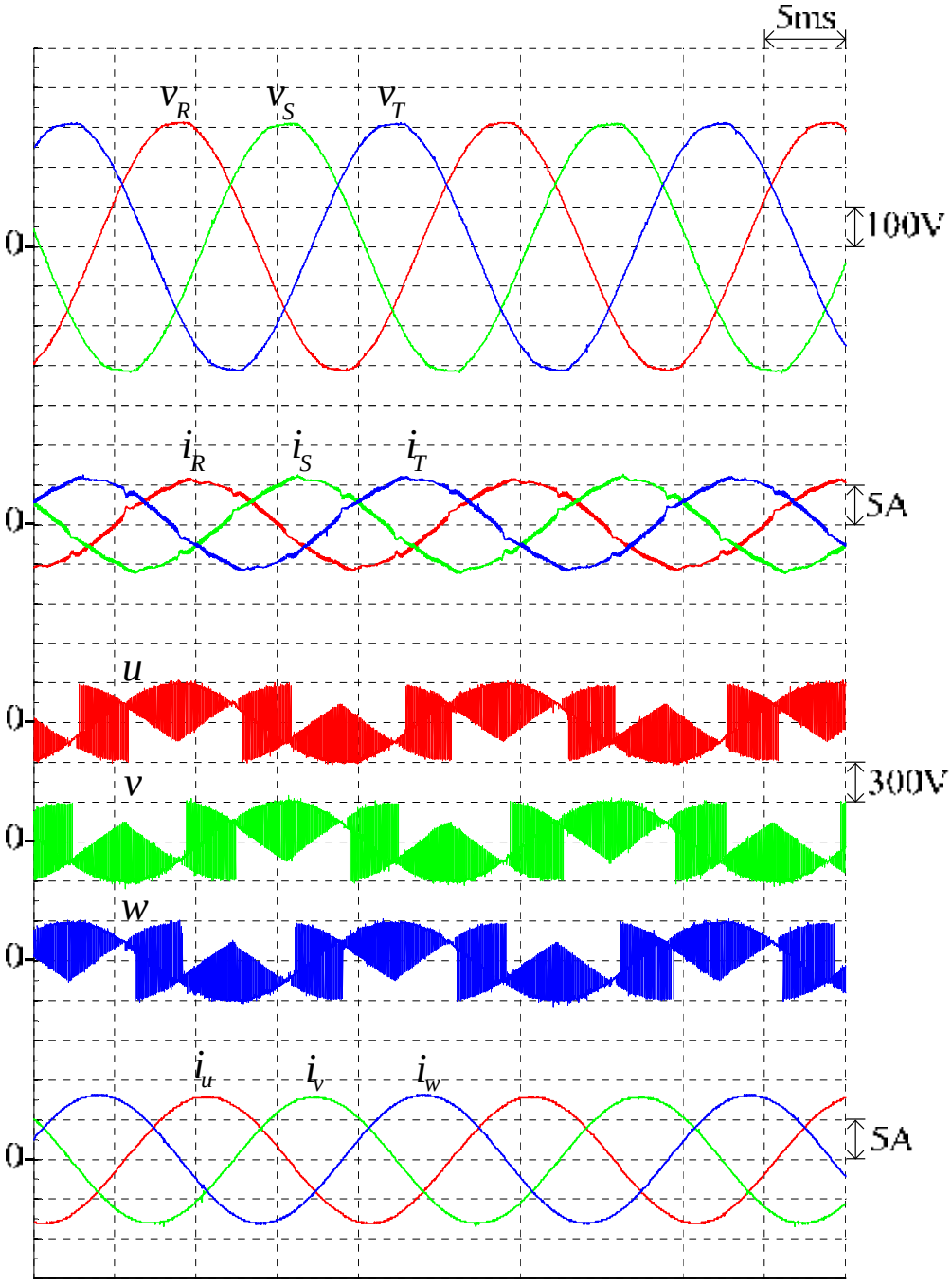



Figure 5.27 Measured input-output waveforms of the prototyped S3L-BTB converter with lagging input power factor compensation at ($M$ = 0.7, $f_o$ = 50 Hz, $k_1 = 15$)

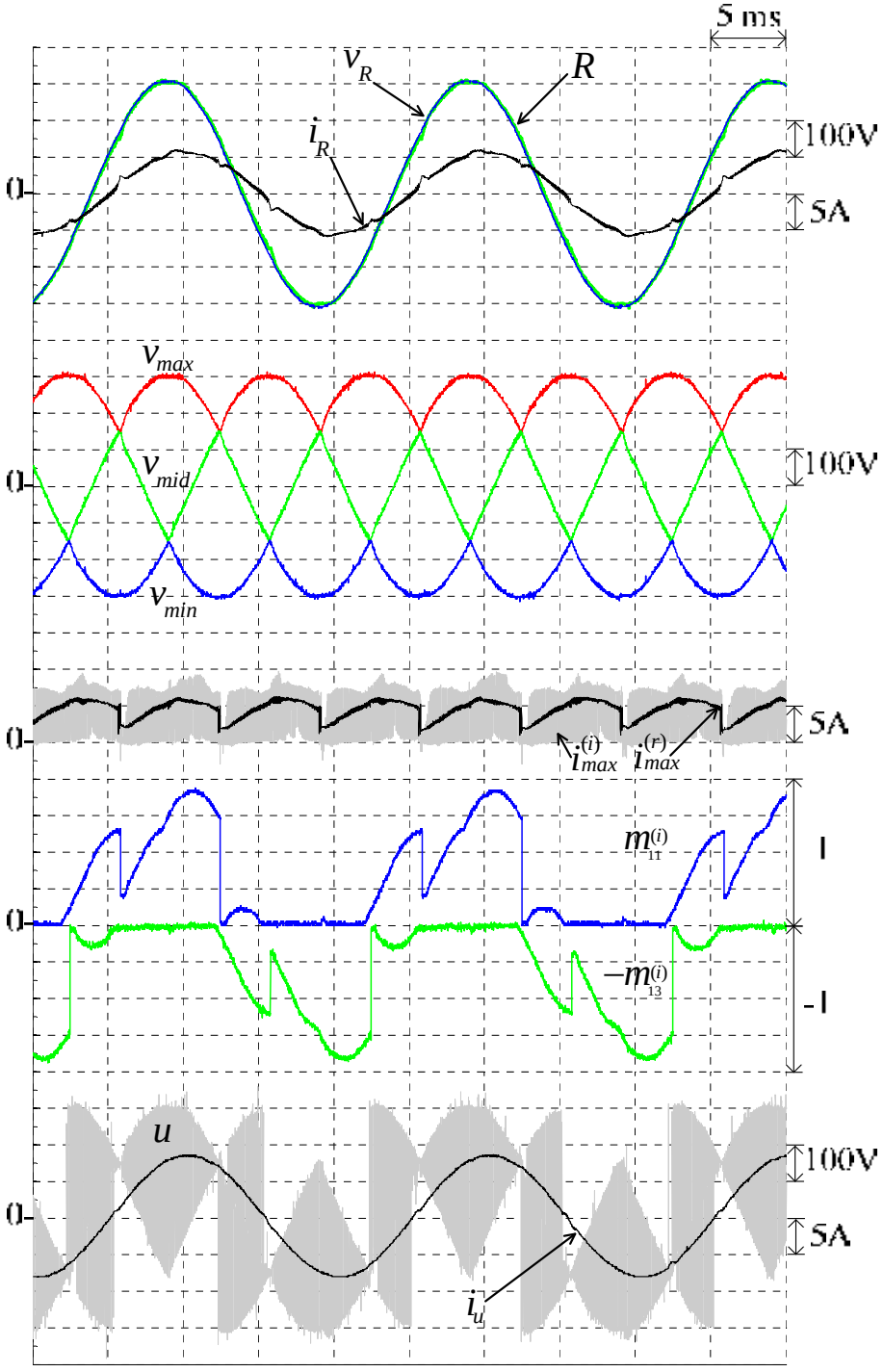



Figure 5.28 Measured waveforms of the prototyped S3L-BTB converter with lagging input power factor compensation at ($M$ = 0.7, $f_o$ = 50 Hz, $k_1 = 15$)

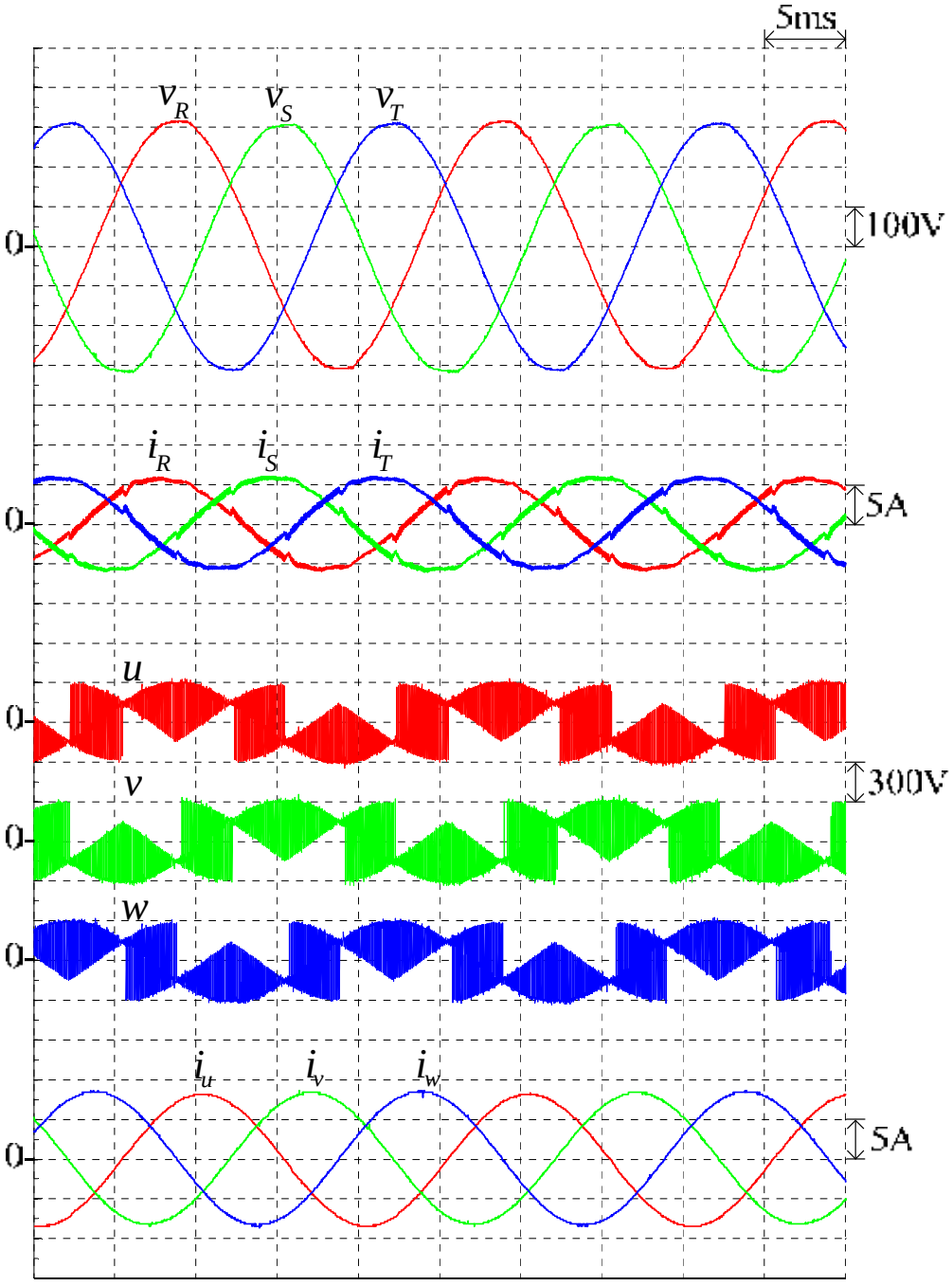



Figure 5.29 Measured input-output waveforms of the prototyped S3L-BTB converter with leading input power factor compensation at ($M$ = 0.7, $f_o$ = 50 Hz, $k_1 = -3.3$)

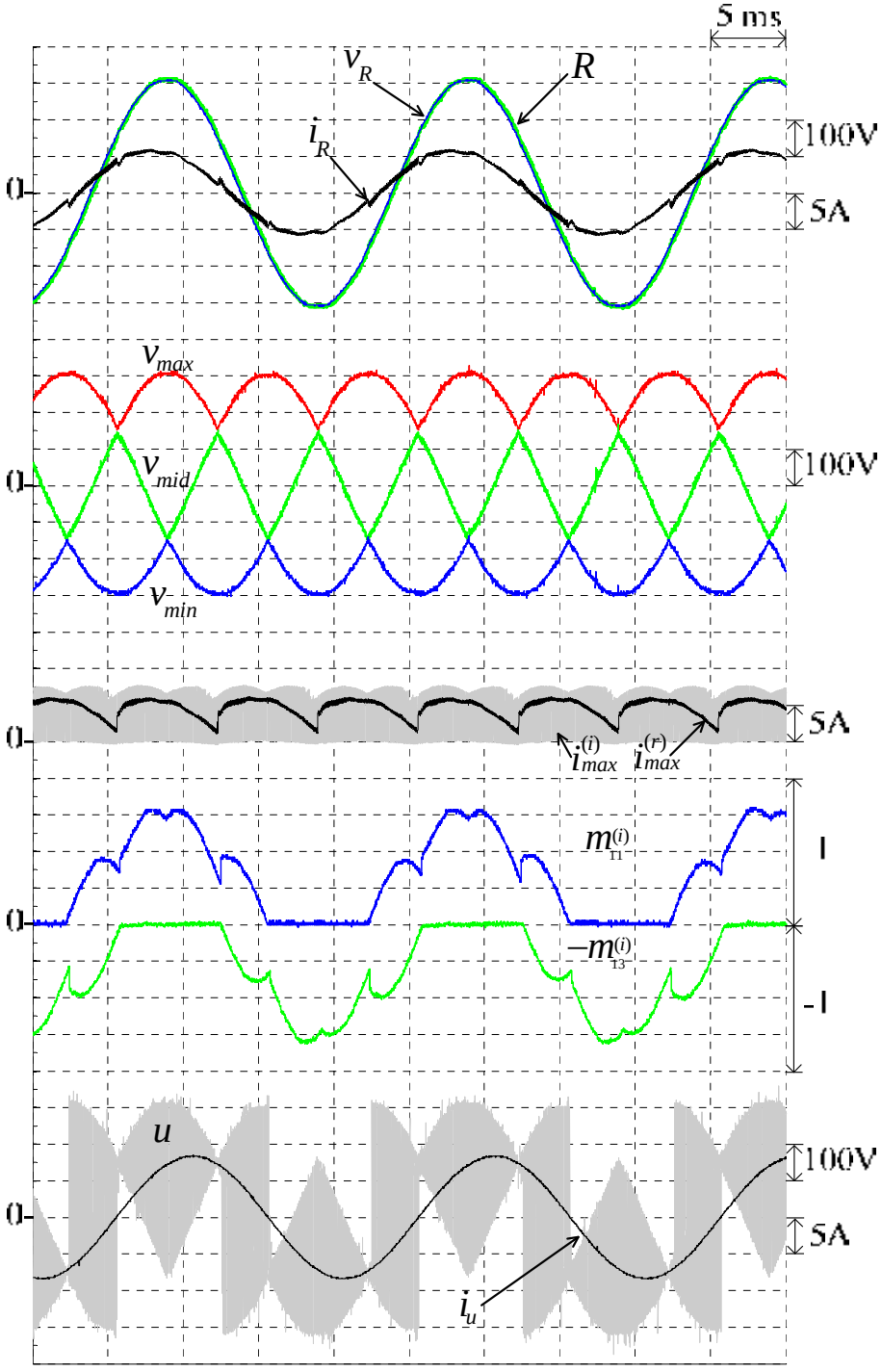



Figure 5.30 Measured waveforms of the prototyped S3L-BTB converter with leading power factor compensation at ($M$ = 0.7, $f_o$ = 50 Hz, $k_1 = -3.3$)

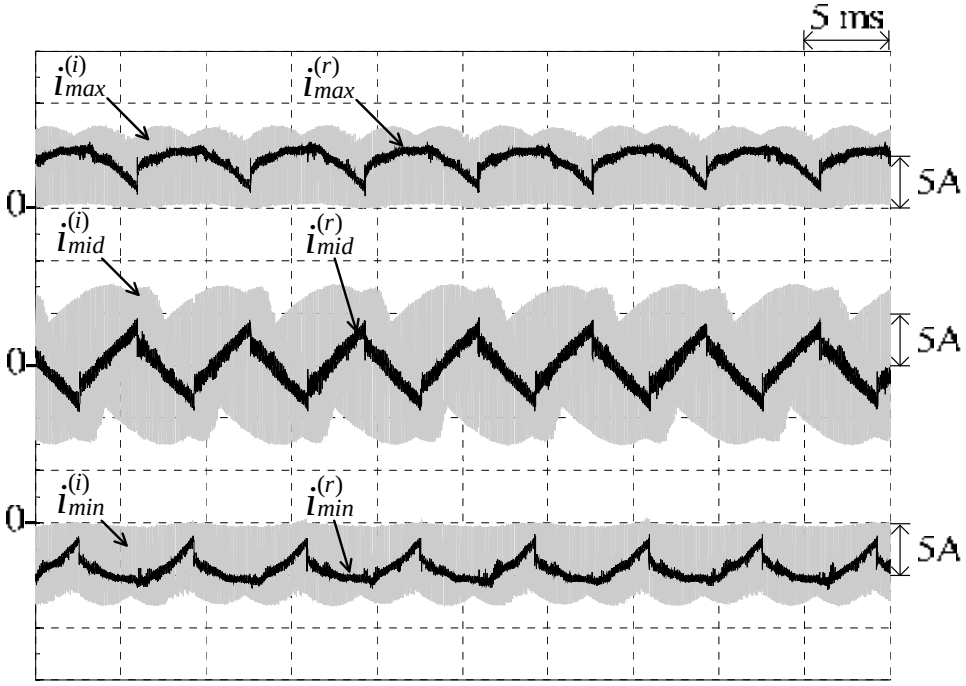



Figure 5.31 Measured dc-link current waveforms of the prototyped S3L-BTB converter without input power factor compensation at ($M$ = 0.7, $f_o$ = 50 Hz, $k_1 = 0$)

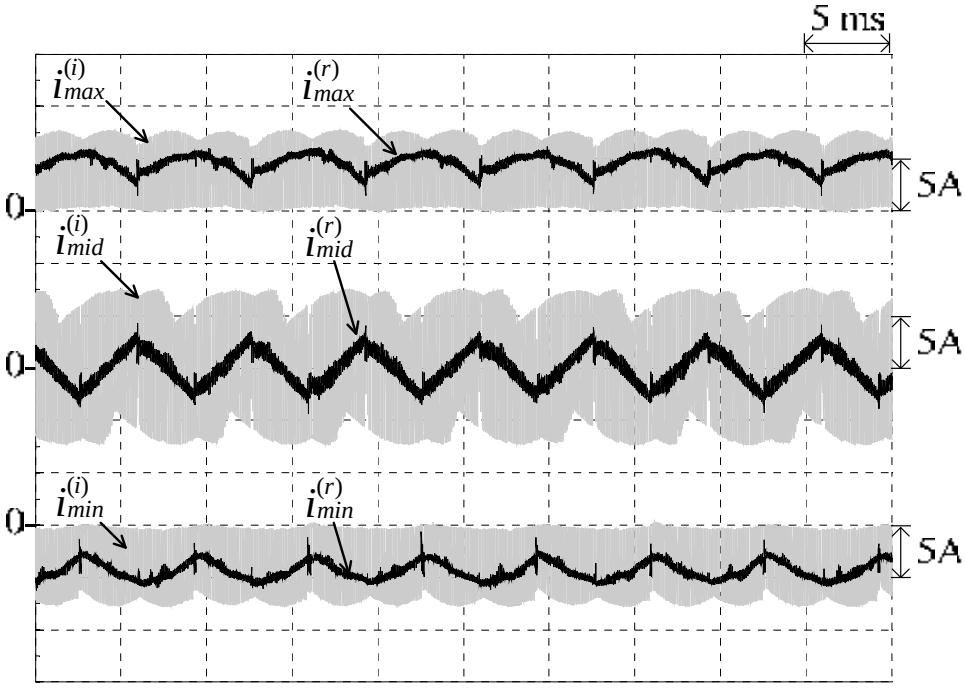



Figure 5.32 Measured dc-link current waveforms of the prototyped S3L-BTB converter with unity input power factor compensation at ($M$ = 0.7, $f_o$ = 50 Hz, $k_1 = -3.3$)

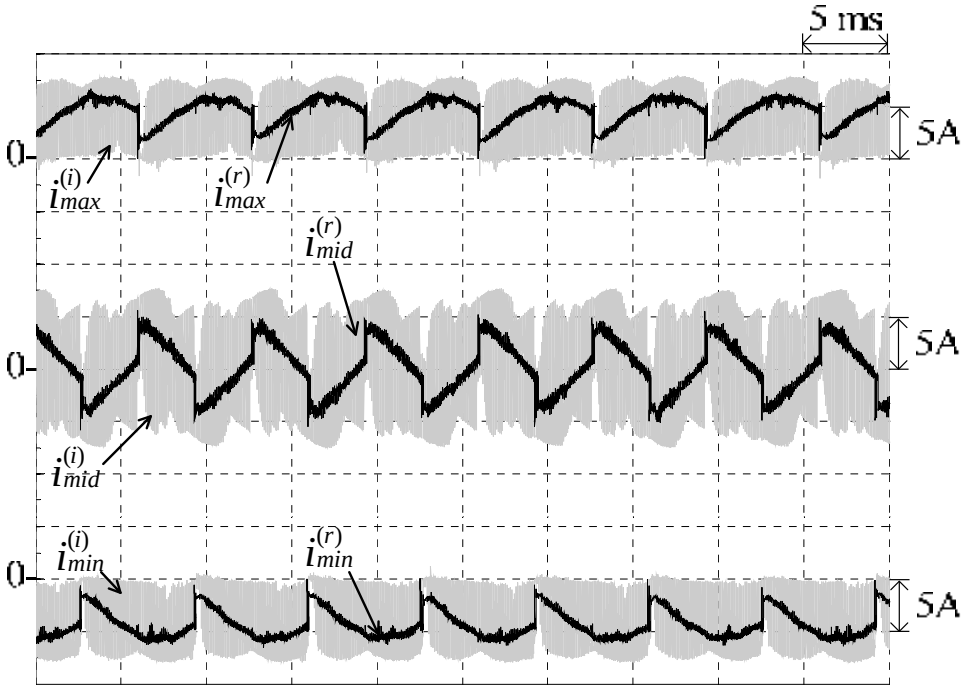



Figure 5.33 Measured dc-link current waveforms of the prototyped S3L-BTB converter with lagging input power factor compensation at ($M$ = 0.7, $f_o$ = 50 Hz, $k_1 = 15$)

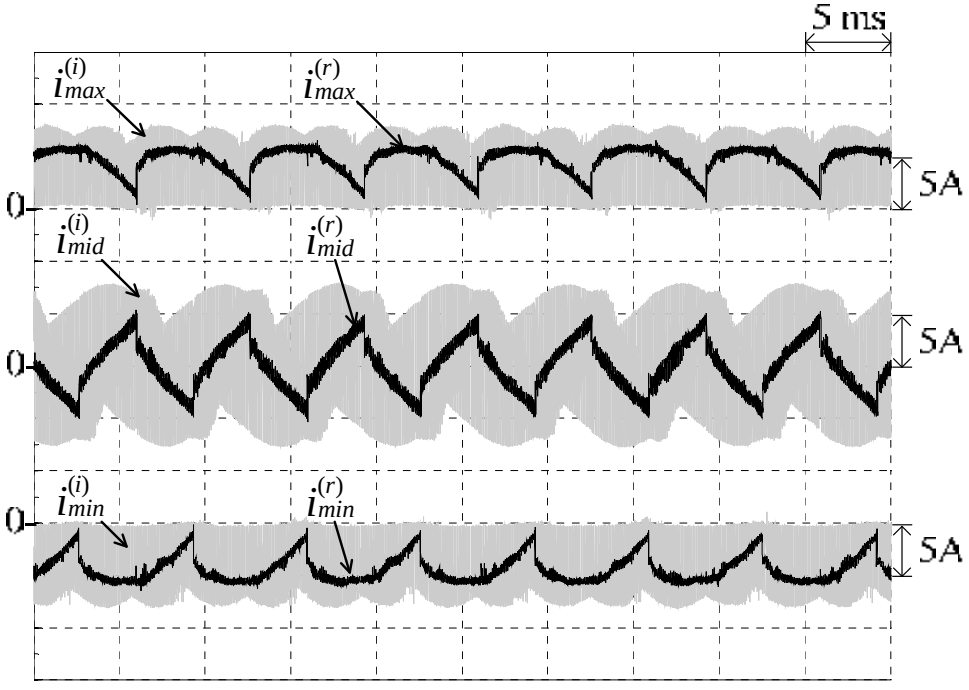



Figure 5.34 Measured dc-link current waveforms of the prototyped S3L-BTB converter with leading input power factor compensation at ($M$ = 0.7, $f_o$ = 50 Hz, $k_1 = -3.3$)

### 5.3.4 **Semiconductor Losses Measurement**

The semiconductor losses of the prototyped converter are measured under the conditions 3 and 4 of Table 5.4. For this purpose, the power meters are installed as shown in Figure 5.12. In order to investigate the reduction of losses to the non-PWM switching, the losses in the input filter which occur in line reactors and the damping resistors are excluded in the measurement. The first power meter and the second one are then installed at the input and output terminals of the front-end rectifier respectively aiming to measure the semiconductor losses in the rectifier. Since the losses in the capacitor network are not significant and can be neglected, the active power measured at the output of the front-end rectifier is approximately equal to the power consumed by the back-end inverter. The last power meter is installed at the output of the inverter to measure the output power and semiconductor losses in the inverter.

Table 5.4 Semiconductor losses in the prototyped S3L-BTB converter

| | $P_1$ | $P_2$ | $P_3$ | Losses in the front-end rectifier ( $P_1 - P_2$) | Losses in the back-end inverter ( $P_2 - P_3$) | Efficiency $(P_3/P_1)*100$ |
|---|---|---|---|---|---|---|
| **Condition 3** | 3.459 kW | 3.422 kW | 3.302 kW | 37 W | 120 W | 95.5% |
| **Condition 4** | 4.081 kW | 4.024 kW | 3.901 kW | 57 W | 123 W | 95.6% |

Table 5.4 shows the results of semiconductor losses in each stage of the constructed S3L-BTB converter. It is clear that the losses in the front-end rectifier are

significantly reduced due to the non-PWM operation. The losses of this stage contribute to only 23% and 32% of the total semiconductor losses of the system under the conditions 4 and 5, respectively. Consequently, the efficiency of the constructed system is at around 95.5%.

# CHAPTER VI
# CONCLUSION AND FUTURE WORK

## 6.1 Conclusion

Based on the double-carrier PWM method for the CMC, This work firstly introduced three-level indirect modulation, of which the rectifier stage and the inverter stage are coupled together with the crucial characteristics of three-level fictitious dc-links. The rectifier stage sort the input voltages into the descending-order voltages. The inverter stage employs those voltages to generate the PWM output voltages with double-carrier PWM method. In this work, the three-level indirect matrix converter (3L-IMC) is newly developed based on the three-level indirect modulation by applying the three-level NPC structure for both the rectifier and the inverter stages. Moreover, this work also presents the symmetrical three-level back-to-back converter (S3L-BTB converter) which is constructed by moving the filter capacitors into the dc-links. Also, the corresponding modulation strategies are proposed for either of them. The proper functions of them as AC/AC converters and the reduction in semiconductor losses are verified by the preliminary simulations and numerical calculation. The results prove that the proposed converters have the capability to vary output voltage, output frequency, to adjust the input power factor, and to work under regenerative mode. In addition, the laboratory prototype of the S3L-BTB converter is constructed using a single FPGA as a controller, and its performances are reconfirmed by the experiments; the experimental results appear to be in good agreement with the simulation results. Moreover, the measured efficiency of the constructed S3L-BTB converter excluding power losses in the filter is about 95.5%, and the semiconductor losses in the rectifier stage are only up to about 30% of the total semiconductor losses of the whole system.

In conclusion, the significant merits of the proposed 3L-BTB converters are listed below.

- Switching losses at the rectifier stage are nearly zero due to the non-PWM operation.

- Switching losses at the inverter stage tend to reduce because the dc-link voltages in the novel 3L-BTB converters are on the average lower than those of the conventional one.
- Smaller input EMI filters can be used as PWM operation is not employed
- Structural compatibility between the S3L-BTB converter and the conventional 3L-BTB converter allows the front-end rectifier stage of the S3L-BTB converter to operate in PWM mode to extend its output voltage range beyond that of the matrix converter, if necessary.
- Unlike the conventional indirect matrix converter, the delta-connected capacitors at the dc link in the S3L-BTB converter can be designed to provide an energy buffer during voltage dips.
- NPC structure is now a commercial building block in the industry, and is applicable to medium and high voltage applications, unlike CMCs.

## 6.2 **Future Works**

Although the concept of the novel 3L-BTB converters is verified and implemented, and the objectives of this thesis are accomplished, there are some issues left to advance as follows:

- The utilization of the free parameter $k_2$ in the inverter modulation matrix to adjust the switching pattern of the PWM output voltages should be studied.
- The regenerative capability of the S3L-BTB converter prototype should be demonstrated to reconfirm the simulation results.
- The hardware implementation of the 3L-IMC should be done. The constraints commutation timing of the rectifier and the inverter stage will be imposed, so the corresponding modulation strategies for each stage must rely on the strict cooperation with each other.
- The optional PWM feature of the rectifier stage of the S3L-BTB should be developed in the prototype so that the S3L-BTB converter can operate as the conventional PWM converter when modulation index exceeds 0.87. Moreover, the on-line change between non-PWM mode and PWM mode should be accomplished.

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# APPENDIX

# APPENDIX A
# NUMERICAL CALCULATION OF SEMICONDUCTOR LOSSES

The mean semiconductor losses of the S3L-BTB converter compared with the conventional PWM 3L-BTB converter are calculated based on the simplified semiconductor model in [15] and [16]. The calculation is done numerically because the analytical calculation for three-level converter is hard to derive and the solutions may be too complicated. Since the switching frequency is much higher than the fundamental frequency of the input and output currents as well as the dc-link voltages, they can be assumed constant during a switching cycle. For simplicity, the calculation for a single leg of the NPC structure is described, and the same principle can be applied further to the other legs.

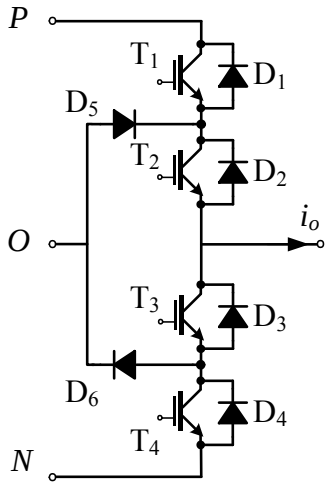


Figure A.1 A three-level neutral-point-clamped structure

## A.1 Conduction Losses

Conduction losses are the power losses occuring in the semiconductor devices which are in the conduction state. The devices having the conduction losses can be easily identified by the current path of the output current $i_o$ for the given output connection as summarized in Table A.1 [16].

Table A.1 Conduction losses of the devices in the NPC structure [16].

| Output connection | Conduction losses |
|---|---|
| $i_o \geq 0$ | |
| $P$ | $P_{\text{cond,T1}}, P_{\text{cond,T2}}$ |
| $O$ | $P_{\text{cond,D5}}, P_{\text{cond,T2}}$ |
| $N$ | $P_{\text{cond,D3}}, P_{\text{cond,D4}}$ |
| $i_o < 0$ | |
| $P$ | $P_{\text{cond,D1}}, P_{\text{cond,D2}}$ |
| $O$ | $P_{\text{cond,T3}}, P_{\text{cond,D6}}$ |
| $N$ | $P_{\text{cond,T3}}, P_{\text{cond,T4}}$ |

To average the conduction losses over one switching period, the conduction period of each device must be known. These can be simply obtained by the calculation of the modulation matrix, which its element represents the duration of the connection between the input dc-links and the outputs. For the proposed 3L-BTB converters, the inverse of the rectifier modulation matrix $\mathbf{M}_r^{-1}$ in Table 3.2 and the inverter modulation matrix $\mathbf{M}_i$ in (3.11) - (3.15) are used for the rectifier and the inverter stages, respectively. For the conventional PWM 3L-BTB converter, the corresponding modulation matrix are given in [19].

Then the conduction losses averaged over one switching period $T_{\text{sw}}$ are weighted with the corresponding duty cycle of each device as seen in (A.1).

$$P_{\text{cond,avg}} = \begin{cases} m_{j1}P_{\text{cond,T1}} + \left(m_{j1} + m_{j2}\right)P_{\text{cond,T2}} + m_{j2}P_{\text{cond,D5}} + m_{j3}P_{\text{cond,D3}} + m_{j3}P_{\text{cond,D4}} & , i_o \geq 0 \\ m_{j1}P_{\text{cond,D1}} + m_{j1}P_{\text{cond,D2}} + (m_{j2} + m_{j3})P_{\text{cond,T3}} + m_{j2}P_{\text{cond,D6}} + m_{j3}P_{\text{cond,T4}} & , i_o < 0 \end{cases} \tag{A.1}$$

where $m_{j1}, m_{j2}, m_{j3}$ represents the duty cycle which each output phase $j^{th}$ is connected to each link $\{P,O,N\}$ respectively during a switching period.

According to (A.1), the averaged conduction losses over a switching period can be calculated if instantaneous conduction losses are known. To avoid the complexity of the non-linear characteristics of the semiconductor devices, the conduction losses of each IGBT $T_k$ and each diode $D_k$ in the single leg of the NPC structure depicted in Figure A.1 can be approximated linearly as (A.2) and (A.3) respectively. The expressions are the function of the current flowing through the devices, which can be easily known through the switching state of each device together with the instantaneous output current.

$$P_{\text{cond},T_k}(i) = V_{\text{f},T_k} \cdot i + r_{\text{f},T_k} \cdot i^2 \tag{A.2}$$

$$P_{\text{cond},D_k}(i) = V_{\text{f},D_k} \cdot i + r_{\text{f},D_k} \cdot i^2 \tag{A.3}$$

Here, $V_{\text{f},T_k}$ and $V_{\text{f},D_k}$ are the threshold voltage of an IGBT and a diode respectively.

$r_{\text{f},T_k}$ and $r_{\text{f},D_k}$ are the differential resistance an IGBT and a diode respectively.

The mean conduction losses over a fundamental period, *T*, then can be found by numerical integration over the fundamental period as shown in (A.4).

$$\bar{P}_{\text{cond}} = \frac{1}{T} \sum P_{\text{cond,avg}} \cdot T_{\text{sw}} \tag{A.4}$$

## A.2 **Switching Losses**

For the calculation of switching losses, similar approach is conducted and starts with the switching loss energy. The switching loss energy for each device depends on the current flowing through the device and the commutation voltage across the device, and is classified as turn-on loss energy and turn-off loss energy. The devices actually exhibiting the switching losses, however, must be determined from the measurement on a test setup in [16]. The results are summarized in Table A.2 for each switching transition and the direction of the output current. To avoid the

complicated models of semiconductor devices, the simplified switching loss models are given in (A.5) - (A.8). The amount of switching loss in a device is assumed to be proportional to the commutation voltage and current flowing through it.

Table A.2 Switching losses of the devices in the NPC structure [16].

| Switching Transition | Loss energies |
|---|---|
| $i_O \geq 0$ | |
| $P \rightarrow N$ | $E_{\mathrm{T1,off}}, E_{\mathrm{T2,off}}, E_{\mathrm{D3,on}}, E_{\mathrm{D4,on}}$ |
| $P \rightarrow O$ | $E_{\mathrm{T1,off}}, E_{\mathrm{D5,on}}$ |
| $N \rightarrow P$ | $E_{\mathrm{T1,on}}, E_{\mathrm{T2,on}}, E_{\mathrm{D3,off}}, E_{\mathrm{D4,off}}$ |
| $N \rightarrow O$ | $E_{\mathrm{T2,on}}, E_{\mathrm{D4,off}}$ |
| $O \rightarrow P$ | $E_{\mathrm{T1,on}}, E_{\mathrm{D5,off}}$ |
| $O \rightarrow N$ | $E_{\mathrm{T2,off}}, E_{\mathrm{D4,on}}$ |
| $i_O < 0$ | |
| $P \rightarrow N$ | $E_{\mathrm{D1,off}}, E_{\mathrm{D2,off}}, E_{\mathrm{T3,on}}, E_{\mathrm{T4,on}}$ |
| $P \rightarrow O$ | $E_{\mathrm{D1,off}}, E_{\mathrm{T3,on}}$ |
| $N \rightarrow P$ | $E_{\mathrm{D1,on}}, E_{\mathrm{D2,on}}, E_{\mathrm{T3,off}}, E_{\mathrm{T4,off}}$ |
| $N \rightarrow O$ | $E_{\mathrm{T4,off}}, E_{\mathrm{D6,on}}$ |
| $O \rightarrow P$ | $E_{\mathrm{D1,on}}, E_{\mathrm{T3,off}}$ |
| $O \rightarrow N$ | $E_{\mathrm{T4,on}}, E_{\mathrm{D6,off}}$ |

$$E_{\mathrm{T_k,on}}(v,i) = \frac{E_{\mathrm{T_k,on,n}}}{V_{\mathrm{n}} I_{\mathrm{n}}} v \cdot i \tag{A.5}$$

$$E_{\mathrm{T_k,off}}(v,i) = \frac{E_{\mathrm{T_k,off,n}}}{V_{\mathrm{n}} I_{\mathrm{n}}} v \cdot i \tag{A.6}$$

$$E_{\mathrm{D_k,on}}(v,i) = \frac{E_{\mathrm{D_k,on,n}}}{V_{\mathrm{n}} I_{\mathrm{n}}} v \cdot i \tag{A.7}$$

$$E_{\mathrm{D_k,off}}(v,i) = \frac{E_{\mathrm{D_k,off,n}}}{V_{\mathrm{n}} I_{\mathrm{n}}} v \cdot i \tag{A.8}$$

where $E_{T_k,on,n}$, $E_{T_k,off,n}$ are the turn-on loss energy and the turn-off loss energy given in the device datasheet, measured at a given commutation voltage $V_n$ and current $I_n$ for each IGBT.

$E_{D_k,on,n}$, $E_{D_k,off,n}$ are the turn-on loss energy and the turn-off loss energy given in the device datasheet, measured at a given commutation voltage $V_n$ and current $I_n$ for each diode.

It should be noted that turn-off loss energy in diodes is caused by the reverse recovery effect when diodes are forced to turn off. Still, the turn-on loss energy is small and is always neglected in the device datasheet [20].

For determined PWM switching patterns, the switching losses averaged over a switching period is expressed in (A.9).

$$P_{sw,avg} = \frac{1}{T_{sw}} \cdot \left( \sum_{k=1}^{4} \left( E_{T_k,on} + E_{T_k,off} \right) + \sum_{k=1}^{6} \left( E_{D_k,on} + E_{D_k,off} \right) \right) \tag{A.9}$$

The mean conduction losses over a fundamental period, *T*, then can be found by numerical integration over the fundamental period as shown in (A.10).

$$\bar{P}_{cond} = \frac{1}{T} \sum P_{sw,avg} \cdot T_{sw} \tag{A.10}$$

Although the conduction loss and switching loss model described so far seem incomplete, the error of the results are not significant and are acceptable for demonstrating loss comparison between different power converter topologies as seen in many researches such as [15] and [16].

## A.3 Loss Parameter of the 3L-NPC module SKM20ML1066

In Chapter IV, the semiconductor losses of the S3L-BTB converter and the conventional PWM 3L-BTB converters are calculated based on the 3L-NPC module

SKM20ML1066 with the above calculation approach. The required parameters of the power module are listed in Table A.3.

Table A.3 Parameters of the 3L-NPC module SEMIKRON SKM20ML1066

| IGBTs |
|---|
| $V_{f,T_k} = 0.9$ V, $r_{f,T_k} = 27.5$ mΩ, |
| $E_{T_k,on,n} = 0.4$ mJ , $E_{T_k,off,n} = 1.07$ mJ when $V_n = 300$ V, $I_n = 20$ A |
| Anti-parallel diodes (k = 1,2,3,4) |
| $V_{f,D_k} = 1$ V, $r_{f,D_k} = 30$ mΩ, |
| $E_{D_k,off,n} \approx 0$ , $E_{D_k,off,n} = 0.2$ mJ when $V_n = 300$ V, $I_n = 20$ A |
| Clamping diodes (k = 5,6) |
| $V_{f,D_k} = 1$ V, $r_{f,D_k} = 20$ mΩ, |
| $E_{D_k,off,n} \approx 0$ , $E_{D_k,off,n} = 0.2$ mJ when $V_n = 300$ V, $I_n = 20$ A |

# Biography

Korawich Niyomsatian was born on February 23, 1989, in Bangkok, Thailand. He received B.Eng from Chulalongkorn University in 2011. He has been working towards a master degree in the department of electrical engineering at Chulalongkorn University since 2011. His current research interests include matrix converters, back-to-back converters and PWM technique.

## Publications

1) K. Niyomsatian, S. Samermurn, S. Suwankawin and S. Sangwongwanich. Novel topologies for three-level back-to-back converters based on matrix converter theory. Proc. Annual Conference on IEEE Industrial Electronics Society, 6099-6104. Montreal: 2012.
2) S. Samermurn, K. Niyomsatian, S. Suwankawin and S. Sangwongwanich. Front-End Power Factor Control of Novel Three-Level Back-to-Back Converters Based on Matrix Converter Theory. Proc. The 35th Electrical Engineering Conference (EECON 35), 401-404 vol.1 Thailand: 2012.
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