เอกสารอ้างอิง

1. สุทัศน์ ลีฬหะพันธุ์ " การพัฒนาเครื่องจ่ายไฟฟ้าแรงสูงสำหรับหัววัดรังสีนิวเคลียร์ " วิทยานิพนธ์ ปริญญามหาบัณฑิต ภาควิชานิวเคลียร์เทคโนโลยี บัณฑิตวิทยาลัย จุฬาลงกรณ์ มหาวิทยาลัย ปี พ.ศ. 2520
2. ไพบูลย์ นาลนิล " การพัฒนาเครื่องวิเคราะห์สเปคตรัมขนาดเบาแบบสี่ช่อง " วิทยานิพนธ์ ปริญญามหาบัณฑิต ภาควิชาวิศวกรรมไฟฟ้า บัณฑิตวิทยาลัย จุฬาลงกรณ์ มหาวิทยาลัย ปี พ.ศ. 2527.
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ภาคผนวก ก

ก.1 แหล่งจ่ายไฟฟ้ากระแสตรงค่าคงที่ $\pm$ 12 โวลต์ จากวงจรรูปที่ 3.3

กำหนดให้

ความต่างศักย์ (V_{out}) = $\pm$ 12 โวลต์

กระแสโหลดสูงสุด I_{lmax} = 1 แอมแปร์

การปรับโหลด (load requlation) ของ ไอซี U_1 และ U_2 คือ 66% เลือกขดทุติยภูมิ N_{s2} ของหม้อแปลง T_1 เป็นแบบมีแทปกลาง 12-0-12 โวลต์

ไอซี U_1 ,U_2 คือ LM 7812 และ LM 7912 ตามลำดับ

ถ้าให้ ไอซี U_1 เป็นเหมือนความต้านทาน R จะได้วงจรฟิลเตอร์ แบบ RC ฟิลเตอร์

จากสูตร

$$V_{out} = \frac{X^2_c \, 2 \, I}{R} \qquad \text{.....(1)}$$

เมื่อ

X_c คือ รีแอกแตนซ์ชนิดความเหนี่ยวนำ

$$R = \frac{V_{in} - V_{out}}{I_L}$$

$$V_{in} = \sqrt{2} \times 12$$

$$= 16.97 \quad \text{โวลต์}$$

$$\text{จะได้ } R = \frac{16.97 - 12}{1}$$

$$= 4.97 \quad \text{โอหม์}$$

ให้ความต่างศักย์ทางออกมีแรงดันระลอกคลื่น(V_r) 50 x 10^{-3} โวลต์ แทนค่าในสมการ (1)

$$X_c = \sqrt{\frac{V_r R}{\sqrt{2}\, I}}$$

$$= \sqrt{\frac{50 \times 10^{-3} \times 4.97}{1.414 \times 1}}$$

$$= .419 \quad \text{โอห์ม}$$

จากสูตร

$$C = \frac{1}{2 f X_c}$$

$$= \frac{1}{2 \times 3.14 \times 100 \times 0.419}$$

$$= 3798 \times 10^{-6} \quad \text{ฟารัด}$$

เลือก = C_{2-5} ค่า 4700 ไมโครฟารัด

D_{5-8} (IN 4002)

ก. 2 **วงจรควบคุมแบบสวิตชิง**[1]

จากวงจรรูปที่ 3.4

ตัวเหนี่ยวนำ L_1 และตัวเก็บประจุ C_7 ต่อเป็นวงจรฟิลเตอร์

จาก $V_1 = L\, di/dt$ .....(2)

จะได้ $V_1 = E_{in} - E_{out}$

$di = I_L$

แทนค่าในสมการ (2)

$$L = \frac{(E_{in} - E_{out})\Delta t}{I_L} \quad .....(3)$$

หรือ

$$L = \frac{V_{out}\ T_{off}}{0.25 I_{out}} \quad .....(4)$$

โดย $$T_{off} = \frac{1}{2}\left[\frac{1-(E_{out}/E_{in})}{f}\right] \quad \text{.....(5)}$$

โดย

L คือ ตัวเหนี่ยวนำ

I_L คือ กระแสที่เปลี่ยนแปลง

V_{in} คือ ความต่างศักย์ทางออก

T_{off} คือ ช่วงเวลาปิด

กำหนดให้

V_{in} = 40 โวลต์

V_{out} = 15 โวลต์

I_{lmax} = 0.4 I_L

f = 55×10^3 เฮิรตซ์

V_{p-p} = 10% V_{out}

แทนค่าในสมการ (5)

$$T_{off} = \frac{1}{2}\left[\frac{1 - (15/40)}{55 \times 10_3}\right]$$

$$= 5.68 \times 10^{-6} \quad \text{วินาที}$$

แทนค่าในสมการ (4)

$$L_1 = \frac{15 \times 5.68 \times 10^{-6}}{0.25 \times 1.5}$$

$$= 227 \quad \text{ไมโครเฮนรี}$$

จากสูตร C ฟิลเตอร์ทางออก

จะได้ $$C_7 = \frac{V_{out} \quad (V_{in} - V_{out}) \quad T^2}{8 \; L_1 \; V_{in} \quad V_{p-p}}$$

$$= \frac{15(40-15)\ (1/55x10^3)^2}{8 \times 227 \times 10^{-6} x\ 40 \times 15x\ .1}$$

$$= 1.1 \quad \text{ไมโครฟารัด}$$

คำนวณหาขนาดของ L_1 เลือกใช้แกนชนิดเฟอร์ไรต์ชนิด 2C3 มีความเข้มสนามแม่เหล็กสูงสุด

(B_{max}) = 3700 เกาส์

ใช้ความหนาแน่นกระแสไฟฟ้า 500 เซอร์คูลามิล/แอมแปร์

จะได้ขนาดของลวดที่ใช้ (D) = ความหนาแน่นกระแส x กระแส

= 500 x 1.5

= 750 เซอร์คูลามิล

จากตารางจะได้ขนาดลวด D = .0314 นิ้ว

จากสูตร

$$A_e A_c = \frac{5.067 \times 10^8 \times L \times I_L \times D^2}{0.8\ Bmax}$$

$$= 5.067 \times 10^8 \times 277 \times 10^{-6} \times 1.5 \times 0.0314^2$$

$$= 0.07 \quad cm^4$$

เลือกใช้แกน Tomita Ferrite

EI 22 ซึ่งมี $A_e A_c$ = 0.16 cm^4

Q_3 ใช้ MOSFET เบอร์ MTP 8N20, V_{DSS} = 200 โวลต์ 8 แอมแปร์

D_{12} ใช้ ซอตส์กีไดโอด เบอร์ MUR 810

ก. 3.1 **<u>วงจรควบคุมแบบสวิตชิง</u>**

ก.3.1 ความถี่ของวงจรพัลส์วิดธ์มอดูเลเตอร์

จากสมการ 3.2

$$f_{osc} = 1.1 / (R_T.C_T)$$

กำหนดให้

f_{osc} = 10 กิโลเฮิรตซ์

C_T = .022 ไมโครฟารัด

ได้ $R_T = 1.1/(10^3 \times .022^{-6})$

$R_T = R_{52} + R_{53}$ = 5000 โอห์ม

วงจรขับแบบ พุช-พูล Q_{5-6} ใช้ MOSFET

(MTP 8N20) ทนกระแสได้ 8 แอมแปร์ , V_{DSS} = 200 V

ก.3.2 **หม้อแปลง**

จากวงจรรูปที่ 3.6

หม้อแปลง T_2 เลือกใช้ชนิดแกนเฟอร์ไรต์ H7c1 TDK EI - 50

พื้นที่หน้าตัดแกน A_e = 2.3 cm^2

พื้นที่สำหรับพันลวด A_c = 2.463 cm^2

จากสูตร

$$N_p = \frac{(V_p)\ 10^8}{4\ f\ B_{max}\ A_e}$$

ให้ V_p = 15 โวลต์

f = 10×10^3 เฮิรตซ์

B_{max} = 2000 เกาส์

A_e = 2.3 cm^2

$$N_p = \frac{15 \times 10^8}{4 \times 10 \times 10^3 \times 2.3 \times 2000}$$

= 8.15 รอบ

เลือกใช้ N_p = 10 รอบ

$$N_s = \frac{N_p\ Vs}{Vp}$$

ต้องการ V_s = 1600 โวลต์

$$N_s = \frac{10 \times 1600}{15}$$

= 1066.67 รอบ

เลือกใช้ N_s = 1100 รอบ

ก.3.3 **วงจรป้องกัน**

วงจรป้องกันเมื่อใช้โหลดเกิน ใช้ไอซีเบอร์ MC34061

จุดทำงานของไอซีคำนวณได้จาก สมการ 3.6

$$V_{trip} = \frac{2.5\ (R_{17} + R_{18})}{R_{17}}$$

กำหนดให้

V_{trip} = 12 โวลต์

R_{17} = 2000 โอห์ม

จะได้ R_{18} = ((12 x 2000)/2.5) - R_{17}

= 7600 โอห์ม

ก.4 การคำนวณหา Resolution

จากสูตร Resolution = $\frac{\text{FWHM X 100}}{E_c}$ %

E_c = centroid channel

ก.4.1 คำนวณหา Resolution จากสเปคตรัมรูปที่ 4.16

E_c = 401

FWHM = 69

ได้ Resolution = (69/401) x 100

= 17.2 %

ก.4.2 คำนวณ Resolution จากสเปคตรัม รูปที่ 4.17

E_c = 394

FWHM = 71

ได้ Resolution = (71/394) x 100

= 18.00 %

ก.4.3 คำนวณหา Resolution จากสเปคตรัม รูปที่ 4.18

E_c = 692

FWHM = 81

ได้ Resolution = (81/692) x 100

= 11.7 %

ก.4.4 คำนวณ Resolution จากสเปคตรัมรูปที่ 4.19

E_c = 642

FWHM = 95

ได้ Resolution = (95/642) x 100

= 14.8 %

ก.4.5 คำนวณ Rsolution จากสเปคตรัม รูปที่ 4.20

E_c = 459

FWHM = 314

ได้ Resolution = (314x459) x 100

= 68.4 %

ก.4.6 คำนวณ Resolution จากสเปคตรัม รูปที่ 4.21

E_c = 469

FWHM = 315

ได้ Resolution = (315/469) x 100

= 67.1 %

ก.4.7 คำนวณหา Resolution จากสเปคตรัมรูปที่ 4.22

E_c = 364

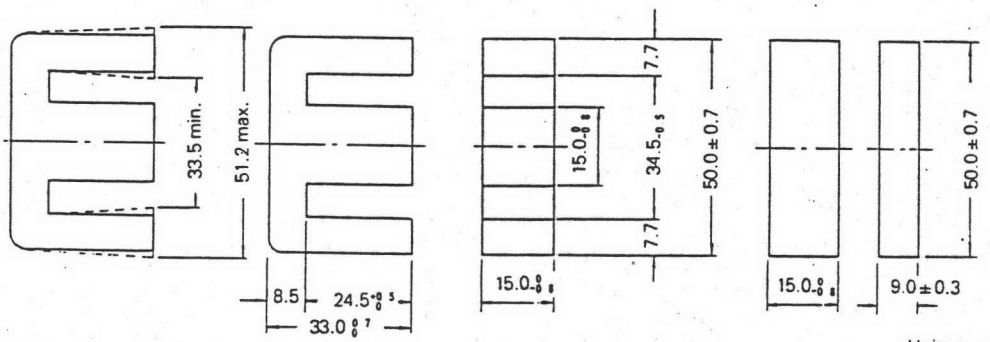
FWHM = 71

ได้ Resolution = (71/364) x 100

= 19.5 %

EI 50 CORE

EI 50 core



Unit: mm

Parameter

Core constant	C_1 mm^{-1}	0.411
Effective magnetic path length	$l_e$mm	94.0
Effective cross-sectional area	A_e mm²	230
Effective core volume	$V_e$mm³	21600
Cross-sectional center leg area	A_{cp}mm²	213
Minimum cross-sectional area	A min. mm²	201.6
Cross-sectional winding area of core	A_{cw}mm²	246.3
Weight (approx.)	g	115

Ordering code	Al-value (nH/n²)		Power loss (25kHz, 2000G*)		
	1kHz, 0.5mA	25kHz, 2000G*	25°C	60°C	100°C
H_{7c1} EI 50-Z (Gap 0)	3960 min.	9170 min.	<3.3W	<2.3W	<3.1W
H_{7c1} EI 50-P	137 ±10%				
H_{7c1} EI 50-R	275 ±10%				
H_{7c1} EI 50-T	550 ± 10%				
H_{7c1} EI 50-V	820 ± 10%				

**sine wave*

Calculated output power (P_{out}) (forward converter mode)

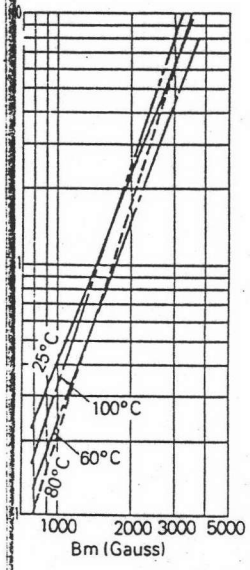
Frequency	25kHz	50kHz	100kHz
P_{out}	193W	301W	444W

input voltage: 100VAC (E_{in} = 141VDC)
output voltage E_{out}: 5VDC
ΔT_{up}: 40°C (ambient temp.; 60°C)
n(= N_P/N_S): 6.5
K_{cu}: 0.24

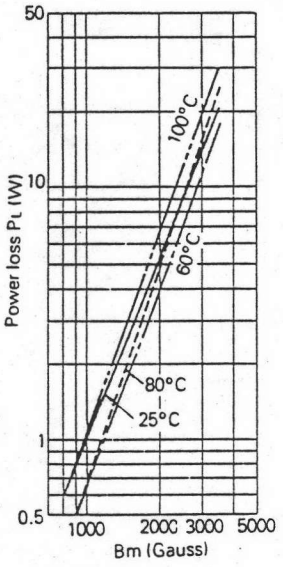
ower loss* vs. Flux density for H_{7c1} EI 50 (Typical)

*sine wave data
Test circuit, see page 10 (Fig. 6)

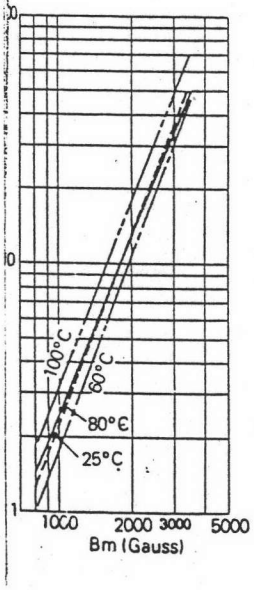
25KHz



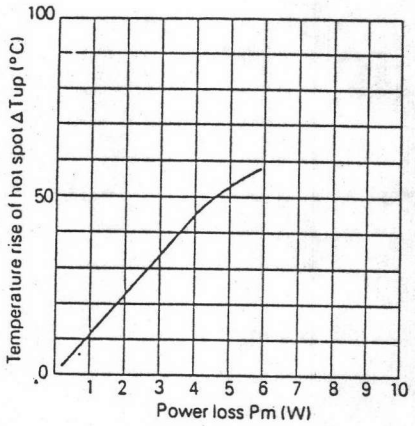
at 50KHz

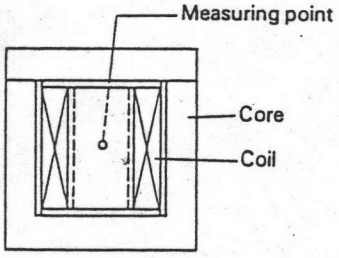


100KHz



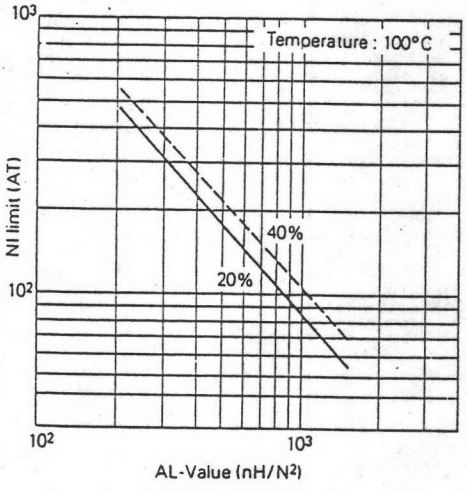
Temperature rise vs. Power loss for H7C1 EI 50 (Typical) (ambient temperature: 25°C)





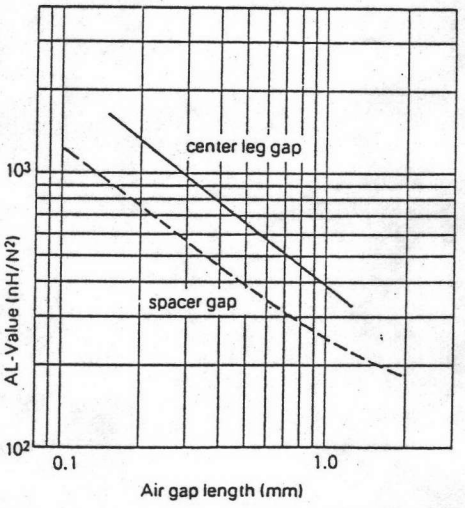
Note: The temperature rise is measured in the room which temperature and humidity are fixed to 25°C and 45% RH. (approx. 400×300×300cm)

NIlimit vs. AL-value for H7C1 EI 50 gapped core (Typical)



Note: NIlimit shows the point that the exciting current is 20% and 40% away from its extended linear part.

AL-value vs. Air gap length for H7C1 EI 50 core (Typical)



Measuring conditions
- *Coil: φ0.35 2UEW 100Ts*
- *Frequency: 10kHz*
- *Level: 0.5 mA*

MOTOROLA

MC34061
MC34061A

Advance Information

THREE-TERMINAL OVERVOLTAGE "CROWBAR" SENSING CIRCUIT

The MC34061,A overvoltage protection (OVP) circuit, in combination with two external programming resistors and a "crowbar" SCR, protects sensitive electronic circuitry from overvoltage damage. It senses an overvoltage condition and quickly "crowbars," or short circuits, the supply. An external capacitor may be used to program a minimum overvoltage duration before tripping, thus providing noise immunity.

This three-terminal circuit provides a cost-effective means of protecting either positive or negative power supplies. The unique design of the MC34061,A eliminates trip voltage and temperature drift errors due to SCR gate variations.

The basic MC34061,A device offers a ±2% tolerance on the sense trip voltage. The A-suffix device has a ±1% sense trip voltage specification and other key parameters have tightened limits. The device is available in a low-cost plastic package and features:

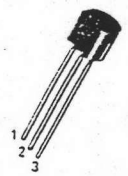
age and features:

- Unique Three-Terminal Design
- SCR Gate Drive Output of 200 mA
- Sense Voltage of 2.5 V ±1% or ±2%
- Hysteresis of 250 mV
- Wide Supply Range: 4.0 V ≤ V_{CC} ≤ 41 V

THREE-TERMINAL PROGRAMMABLE OVERVOLTAGE SENSING CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

P SUFFIX
PLASTIC PACKAGE
CASE 29-04



Pin 1. V_{CC}
2. Drive Output
3. Sense

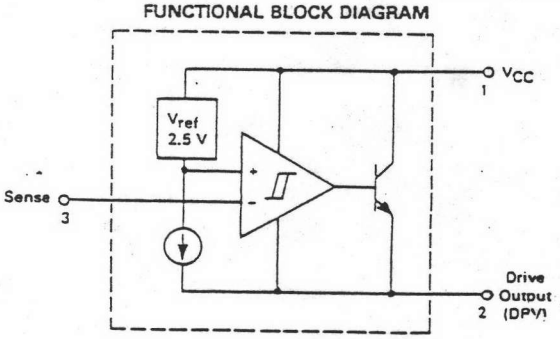
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Operating Voltage	$V_{CC} - V_{DRV}$	40	Vdc
Sense Voltage	V_{Sense}	40	Vdc
Drive Output Current	I_{DRV}	Internally Limited	mA
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ORDERING INFORMATION

Device	Temperature Range	Package
MC34061P,AP	0 to −70° C	Plastic TO-92

FUNCTIONAL BLOCK DIAGRAM



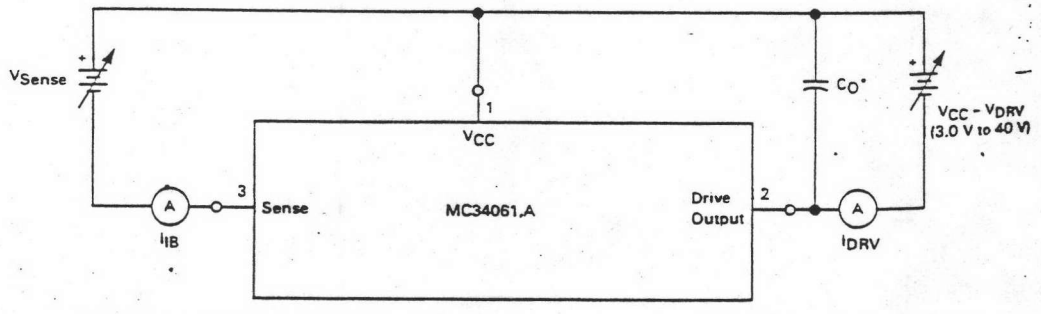
This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS ($V_{CC} - V_{DRV}$ = 5.0 V; T_A = T_{low} to T_{high} [see Note 1] unless otherwise specified)

Characteristic	Symbol	MC34061A			MC34061			Unit
		Min	Typ	Max	Min	Typ	Max	
Operating Voltage Range	$V_{CC} - V_{DRV}$	3.0	—	40	3.0	—	40	Vdc
Sense Trip Voltage T_A = 25°C T_{low} to T_{high} (Note 1)	V_{Sense}	 2.475 2.45	 2.5 2.5	 2.525 2.55	 2.45 2.4	 2.5 2.5	 2.55 2.6	Vdc
Line Regulation, V_{Sense} (3.0 ≤ $V_{CC} - V_{DRV}$ ≤ 40 V) T_A = 25°C T_{low} to T_{high} (Note 1)	Reg_{line}	 — —	 0.001 0.001	 0.005 0.01	 — —	 0.001 0.001	 0.01 0.02	%/V
Input Bias Current, Sense Pin At Trip Point (Note 2) After Trip (V_{Sense} = 3.0 V)	I_{IB}	 — —	 0.3 0.9	 1.0 3.0	 — —	 0.3 0.9	 2.0 6.0	μA
Hysteresis Voltage, Sense Pin	V_H	—	250	—	—	250	—	mV
Drive Output Current, ON State T_J = 25°C T_{low} to T_{high} (Note 1)	$I_{DRV(on)}$	 130 90	 200 —	 300 350	 130 90	 200 —	 300 350	mA
Drive Output Current, OFF State $V_{CC} - V_{DRV}$ = 5.0 V 3.0 V ≤ $V_{CC} - V_{DRV}$ ≤ 40 V	$I_{DRV(off)}$	 0.2 0.2	 0.6 0.6	 1.0 1.5	 0.2 0.2	 0.6 0.6	 1.0 1.5	mA
Drive Output Current Slew Rate T_A = 25°C	di/dt	—	2.0	—	—	2.0	—	A/μs
Drive Output V_{CC} Transient Rejection $V_{CC} - V_{DRV}$ = 0 V to 15 V at dV/dt = 200 V/μs; V_{Sense} = 0 V; T_A = 25°C	$\Delta I_{DRV(trans)}$	—	1.0	—	—	1.0	—	mA (Peak)
Propagation Delay Time (T_A = 25°C) 500 mV Overdrive	t_{PLH}	—	500	—	—	500	—	ns

NOTES:
(1) T_{low} to T_{high} = 0°C to 70°C
(2) This specification is an engineering estimate based on design parameters, and is not tested.

FIGURE 1 — STANDARD TEST CIRCUIT



*A 1.0 μF tantalum or 10 μF electrolytic capacitor may be necessary to compensate for lead inductance when measuring Hysteresis Voltage. When this capacitor is used, it should be placed as close as possible to the device package.

TYPICAL CHARACTERISTICS

FIGURE 2 — DRIVE CURRENT versus SENSE VOLTAGE

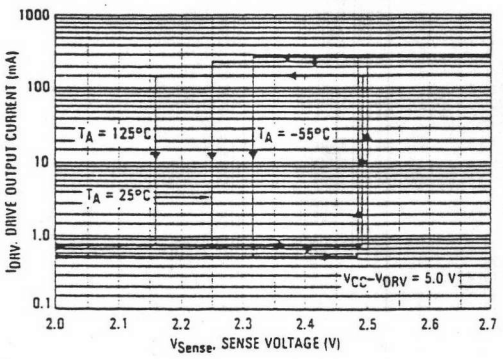


FIGURE 3 — SENSE TRIP VOLTAGE versus TEMPERATURE

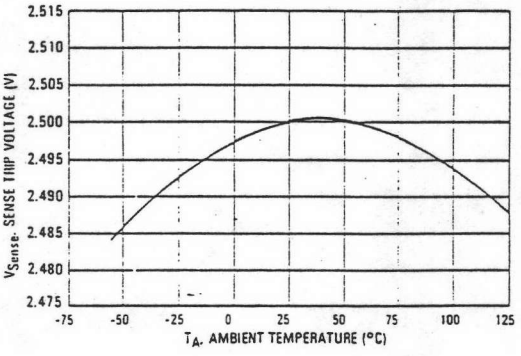


FIGURE 4 — OFF STATE DRIVE CURRENT versus SUPPLY VOLTAGE

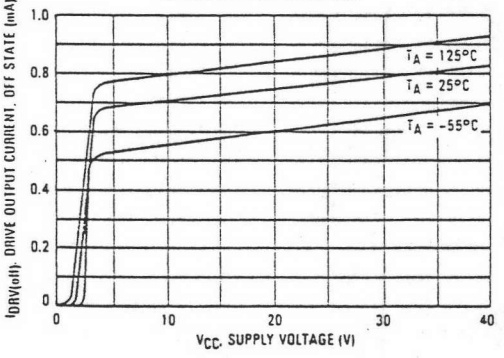


FIGURE 5 — INPUT BIAS CURRENT versus SENSE VOLTAGE

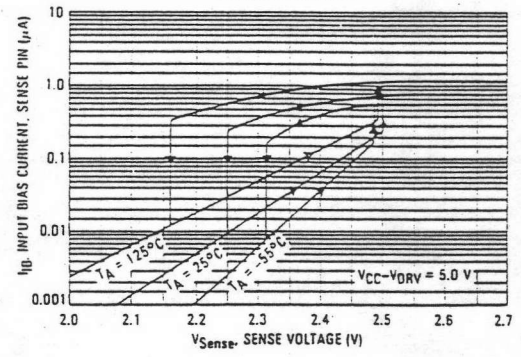


FIGURE 6 — DELAY CAPACITANCE versus DELAY TIME

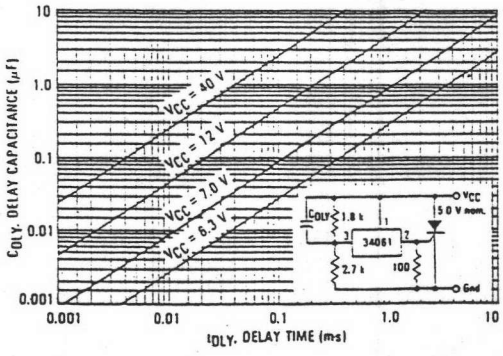
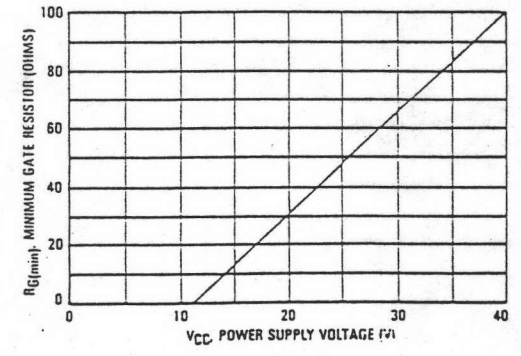
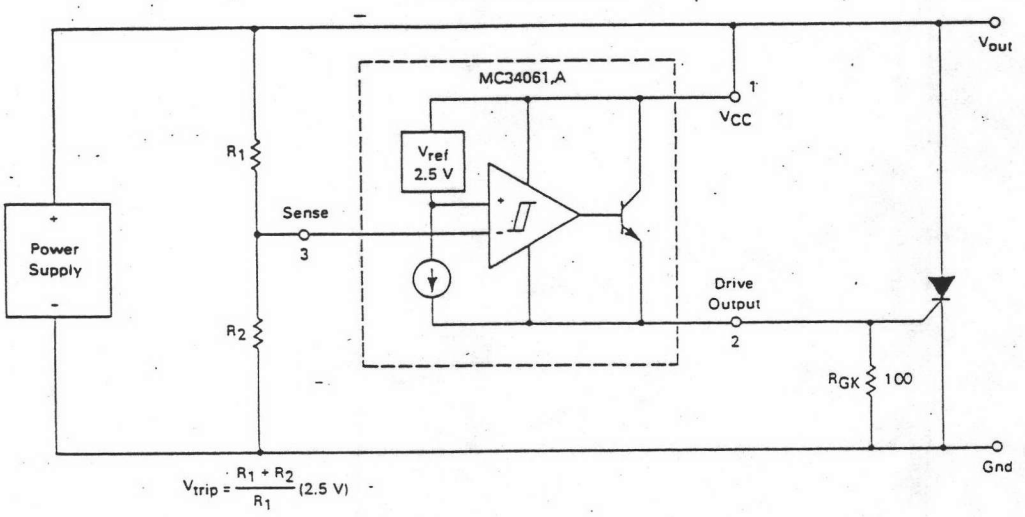


FIGURE 7 — MINIMUM R_G versus SUPPLY VOLTAGE



APPLICATIONS INFORMATION

FIGURE 8 — BLOCK DIAGRAM AND TYPICAL APPLICATION



BASIC CIRCUIT CONFIGURATION

The MC34061,A consists of a 2.5 V shunt reference, a comparator with 250 mV hysteresis and a power output transistor. In the typical application of Figure 8, the voltage at the inverting input of the comparator is $\frac{V_{CC}\ R_2}{R_1 + R_2}$, while the voltage at the non-inverting input is $V_{CC} - 2.5$ V. Thus, given (R_1, R_2) voltage divider, the comparator's output state is a function of V_{CC}. The following table applies:

V_{CC}	Drive Output
$< \frac{R_1 + R_2}{R_1}$ (2.5 V)	OFF State
$> \frac{R_1 + R_2}{R_1}$ (2.5 V)	ON State

By making the proper choice of R_1 and R_2, a level detector for any voltage within the device's operating voltage range may be realized. A few precautions are necessary, however.

Note that even in the OFF State, a minimum drive output current, equal to the sum of the reference and comparator supply currents, is available. Therefore, a means of shunting this current away from the driven circuit is necessary. In the example of Figure 8, a 100 Ω resistor (R_{GK}) is used, producing a voltage at the Drive Output of approximately 60 mV in the OFF State.

In the ON State the MC34061,A becomes a current source capable of saturating to within 2.0 V of V_{CC}. Therefore, when driving a high impedance load, it may be desirable to clamp the drive output to at least 3.0 V below V_{CC} ($V_{CC} - V_{DRV} \geq 3.0$ V) if it is important that the voltage reference continue to regulate.

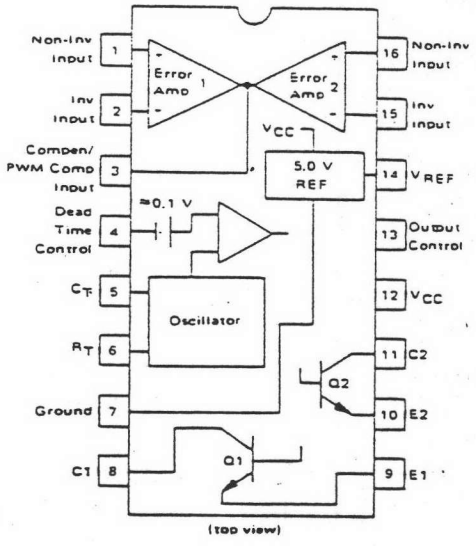
MOTOROLA

TL494

SWITCHMODE PULSE WIDTH MODULATION CONTROL CIRCUITS

The TL494 is a fixed frequency, pulse width modulation control circuit designed primarily for Switchmode power supply control. This device features:

- Complete Pulse Width Modulation Control Circuitry
- On-Chip Oscillator With Master Or Slave Operation
- On-Chip Error Amplifiers
- On-Chip 5 Volt Reference
- Adjustable Dead-Time Control
- Uncommitted Output Transistors Rated to 500 mA Source Or Sink
- Output Control For Push-Pull Or Single-Ended Operation
- Undervoltage Lockout

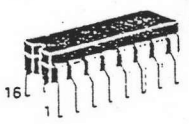


(top view)

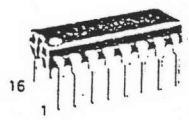
The TL494C is specified over the commercial operating range of 0°C to 70°C. The TL494I is specified over the industrial range of −25°C to 85°C. The TL494M is specified over the full military range of −55°C to 125°C.

SWITCHMODE
PULSE WIDTH MODULATION
CONTROL CIRCUITS

SILICON MONOLITHIC
INTEGRATED CIRCUITS



J SUFFIX
CERAMIC PACKAGE
CASE 620-10



N SUFFIX
PLASTIC PACKAGE
CASE 648-06

ORDERING INFORMATION

Device	Temperature Range	Package
TL494CN	0° to +70°C	Plastic DIP
TL494CJ	0° to +70°C	Ceramic DIP
TL494IN	−25° to +85°C	Plastic DIP
TL494IJ	−25° to +85°C	Ceramic DIP
TL494MJ	−55° to +125°C	Ceramic DIP

FIGURE 1 — BLOCK DIAGRAM

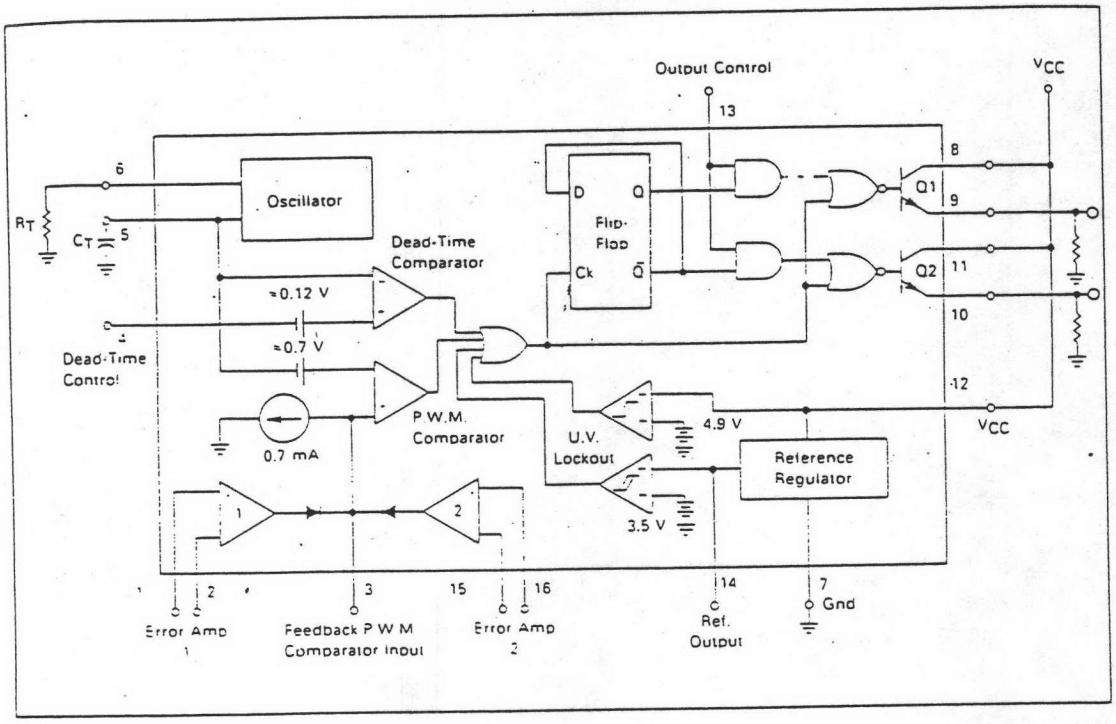
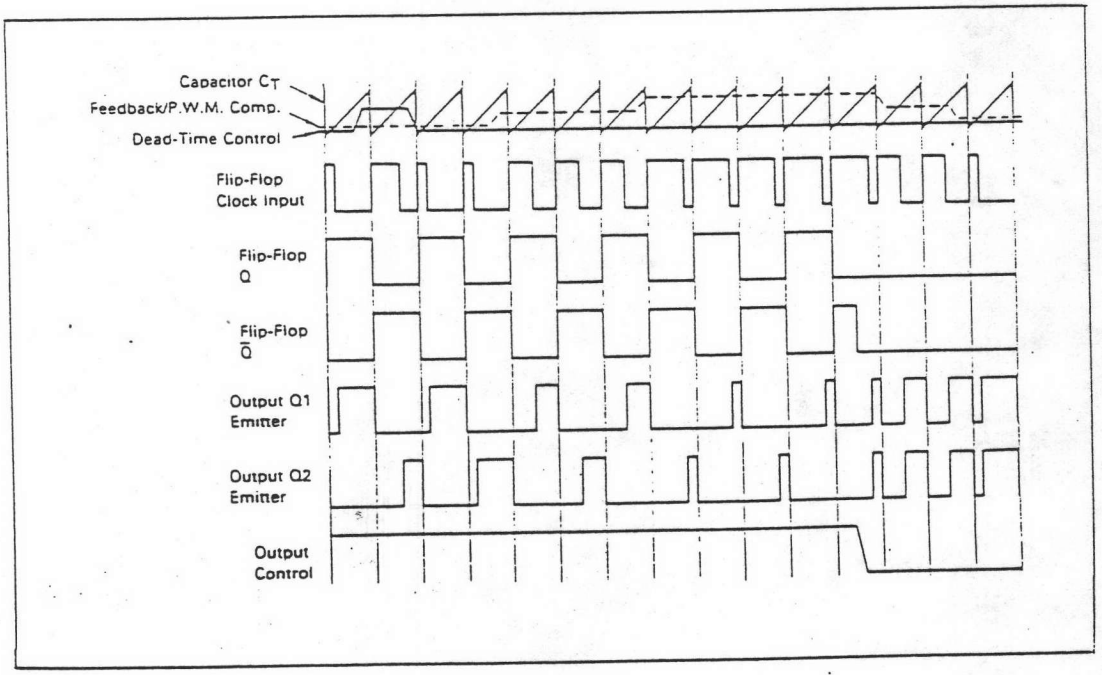


FIGURE 2 — TIMING DIAGRAM



TL494

Description

The TL494 is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal-linear sawtooth oscillator is frequency-programmable by two external components, R_T and C_T. The approximate oscillator frequency is determined by:

$$f_{osc} \approx \frac{1.1}{R_T \bullet C_T}$$

For more information refer to Figure 4.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The NOR gates, which drive output transistors Q1 and Q2, are enabled only when the flip-flop clock-input line is in its low state. This happens only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control-signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the timing diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the dead-time control, the error amplifier inputs, or the feedback input. The dead-time control comparator has an effective 120 mV input offset which limits the minimum output dead time to approximately the first 4% of the sawtooth-cycle time. This would result in a maximum duty cycle on a given output of 96% with the output control grounded, and 48% with it connected to the reference line. Additional dead time may be imposed on the output by setting the dead time-control input to a fixed voltage, ranging between 0 to 3.3 V.

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on-time, established by the dead time control input, down to zero, as the voltage at the feedback pin varies from 0.5 to 3.5 V. Both error amplifiers have a common-mode input range from −0.3 V to (V_{CC} − 2 V), and may be used to sense power-supply output voltage and current. The error-amplifier outputs are active high and are ORed together at the non-inverting input of the pulse-width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

When capacitor C_T is discharged, a positive pulse is generated on the output of the dead-time comparator, which clocks the pulse-steering flip-flop and inhibits the output transistors, Q1 and Q2. With the output-control connected to the reference line, the pulse-steering flip-flop directs the modulated pulses to each of the two output transistors alternately for push-pull operation. The output frequency is equal to half that of the oscillator. Output drive can also be taken from Q1 or Q2, when single-ended operation with a maximum on-time of less than 50% is required. This is desirable when the output transformer has a ringback winding with a catch diode used for snubbing. When higher output-drive currents are required for single-ended operation, Q1 and Q2 may be connected in parallel, and the output-mode pin must be tied to ground to disable the flip-flop. The output frequency will now be equal to that of the oscillator.

The TL494 has an internal 5 V reference capable of sourcing up to 10 mA of load current for external bias circuits. The reference has an internal accuracy of ±1.5% with a typical thermal drift of less than 50 mV over an operating temperature range of 0 to 70°C.

FIGURE 3 — FUNCTIONAL TABLE

Input Output Control	Output Function	$\frac{f_{out}}{f_{osc}}$ =
Grounded	Single-ended P.W.M. at Q1 and Q2	1
At V_{ref}	Push-pull operation	0.5

TL494

MAXIMUM RATINGS (Full operating ambient temperature range applies unless otherwise noted)

Rating	Symbol	TL494C	TL494I	TL494M	Unit
Power Supply Voltage	V_{CC}	42	42	42	V
Collector Output Voltage	V_{C1}, V_{C2}	42	42	42	V
Collector Output Current (each transistor) (1)	I_{C1}, I_{C2}	500	500	500	mA
Amplifier Input Voltage Range	V_{IR}	−0.3 to 42	−0.3 to 42	−0.3 to 42	V
Power Dissipation @ $T_A \leq 45°C$	P_D	1000	1000	1000	mW
Operating Junction Temperature Plastic Package Ceramic Package	T_J	 125 150	 125 150	 — 150	°C °C °C
Operating Ambient Temperature Range	T_A	0 to 70	−25 to 85	−55 to 125	°C
Storage Temperature Range Plastic Package Ceramic Package	T_{stg}	 −55 to 125 −65 to 150	 −55 to 125 −65 to 150	 — −65 to 150	°C

NOTE 1: Maximum thermal limits must be observed.

THERMAL CHARACTERISTICS

Characteristics	Symbol	N Suffix Plastic Package	J Suffix Ceramic Package	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	80	100	°C/W
Derating Ambient Temperature	T_A	45	50	°C

RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	TL494			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_{C1}, V_{C2}	—	30	40	V
Collector Output Current (each transistor)	I_{C1}, I_{C2}	—	—	200	mA
Amplifier Input Voltage	V_{in}	−0.3	—	V_{CC} − 2.0	V
Current Into Feedback Terminal	I_{fb}	—	—	0.3	mA
Reference Output Current	I_{ref}	—	—	10	mA
Timing Resistor	R_T	1.8	30	500	kΩ
Timing Capacitor	C_T	0.0047	0.001	10	μF
Oscillator Frequency	f_{osc}	1.0	40	200	kHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ unless otherwise noted.)
For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	TL494C,I			TL494M			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Voltage (I_O = 1.0 mA)	V_{ref}	4.75	5.0	5.25	4.75	5.0	5.25	V
Line Regulation (V_{CC} = 7.0 V to 40 V)	Reg_{line}	—	2.0	25	—	2.0	25	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	—	3.0	15	—	3.0	15	mV
Short-Circuit Output Current (V_{ref} = 0 V)	I_{SC}	15	35	75	15	35	75	mA

TL494

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ unless otherwise noted.)
For typical values T_A = 25°C, for min max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	TL494C,I			TL494M			Unit
		Min	Typ	Max	Min	Typ	Max	
OUTPUT SECTION								
Collector Off-State Current (V_{CC} = 40 V, V_{CE} = 40 V)	$I_{C(off)}$	—	2.0	100	—	2.0	100	μA
Emitter Off-State Current (V_{CC} = 40 V, V_C = 40 V, V_E = 0 V)	$I_{E(off)}$	—	—	−100	—	—	−150	μA
Collector-Emitter Saturation Voltage (2) Common-Emitter (V_E = 0 V, I_C = 200 mA)	$V_{SAT(C)}$	—	1.1	1.3	—	1.1	1.5	V
Emitter-Follower (V_C = 15 V, I_E = −200 mA)	$V_{SAT(E)}$	—	1.5	2.5	—	1.5	2.5	V
Output Control Pin Current Low State (V_{OC} ≤ 0.4 V)	I_{OCL}	—	10	—	—	10	—	μA
High State (V_{OC} = V_{ref})	I_{OCH}	—	0.2	3.5	—	0.2	3.5	mA
Output Voltage Rise Time Common-Emitter (See Figure 13)	t_r	—	100	200	—	100	200	ns
Emitter-Follower (See Figure 14)		—	100	200	—	100	200	ns
Output Voltage Fall Time Common-Emitter (See Figure 13)	t_f	—	25	100	—	25	100	ns
Emitter-Follower (See Figure 14)		—	40	100	—	40	100	ns

Characteristic	Symbol	TL494			Unit
		Min	Typ	Max	
ERROR AMPLIFIER SECTIONS					
Input Offset Voltage (V_O (Pin 3) = 2.5 V)	V_{IO}	—	2.0	10	mV
Input Offset Current (V_O (Pin 3) = 2.5 V)	I_{IO}	—	5.0	250	nA
Input Bias Current (V_O (Pin 3) = 2.5 V)	I_{IB}	—	−0.1	−1.0	μA
Input Common-Mode Voltage Range (V_{CC} = 40 V, T_A = 25°C)	V_{ICR}	−0.3 to V_{CC} − 2.0	—	—	V
Open-Loop Voltage Gain (ΔV_O = 3.0 V, V_O = 0.5 to 3.5 V, R_L = 2.0 kΩ)	A_{VOL}	70	95	—	dB
Unity-Gain Crossover Frequency (V_O = 0.5 to 3.5 V, R_L = 2.0 kΩ)	f_C	—	350	—	kHz
Phase Margin at Unity-Gain (V_O = 0.5 to 3.5 V, R_L = 2.0 kΩ)	θ_m	—	65	—	deg.
Common-Mode Rejection Ratio (V_{CC} = 40 V)	CMRR	65	90		dB
Power Supply Rejection Ratio (ΔV_{CC} = 33 V, V_O = 2.5 V, R_L = 2.0 kΩ)	PSRR	—	100	—	dB
Output Sink Current (V_O (Pin 3) = 0.7 V)	I_O-	0.3	0.7	—	mA
Output Source Current (V_O (Pin 3) = 3.5 V)	I_O+	−2.0	−4.0	—	mA

NOTE 2: Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperatures as possible.

TL494

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ unless otherwise noted.)
For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies unless otherwise noted.

Characteristic	Symbol	TL494 Min	TL494 Typ	TL494 Max	Unit
PWM COMPARATOR SECTION (Test Circuit Figure 12)					
Input Threshold Voltage (Zero duty cycle)	V_{TH}	—	3.5	4.5	V
Input Sink Current ($V_{(Pin\ 3)}$ = 0.7 V)	I_{I-}	0.3	0.7	—	mA
DEAD-TIME CONTROL SECTION (Test Circuit Figure 12)					
Input Bias Current (Pin 4) ($V_{Pin\ 4}$ = 0 to 5.25 V)	$I_{IB\ (DT)}$	—	−2.0	−10	μA
Maximum Duty Cycle, Each Output, Push-Pull Mode ($V_{Pin\ 4}$ = 0 V, C_T = 0.01 μF, R_T = 12 kΩ) ($V_{Pin\ 4}$ = 0 V, C_T = 0.001 μF, R_T = 30 kΩ)	DC_{max}	 45 —	 48 45	 50 50	%
Input Threshold Voltage (Pin 4) (Zero Duty Cycle) (Maximum Duty Cycle)	V_{TH}	 — 0	 2.8 —	 3.3 —	V
OSCILLATOR SECTION					
Frequency (C_T = 0.001 μF, R_T = 30 kΩ)	f_{osc}	—	40	—	kHz
Standard Deviation of Frequency* (C_T = 0.001 μF, R_T = 30 kΩ)	σf_{osc}	—	3.0	—	%
Frequency Change with Voltage (V_{CC} = 7.0 V to 40 V, T_A = 25°C)	$\Delta f_{osc}\ (\Delta V)$	—	0.1	—	%
Frequency Change with Temperature ($\Delta T_A = T_{low}$ to T_{high}) (C_T = 0.01 μF, R_T = 12 kΩ)	$\Delta f_{osc}\ (\Delta T)$	—	—	12	%
UNDERVOLTAGE LOCKOUT SECTION					
Turn-On Threshold (V_{CC} increasing, I_{ref} = 1.0 mA)	V_{th}	5.5	6.43	7.0	V
TOTAL DEVICE					
Standby Supply Current (Pin 6 at V_{ref}, All Other Inputs and Outputs Open) (V_{CC} = 15 V) (V_{CC} = 40 V)	I_{CC}	 — —	 5.5 7.0	 10 15	mA
Average Supply Current ($V_{(Pin\ 4)}$ = 2.0 V) (See Figure 12) (C_T = 0.01 μF, R_T = 12 kΩ, V_{CC} = 15 V)	—	—	7.0	—	mA

* Standard deviation is a measure of the statistical distribution about the mean as derived from the formula, $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (X_n - \bar{X})^2}{N-1}}$

FIGURE 4 — OSCILLATOR FREQUENCY versus TIMING RESISTANCE

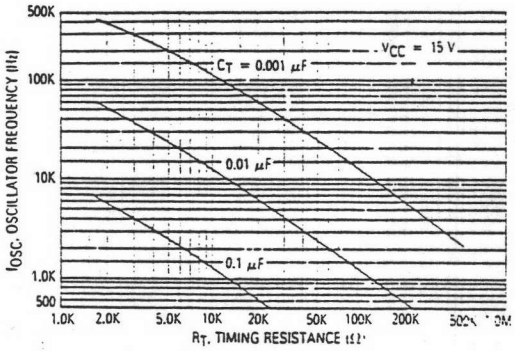


FIGURE 5 — OPEN-LOOP VOLTAGE GAIN AND PHASE versus FREQUENCY

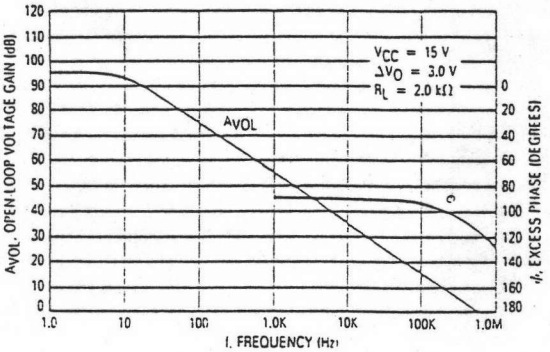


FIGURE 6 — PERCENT DEAD-TIME versus OSCILLATOR FREQUENCY

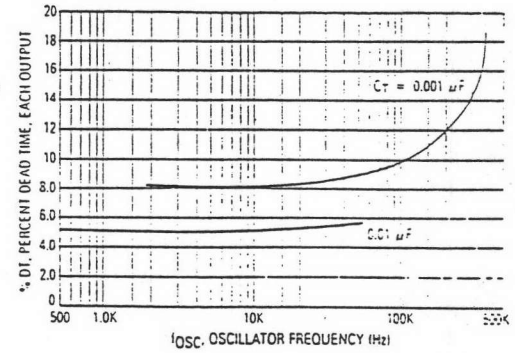


FIGURE 7 — PERCENT DUTY CYCLE versus DEAD-TIME CONTROL VOLTAGE

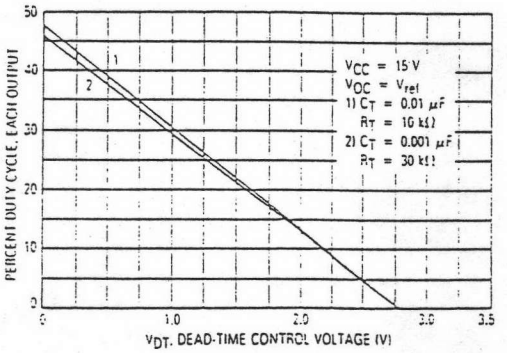


FIGURE 8 — EMITTER FOLLOWER CONFIGURATION OUTPUT SATURATION VOLTAGE versus EMITTER CURRENT

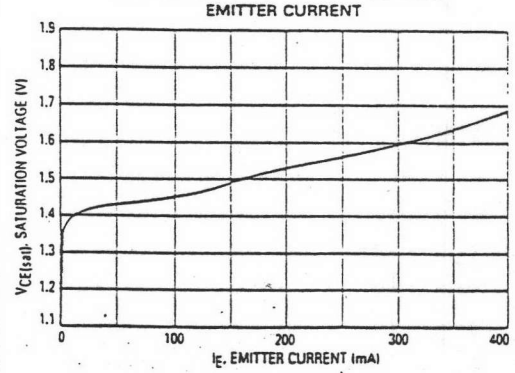


FIGURE 9 — COMMON EMITTER CONFIGURATION OUTPUT SATURATION VOLTAGE versus COLLECTOR CURRENT

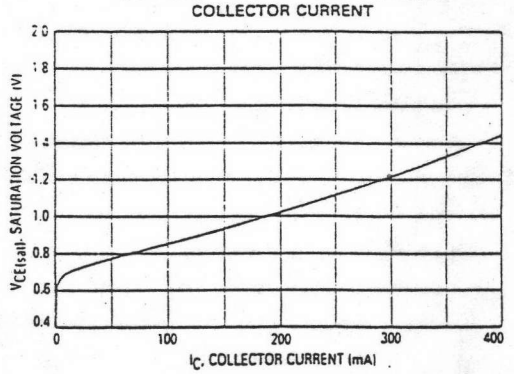


FIGURE 10 — STANDBY SUPPLY CURRENT versus SUPPLY VOLTAGE

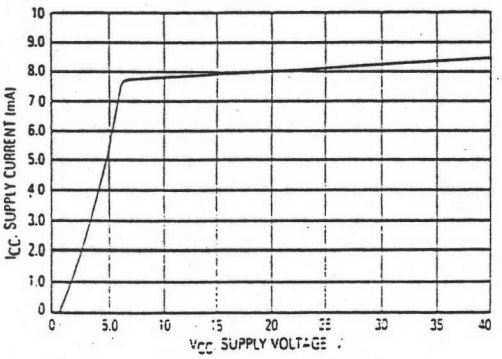


FIGURE 11 — ERROR AMPLIFIER CHARACTERISTICS

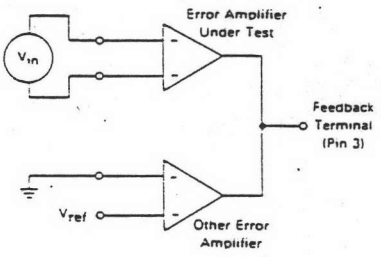


FIGURE 12 — DEAD-TIME AND FEEDBACK CONTROL TEST CIRCUIT

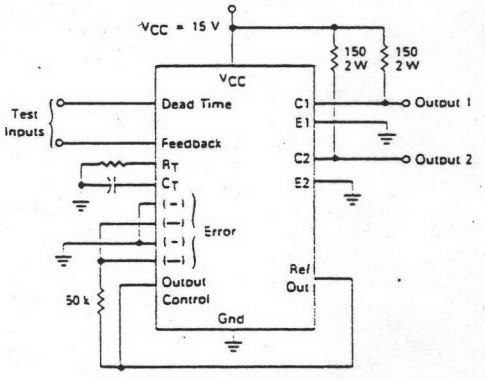


FIGURE 13 — COMMON-EMITTER CONFIGURATION TEST CIRCUIT AND WAVEFORM

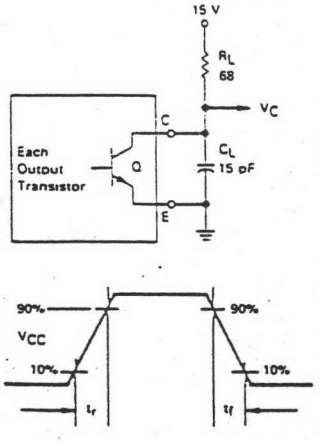


FIGURE 14 — EMITTER-FOLLOWER CONFIGURATION TEST CIRCUIT AND WAVEFORM

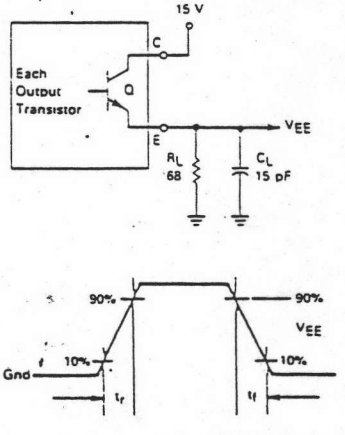
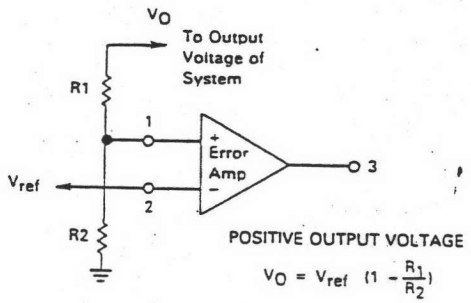


FIGURE 15 — ERROR-AMPLIFIER SENSING TECHNIQUES



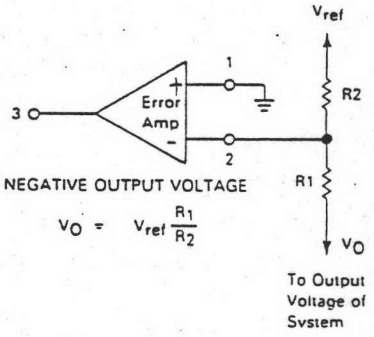


FIGURE 16 — DEAD-TIME CONTROL CIRCUIT

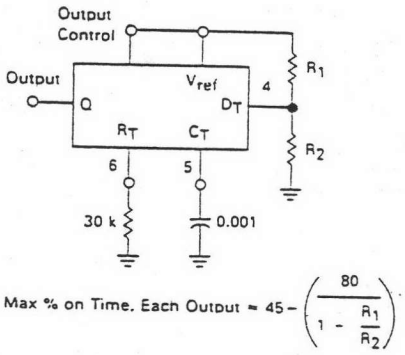


FIGURE 17 — SOFT-START CIRCUIT

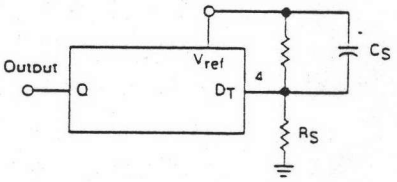
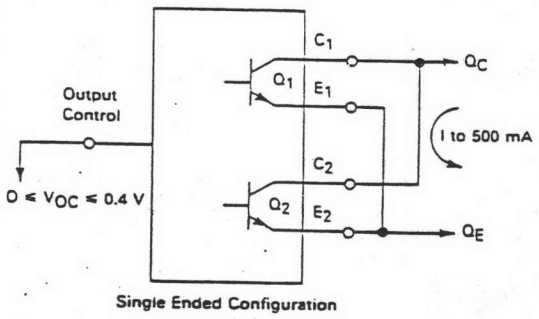
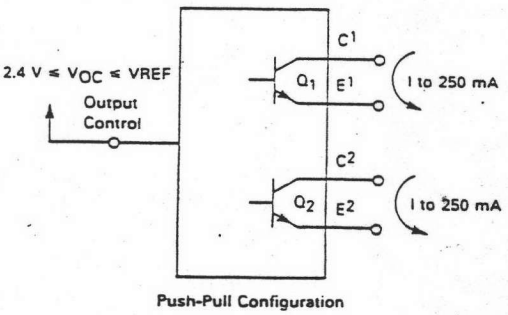


FIGURE 18 — OUTPUT CONNECTIONS FOR SINGLE-ENDED AND PUSH-PULL CONFIGURATIONS





FAST RECOVERY RECTIFIERS

OPERATING AND STORAGE TEMPERATURE –65°C to +175°C

TYPE	Maximum Peak Reverse Voltage	Maximum Average Rectified Current @ Half-Wave Resistive Load 60Hz		Maximum Forward Peak Surge Current @ 8.3ms Superimposed	Maximum Reverse Current @ PRV @ 25°C T_A	Maximum Forward Voltage @ 25°C T_A		Maximum Reverse Recovery Time
	PRV	Io @ T_A		I_{FM} (Surge)	I_R	I_{FM}	V_{FM}	Trr
	V_{PK}	A_{AV}	°C	A_{PK}	µAdc	A_{PK}	V_{PK}	nS

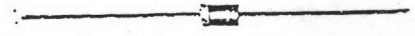
.0 AMPERES FAST RECOVERY/GD 6

GD601F	50	6.0	55	300	10	6.0	1.3	150
GD602F	100	6.0	55	300	10	6.0	1.3	150
GD603F	200	6.0	55	300	10	6.0	1.3	150
GD604F	400	6.0	55	300	10	6.0	1.3	150
GD605F	600	6.0	55	300	10	6.0	1.3	250
GD606F	800	6.0	55	300	10	6.0	1.3	500
GD607F	1000	6.0	55	300	10	6.0	1.3	500

HIGH VOLTAGE RECTIFIERS

OPERATING AND STORAGE TEMPERATURE –55°C to +175°C

TYPE	Maximum Peak Reverse Voltage	Maximum Average Rectified Current @ Half-Wave Resistive Load 60Hz		Maximum Forward Peak Surge Current @ 8.3ms Superimposed	Maximum Reverse Current @ PRV @ 25°C T_A	Maximum Forward Voltage @ 25°C T_A		Maximum Reverse Recovery Time
	PRV	Io @ T_A		I_{FM} (Surge)	I_R	I_{FM}	V_{FM}	Trr
	V_{PK}	mA	°C	A_{PK}	µAdc	A_{PK}	V_{PK}	nS



IGH VOLTAGE/DO-41/DO-15

GD1200	1200	500	50	30	5.0	0.5	2.0	–
GD1500	1500	500	50	30	5.0	0.5	2.0	–
GD1800	1800	500	50	30	5.0	0.5	2.0	–
GD2000	2000	500	50	30	5.0	0.5	3.0	–
GD2500	2500	200	50	30	5.0	0.2	3.0	–
GD3000	3000	200	50	30	5.0	0.2	3.0	–
GD5000	5000	200	50	30	5.0	0.2		–

IGH VOLTAGE FAST RECOVERY/DO-41/DO-15

GD1200F	1200	500	50	30	5.0	0.5	2.0	500
GD1500F	1500	500	50	30	5.0	0.5	2.0	500
GD1800F	1800	500	50	30	5.0	0.5	2.0	500
GD2000F	2000	500	50	30	5.0	0.5	2.0	500
GD2500F	2500	200	50	30	5.0	0.2	3.0	500
GD3000F	3000	200	50	30	5.0	0.2	3.0	500
GD5000F	5000	200	50	30	5.0	0.2	3.0	500

MOTOROLA

MTM8N18, MTM8N20
MTP8N18, MTP8N20

Designer's Data Sheet

8.0 AMPERE

N-CHANNEL TMOS POWER FET

$r_{DS(on)}$ = 0.4 OHM

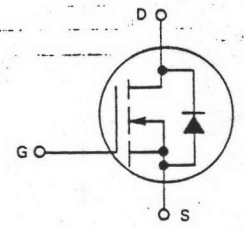
180 and 200 VOLTS

N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

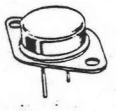
These TMOS Power FETs are designed for high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

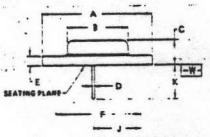
- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, SOA and $V_{GS(th)}$ Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™

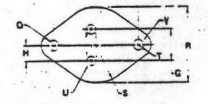


MTM8N18
MTM8N20





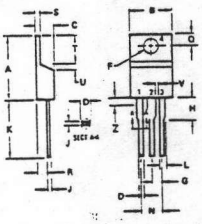
STYLE 3:
PIN 1. GATE
2. SOURCE
CASE DRAIN



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	8.35	7.62	0.250	0.300
D	0.97	1.09	0.038	0.043
E	1.40	1.78	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.81	4.19	0.150	0.165
R	–	26.67	–	1.050
U	2.54	3.05	0.100	0.120
V	3.81	4.19	0.150	0.165

CASE 1-04
TO-204AA
(TO-3 TYPE)

MTP8N18
MTP8N20



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	15.11	15.75	0.595	0.620
B	9.65	10.29	0.380	0.405
C	4.06	4.82	0.160	0.190
D	0.64	0.89	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.41	2.67	0.095	0.105
H	2.79	3.30	0.110	0.130
J	0.36	0.56	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.14	1.39	0.045	0.054
R	4.83	5.33	0.190	0.210
S	2.54	3.04	0.100	0.120
A	2.04	2.79	0.080	0.110
F	1.14	1.39	0.045	0.054
T	5.97	6.48	0.235	0.255
U	0.76	1.27	0.030	0.050
V	1.14		0.045	
X	–	2.65	–	0.095

CASE 221A-02
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	MTM8N18 MTP8N18	MTM8N20 MTP8N20	Unit
Drain-Source Voltage	V_{DSS}	180	200	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	180	200	Vdc
Gate-Source Voltage	V_{GS}	±20		Vdc
Drain Current Continuous Pulsed	 I_D I_{DM}	 8.0 25		Adc
Gate Current — Pulsed	I_{GM}	1.5		Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6		Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150		°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case	$R_{\theta JC}$	1.67	°C/W
Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 5.0 mA)	MTM8N18/MTP8N18 MTMN818/MTP8N20	$V_{(BR)DSS}$	 180 200	 — —	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 0.85 BV_{DSS}, V_{GS} = 0) T_J = 100°C		I_{DSS}	 — —	 0.25 2.5	mAdc
Gate-Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	500	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (I_D = 1.0 mA, V_{DS} = V_{GS})	T_J = 100°C	$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 4.0 Adc) (I_D = 8.0 Adc) (I_D = 4.0 Adc, T_J = 100°C)		$V_{DS(on)}$	 — — —	 1.6 4.0 3.2	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 4.0 Adc)		$r_{DS(on)}$	—	0.4	Ohms
Forward Transconductance (V_{DS} = 15 V, I_D = 4.0 A)		g_{fs}	3.0	—	mhos
SAFE OPERATING AREAS					
Forward Biased Safe Operating Area		FBSOA	See Figure 12		
Switching Safe Operating Area		SSOA	See Figure 13		
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	1000	pF
Output Capacitance		C_{oss}	—	300	pF
Reverse Transfer Capacitance		C_{rss}	—	80	pF
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DS} = 25 V, I_D = 4.0 A, R_{gen} = 50 ohms)	$t_{d(on)}$	—	40	ns
Rise Time		t_r	—	150	ns
Turn-Off Delay Time		$t_{d(off)}$	—	100	ns
Fall Time		t_f	—	100	ns

SOURCE DRAIN DIODE CHARACTERISTICS*

Characteristic		Symbol	Typ	Unit
Forward On-Voltage	I_S = 8.0 A V_{GS} = 0	V_{SD}	2.0	Vdc
Forward Turn-On Time		t_{on}	250	ns
Reverse Recovery Time		t_{rr}	325	ns

*Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2%.

RESISTIVE SWITCHING

FIGURE 1 — SWITCHING TEST CIRCUIT

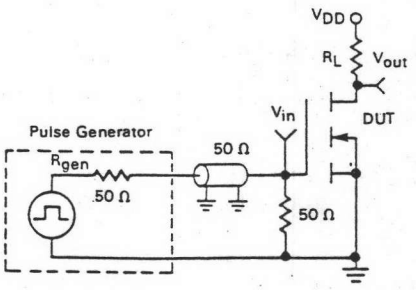
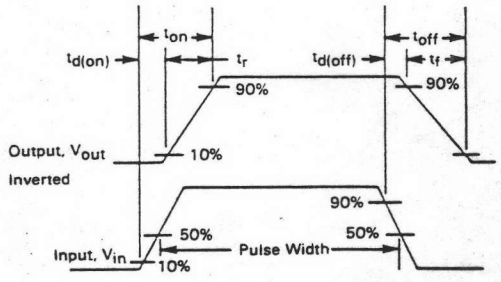


FIGURE 2 — SWITCHING WAVEFORMS



TYPICAL CHARACTERISTICS

FIGURE 3 — OUTPUT CHARACTERISTICS

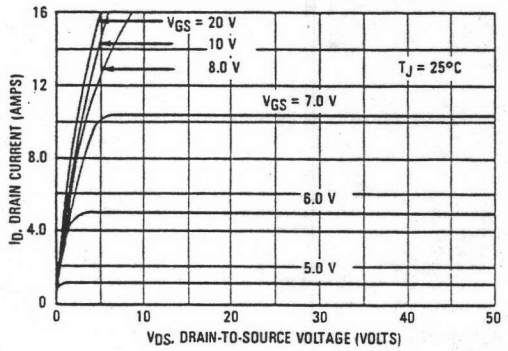


FIGURE 4 — ON-REGION CHARACTERISTICS

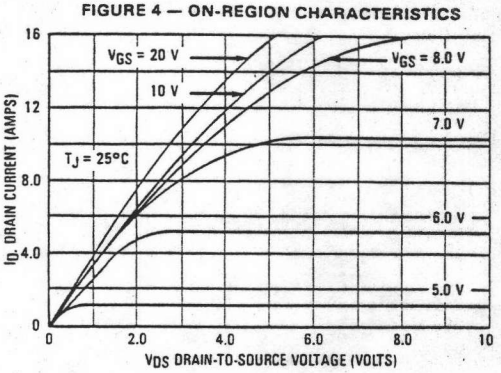


FIGURE 5 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

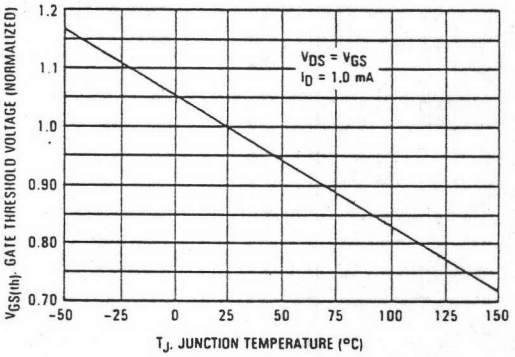


FIGURE 6 — TRANSFER CHARACTERISTICS

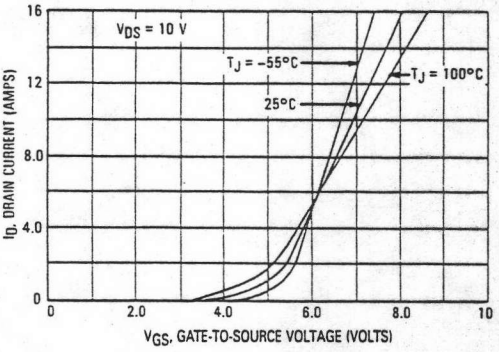


FIGURE 7 — ON-RESISTANCE versus DRAIN CURRENT

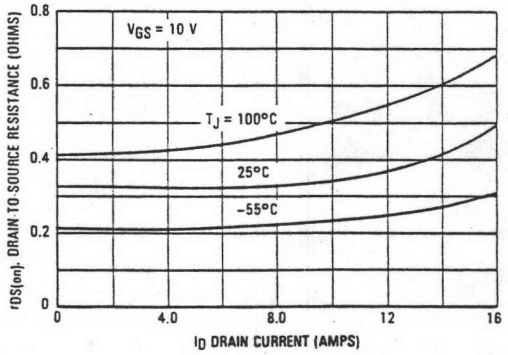
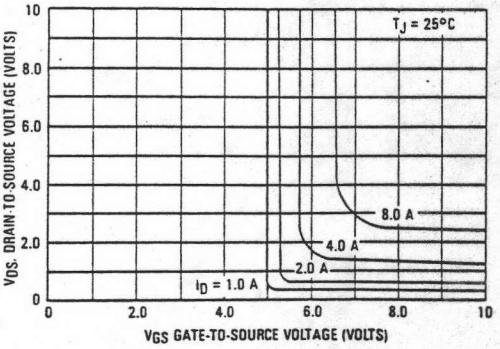
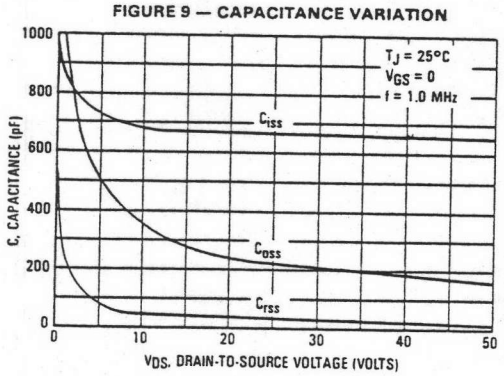


FIGURE 8 — ON-VOLTAGE VARIATION



TYPICAL CHARACTERISTICS

FIGURE 9 — CAPACITANCE VARIATION



THERMAL RESPONSE

FIGURE 10 — MTM8N18/MTM8N20

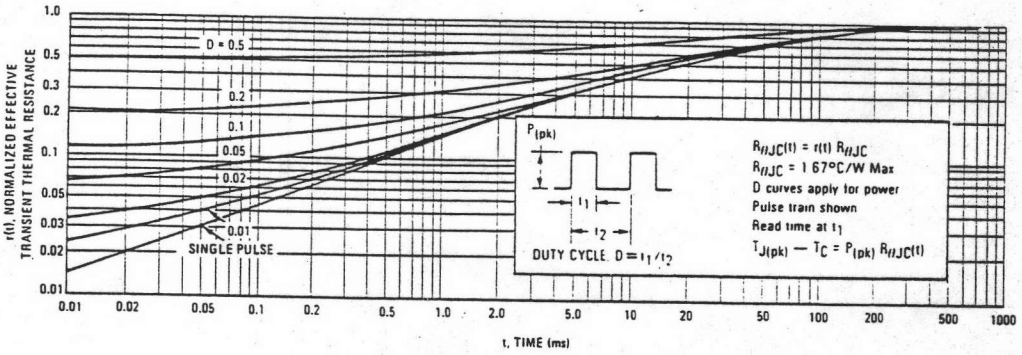
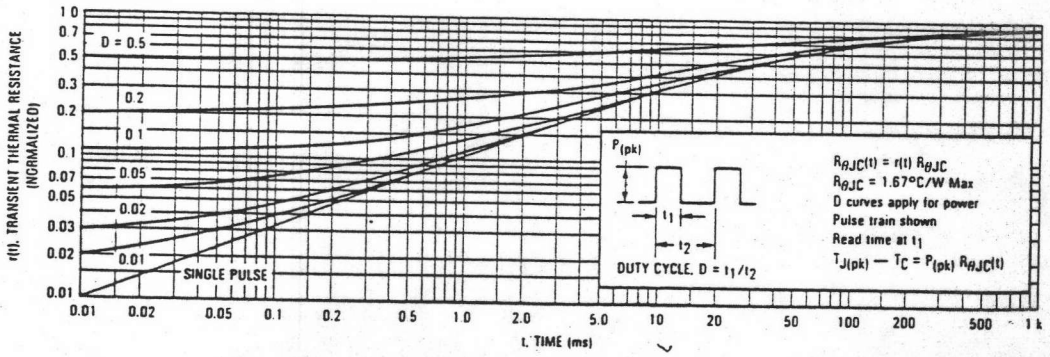


FIGURE 11 — MTP8N18/MTP8N20



SAFE OPERATING AREA INFORMATION

FIGURE 12 — MAXIMUM FORWARD BIASED SAFE OPERATING AREA

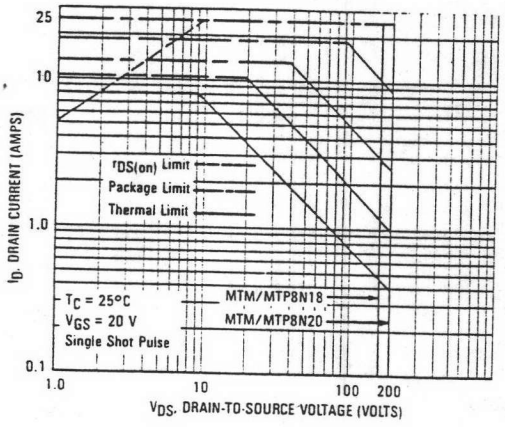
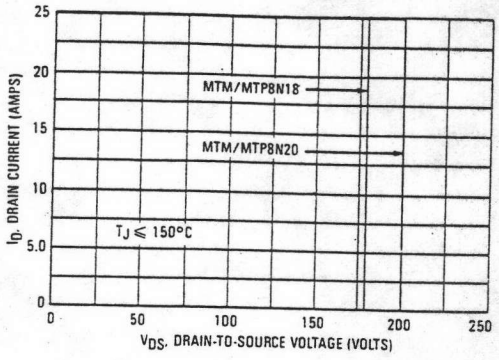


FIGURE 13 — MAXIMUM SWITCHING SAFE OPERATING AREA



FORWARD BIASED SAFE OPERATING AREA

The dc data of Figure 12 is based on a case temperature (T_C) of 25°C and a maximum junction temperature (T_{Jmax}) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current (I_{DM}) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at T_C = 25°C from Figure 12.
$T_{J(max)}$ = rated maximum junction temperature.
T_C = device case temperature.
P_D = rated power dissipation at T_C = 25°C.
$R_{\theta JC}$ = rated steady state thermal resistance.
$r(t)$ = normalized thermal response from Figures 10 or 11.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 13 is the boundary that the load line may traverse without incurring damage to the MOSFET. The Fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 13 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

TMOS POWER FET CONSIDERATIONS

Switching Speed — The switching speeds of these devices are dependent on the driving impedance. Extremely fast switching speeds can be attained by driving the gate from a voltage source.

Transfer Characteristics — The transfer characteristics are linear at drain currents of 2.0 A. (See Figure 6.) Linear amplifiers with high frequency response can be designed using this product.

Gate Voltage Rating — Never exceed the gate voltage rating of ±20 V. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gate of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate to source. The addition of an internal zener diode may result in detrimental effects on the reliability of a power MOSFET. If gate protection is required, an external zener diode is recommended.

Handling and Packaging — MOS ICs are susceptible to damage from electrostatic charge. Experience has shown that these devices are more rugged than MOS ICs. This is primarily due to the comparatively larger capacitances associated with power devices, however, reasonable precautions in handling and packaging MOS devices should be observed.

ภาคผนวก ค

รายการอุปกรณ์

ไอซี

U_1	LM7812
U_2	LM7012
U_3	MC14001
U_{4-5}	MC34061
U_{6-7}	LM741
U_8	TL494
U_{9-10}	CA3140
U_{11}	MC14027

ทรานซิสเตอร์

Q_{7-8}	2N4400
Q_9 , Q_{13-14}	MTP8N20
Q_{10-12}	2N440
SCR_1 , SCR_2	MCR 106 - 6

ตัวความต้านทาน 1/4 W 5% (แบบคาร์บอนฟิล์ม เฉพาะ 1 % แบบเมทัลฟิล์ม)

R_{11} , R_{43} ,	100K		
R_{14} , R_{16} , R_{27} , R_{49} , R_{52} , R_{56}	1K		
R_{22} , R_{23}	180	1%	1/4W
R_{24} , R_{25}	620	1%	1/2W
R_{28} , R_{29} , R_{45}	100		
R_{30} , R_{37}	4.7K		
R_{31-33}	3.3M		
R_{34}	6.9K		
R_{35} , R_{39} , R_{53} , R_{58}	VR10K		
R_{36}	8K		
R_{38}	50K		
R_{40} , R_{41}	3.3K		
R_{47}	2.2K		
R_{54}	2.4K		
R_{55}	330		
R_{59}	680K		

R_{60-63}		100M
R_{63}		VR 1M

ตัวเก็บประจุ

C_{1}	10,000 uF 50V	แบบอิเล็กโตรไลติก
C_{2-4}	4,700 uF 35V	แบบอิเล็กโตรไลติก
C_{6}	1 uF 35V	แบบอิเล็กโตรไลติก
C_{7}	100 uF 35V	แบบอิเล็กโตรไลติก
C_{9-10}	0.1 uF 100V	แบบไมลา
C_{11-12}	0.01 uF 100V	แบบไมลา
C_{13-14}	1 uF 3KV	แบบเซรามิก
C_{15-16}	0.1 uF 1.5KV	แบบโพลีสไตรีน
C_{17}	0.01 uF 3KV	แบบเซรามิก
C_{18}	470 pF 100V	แบบเซรามิก
C_{19}	0.01 uF 100V	แบบไมลา
C_{20}	0.1 uF 100V	แบบไมลา
C_{21}	0.022 uF 100V	แบบไมลา
C_{22-23}	0.1 uF 100V	แบบไมลา
C_{24}	0.005 uF 50V	แบบเซรามิค
C_{25}	100 uF 50V	แบบอิเล็กโตรไลติก
C_{26}	0.1 uF 50V	แบบไมลา
C_{27}	0.01 uF 50V	แบบเซรามิค
C_{28-29}	0.05 uF 50V	แบบเซรามิค

ไดโอด

D_{1-4}	IN4002
D_{5-8}	IN5402
D_{8-10} , D_{15-16} , D_{21}	IN4148
D_{11}	ซีเนอร์ 5.1V
D_{13-14}	ซีเนอร์ 7.5V
D_{17-18}	ซีเนอร์ 75V
D_{19-20}	D5000

ประวัติผู้เขียน

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