บรรณานุกรม

ภาษาไทย

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I^{2}C Bus Specification

Contents - The I^2C-bus Specification

Full details of Philips' I^2C-bus compatible ICs is given in Data Handbook IC12, ordering code 9398 153 10011

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C system provided the system conforms to the I^2C specification defined by Philips.

1.0 Introduction

For 8-bit applications, such as those requiring single-chip microcomputers, certain design criteria can be established:

- A complete system usually consists of at least one microcomputer and other peripheral devices such as memories and I/O expanders.
- The cost of connecting the various devices within the system must be kept to a minimum.
- Such a system usually performs a control function and doesn't require high-speed data transfer.
- Overall efficiency depends on the devices chosen and the interconnecting bus structure.

To produce a system to satisfy these criteria, a serial bus structure is needed. Although serial buses don't have the throughput capability of parallel buses, they do require less wiring and fewer connecting pins. However, a bus is not merely an interconnecting wire, it embodies all the formats and procedures for communication within the system.

ICs communicating with each other on a serial bus must have some form of protocol which avoids all possibilities of confusion, data loss and blockage of information. Fast ICs must be able to communicate with slow ICs. The system must not be dependent on the ICs connected to it, otherwise modifications or improvements would be impossible. A procedure has also to be devised to decide which IC will be in control of the bus and when. And if different ICs with different clock speeds are connected to the bus - the bus clock source must be defined.

All these criteria are involved in the specification of the I^{2}C-bus.

2.0 The I^{2}C-bus concept

The I^{2}C-bus supports ICs manufactured with any process (NMOS, CMOS, I^{2}L). Two wires, serial data (SDA) and serial clock (SCL) carry information between the ICs connected to the bus. Each IC is recognised by a unique address - whether it's a microcomputer, LCD driver, memory or keyboard interface - and can operate as either a transmitter or receiver, depending on the function of the ICs we're considering. Obviously an LCD driver is only a receiver, while a memory can both receive and transmit data. In addition to transmitters and receivers, ICs can also be considered as masters or slaves when performing data transfers (see Table 1). A master is the IC which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any IC addressed is considered a slave.

The I^{2}C-bus is a multi-master bus. This means that more than one IC capable of controlling the bus can be connected to it. As masters are usually microcomputers, let's consider the case of a data transfer between two microcomputers connected to the I^{2}C-bus (Fig.1). This highlights the master-slave and receiver-transmitter relationships to be found on the I^{2}C-bus. It should be noted that these relationships are not permanent, but only depend on the direction of data transfer at that time. The transfer of data would proceed as follows:

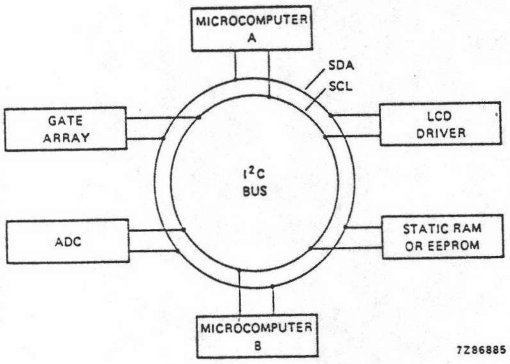

Fig.1 Typical I^{2}C-bus configuration

1) Suppose microcomputer A wants to send information to microcomputer B:
- microcomputer A (master), addresses microcomputer B (slave)
- microcomputer A (master transmitter), sends data to microcomputer B (slave receiver)
- microcomputer A terminates the transfer.

2) If microcomputer A wants to receive information from microcomputer B:
- microcomputer A (master) addresses microcomputer B (slave)
- microcomputer A (master receiver) receives data from microcomputer B (slave transmitter)
- microcomputer A terminates the transfer.

Even in this case, the master (microcomputer A) generates the timing and terminates the transfer.

The possibility of connecting more than one microcomputer to the I^{2}C-bus means that more than one master could try to initiate a data transfer at the same time. To avoid the chaos that might ensue from such an event - an arbitration procedure has been developed. This procedure relies on the wired-AND connection of all I^{2}C interfaces to the I^{2}C-bus.

If two or more masters try to put information onto the bus, the first to produce a 'one' when the other produces a 'zero' will lose the arbitration. The clock signals during arbitration are a synchronised combination of the clocks generated by the masters using the wired-AND connection to the SCL line (for more detailed information concerning arbitration see section 6.0).

Generation of clock signals on the I^{2}C-bus is always the responsibility of master ICs; each master generates its own clock signals when transferring data on the bus. Bus clock signals from a master can only be altered when they are stretched by a slow-slave IC holding-down the clock line, or by another master when arbitration takes place.

Table 1 Definition of I^{2}C-bus terminology

Transmitter:	the IC which sends data to the bus
Receiver:	the IC which receives data from the bus
Master:	the IC which initiates a transfer, generates clock signals and terminates a transfer
Slave:	the IC addressed by a master
Multi-master:	more than one master can attempt to control the bus at the same time without corrupting the message
Arbitration:	procedure to ensure that if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
Synchronization:	procedure to synchronize the clock signals of two or more ICs

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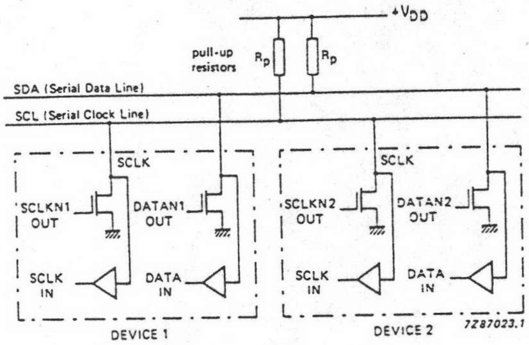


Fig.2 Connection of I^2C interfaces to the I^2C-bus

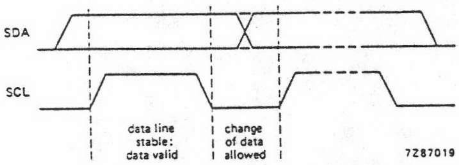


Fig.3 Bit transfer on the I^2C-bus

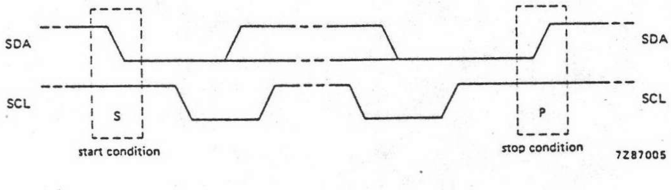


Fig.4 START and STOP conditions

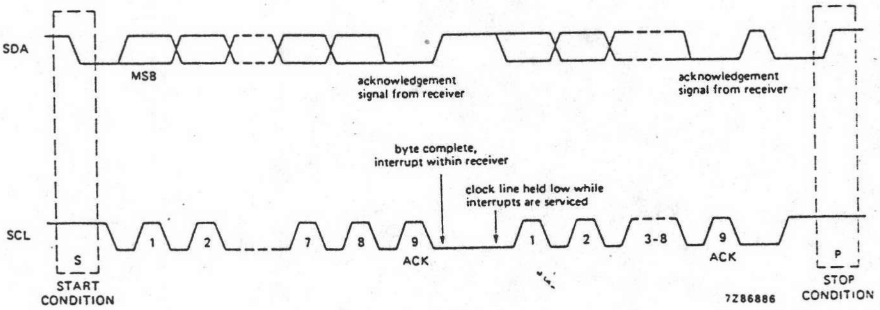

SDA
MSB
acknowledgement signal from receiver
acknowledgement signal from receiver
byte complete, interrupt within receiver
clock line held low while interrupts are serviced
SCL
S
1
2
7
8
9
ACK
1
2
3-8
9
ACK
P
START CONDITION
7Z86886
STOP CONDITION

Fig.5 Data transfer on the I^2C-bus

3.0 General characteristics

Both SDA and SCL are bidirectional lines, connected to a positive supply voltage via a pull-up resistor (see Fig.2). When the bus is free, both lines are HIGH. The output stages of I^2C interfaces connected to the bus must have an open-drain or open-collector to perform the wired-AND function. Data on the I^2C-bus can be transferred at a rate up to 100 kbit/s. The number of interfaces connected to the bus is solely dependent on the limiting bus capacitance of 400 pF.

4.0 Bit transfer

Due to the variety of different technology ICs (CMOS, NMOS, I^2L) which can be connected to the I^2C-bus, the levels of the logical '0' (LOW) and '1' (HIGH) are not fixed and depend on the associated level of V_{DD} (see section 9.0 for Electrical specifications). One clock pulse is generated for each data bit transferred.

4.1 Data validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Fig.3).

4.2 START and STOP conditions

Within the procedure of the I^2C-bus, unique situations arise which are defined as START and STOP conditions (see Fig.4).

A HIGH to LOW transition of the SDA line while SCL is HIGH is one such unique case. This situation indicates a START condition.

A LOW to HIGH transition of the SDA line while SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition. This bus free situation will be described in detail later (in section 10.0).

Detection of START and STOP conditions by ICs connected to the bus is easy if they incorporate the necessary interfacing hardware. However, microcomputers with no such interface have to sample the SDA line at least twice per clock period to sense the transition.

5.0 Transferring data

5.1 Byte format

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first (Fig.5). If a receiver can't receive another complete byte of data until it has performed some other function, for example, servicing an internal interrupt, it can hold the clock line SCL LOW to force the transmitter into a wait state. Data transfer then continues when the receiver is ready for another byte of data and releases clock line SCL.

In some cases, it's permissible to use a different format from the I^2C-bus format (for CBUS compatible ICs for example). A message which starts with such an address can be terminated by generation of a STOP condition, even during the transmission of a byte. In this case, no acknowledge is generated (see section 8.4).

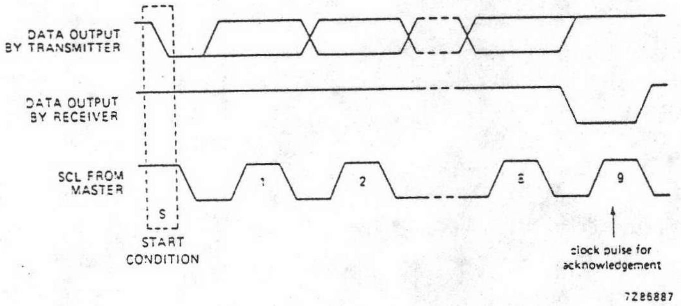


Fig.6 Acknowledge on the I^{2}C-bus

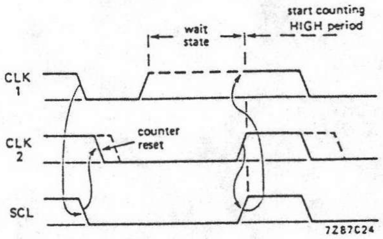


Fig.7 Clock synchronization during the arbitration procedure

5.2 Acknowledge

Data transfer with acknowledge is obligatory. The acknowledge-related clock pulse is generated by the master. The transmittier releases the SDA line (HIGH) during the acknowledge clock pulse.

The receiver has to pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the high period of this clock pulse (Fig.6). Of course, set-up and hold times must also be taken into account and these will be described in section 10.0.

Usually, a receiver which has been addressed is obliged to generate an acknowledge after each byte has been received (except when the message starts with an RC-5 or CBUS address - see section 8.1.3).

When a slave receiver doesn't acknowledge on the slave address (for example, it's unable to receive because it's performing some real-time function), the data line has to be left HIGH by the slave. The master can then generate a STOP condition to abort the transfer.

If a slave receiver acknowledges the slave address but, some time later in the transfer cannot receive any more data bytes, the master must again abort the transfer. This is indicated by the salve not generating the acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates the STOP condition.

If a master receiver is involved in a transfer, it must signal the end of data to the slave transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave transmitter must release the data line to allow the master to generate the STOP condition.

6.0 Arbitration and clock generation

6.1 Synchronization

All masters generate their own clock on the SCL line to transfer messages on the I^2C-bus. Data is only valid during the clock HIGH period. A defined clock is therefore needed for the bit-by-bit arbitration procedure to take place.

Clock synchronization is performed using the wired-AND connection of I^2C interfaces to the SCL line. This means that a HIGH to LOW transition on the SCL line will cause the ICs concerned to start counting off their LOW period and, once an IC clock has gone LOW, it will hold the SCL line in that state until the clock HIGH state is reached (Fig.7). However, the LOW to HIGH transition of this clock may not change the state of the SCL line if another clock is still within its LOW period. The SCL line will therefore be held LOW by the IC with the longest LOW period. ICs with shorter LOW periods enter a HIGH wait-state during this time.

When all ICs concerned have counted off their LOW period, the clock line will be released and go HIGH. There will then be no difference between the IC clocks and the state of the SCL line and all the ICs will start counting their HIGH periods. The first IC to complete its HIGH period will again pull the SCL line LOW.

In this way, a synchronised SCL clock is generated with its LOW period determined by the IC with the longest clock LOW period, and its HIGH period determined by the one with the shortest clock HIGH period.

6.2 Arbitration (see also Appendix B)

Arbitration takes place on the SDA line in such a way that the master which transmits a HIGH level, while another master is transmitting a LOW level will

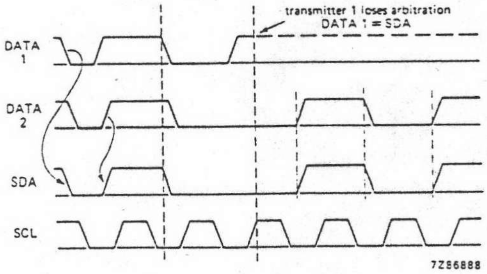


Fig.8 Arbitration procedure of two masters

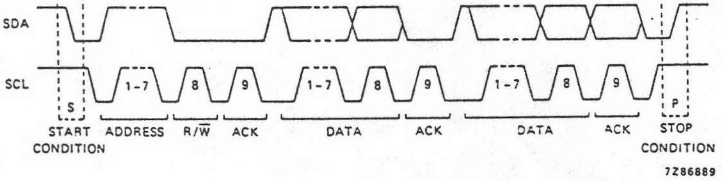


Fig.9 A complete data transfer

switch off its DATA output stage because the level on the bus doesn't correspond to its own level.

Arbitration can continue for many bits. Its first stage is comparison of the address bits (addressing information is in section 8.0). If the masters are each trying to address the same IC, arbitration continues with comparison of the data. Because address and data information on the I^{2}C-bus is used for arbitration, no information is lost during this process.

A master which loses the arbitration can generate clock pulses until the end of the byte in which it loses the arbitration.

If a master loses arbitration during the addressing stage, it's possible that the winning master is trying to address it. The losing master must therefore switch over immediately to its slave receiver mode.

Figure 8 shows the arbitration procedure for two masters. Of course, more may be involved (depending on how many masters are connected to the bus). The moment there is a difference between the internal data level of the master generating DATA 1 and the actual level on the SDA line, its data output is switched off, which means that a HIGH output level is then connected to the bus. This will not affect the data transfer initiated by the winning master. Since control of the I^{2}C-bus is decided solely on the address and data sent by competing masters, there is no central master, nor any order of priority on the bus.

6.3 Use of the clock synchronising mechanism as a handshake

In addition to being used during the arbitration procedure, the clock synchronization mechanism can be used to enable receivers to cope with fast data transfers, on either a byte level or a bit level.

On the byte level, an IC may be able to receive bytes of data at a fast rate, but needs more time to store a received byte or prepare another byte to be transmitted. Slaves can then hold the SCL line LOW after reception and acknowledgement of a byte to force the master into a wait state until the slave is ready for the next byte transfer in a type of handshake procedure.

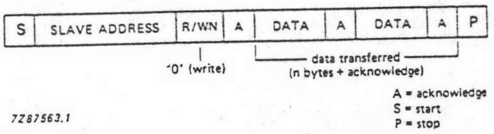
On the bit level, an IC such as a microcomputer without a hardware I^{2}C interface on-chip can slow down the bus clock by extending each clock LOW period. In this way, the speed of any master is adapted to the internal operating rate of this IC.

7.0 Formats

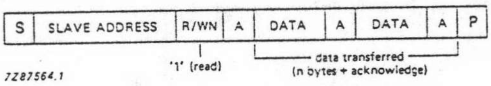
Data transfers follow the format shown in Fig.9. After the START condition, a slave address is sent. This address is 7 bits long, the eighth bit is a data direction bit (R/$\overline{W}$) - a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition generated by the master. However, if a master still wishes to communicate on the bus, it can generate another START condition and address another slave without first generating a STOP condition. Various combinations of read/write formats are then possible within such a transfer.

Possible data transfer formats are:

a) Master transmitter transmits to slave receiver. Direction is not changed.



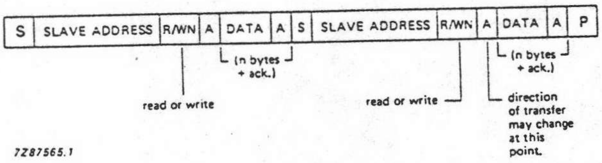
b) Master reads slave immediately after first byte.



At the moment of the first acknowledge, the master transmitter becomes a master receiver and the slave receiver becomes a slave transmitter. This acknowledge is still generated by the slave.

The STOP condition is generated by the master.

c) Combined formats.



During a change of direction within a transfer, the START condition and the slave address are both repeated, but with the R/$\overline{W}$ bit reversed.

NOTES:

1) Combined formats can be used, for example, to control a serial memory. During the first data byte, the internal memory location has to be written. After the START condition is repeated, data can be transferred.

2) All decisions on auto-increment or decrement of previously accessed memory locations etc. are taken by the designer of the IC.

3) Each byte is followed by an acknowledge as indicated by the A blocks in the sequence.

4) I^2C-bus compatible ICs must reset their bus logic on receipt of a START condition such that they all anticipate the sending of a slave address.

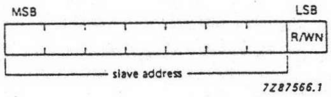


Fig.10 The first byte after the start procedure

8.0 Addressing

The addressing procedure for the I^{2}C-bus is such that the first byte after the START condition determines which slave will be selected by the master. Usually, this first byte follows that start procedure. The exception is the 'general call' address which can address all ICs. When this address is used, all ICs should, in theory, respond with an acknowledge. However, ICs can be made to ignore this address. The second byte of the general call address then defines the action to be taken.

8.1 Definition of bits in the first byte

The first seven bits of the first byte make up the slave address (Fig.10). The eighth bit is the LSB (least significant bit). It determines the direction of the message. A 'zero' in the least significant position of the first byte means that the master will write information to a selected slave. A 'one' in this position means that the master will read information from the slave.

When an address is sent, each IC in a system compares the first 7 bits after the START condition with its address. If they match, the IC considers itself addressed by the master as a slave receiver or slave transmitter, depending on the R/$\overline{W}$ bit.

A slave address can be made-up of a fixed and a programmable part. Since it's likely that there will be several identical ICs in a system, the programmable part of the slave address enables the maximum possible number of such ICs to be connected to the I^{2}C-bus. The number of programmable address bits of an IC depends on the number of pins available. For example, if an IC has 4 fixed and 3 programmable address bits, a total of 8 identical ICs can be connected to the same bus.

The I^{2}C-bus committee coordinates allocation of I^{2}C addresses. The bit combination 1111XXX of the slave address is reserved for future extension purposes. Address 1111111 is reserved as the extension address. This means that the addressing procedure will be continued in the next byte(s). ICs that don't use the extended addressing don't react on reception of this byte. The seven other possibilities in group 1111 will also only be used for extension purposes but are not yet allocated. Combination 0000XXX has been defined as a special group. The following addresses have been allocated (also see notes on next page):

first byte			
SLAVE ADDRESS	R/$\overline{W}$		
0000 000	0	general call address	see NOTES on page 15
0000 000	1	start byte	
0000 001	X	CBUS address	
0000 010	X	Address reserved for different bus format	
0000 011	X	to be defined	
0000 100	X		
0000 101	X		
0000 110	X		
0000 111	X		

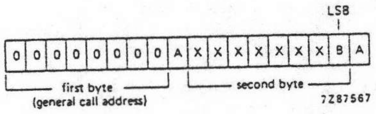


Fig.11 General call address format

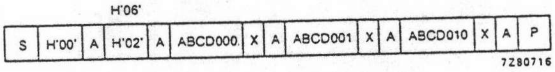


Fig.12 Sequence of a programming master

NOTES:

1) No IC is allowed to acknowledge at the reception of the START byte.

2) The CBUS address has been reserved to enable the inter-mixing of CBUS compatible and I^2C-bus compatible ICs in the same system. I^2C-bus compatible ICs are not allowed to respond on reception of this address.

3) The address reserved for a different bus format is included to enable I^2C and other protocols to be mixed. Only I^2C-bus compatible ICs that can work with such formats and protocols are allowed to respond to this address.

8.1.1 General call address

The general call address should be used to address every IC connected to the I^2C-bus. However, if an IC doesn't need any of the data supplied within the general call structure, it can ignore this address by not acknowledging. If an IC does require data from a general call address, it will acknowledge this address and behave as a slave receiver. The second and following bytes will be acknowledged by every slave receiver capable of handling this data. A slave which cannot process one of these bytes must ignore it by not acknowledging. The meaning of the general call address is always specified in the second byte (Fig.11).

There are two cases to consider:

- When the least significant bit B is a 'zero'.
- When the least significant bit B is a 'one'.

When B is a 'zero'; the second byte has the following definition:

00000110 (H'06') Reset and write programmable part of slave address by software and hardware. On receiving this 2-byte sequence, all ICs designed to respond to the general call address will reset and take in the programmable part of their address. Precautions have to be taken to ensure that an IC is not pulling down the SDA or SCL line after applying the supply voltage, since these low levels would block the bus.

00000010 (H'02') Write slave address by software only. All ICs which obtain the programmable part of their address by software (and which have been designed to respond to the general call address) will enter a mode in which they can be programmed. The IC will not reset. An example of a data transfer of a programming master is shown in Fig.12 (ABCD represents the fixed part of the address).

00000100 (H'04') Write slave address by hardware only. All ICs which define the programmable part of their address by hardware (and which respond to the general call address) will latch this programmable part at the reception of this two byte sequence. The IC will not reset.

00000000 (H'00') This code is not allowed to be used as the second byte. Sequences of programming procedure are published in the appropriate IC data sheets.

The remaining codes have not been fixed and ICs must ignore them.

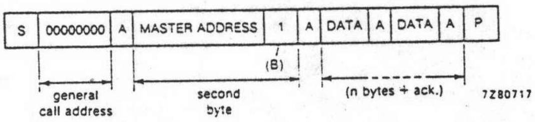


Fig.13 Data transfer from a hardware master transmitter

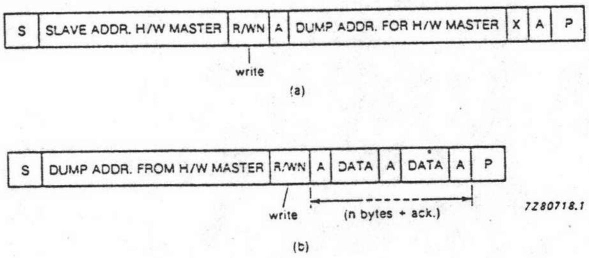


Fig.14 Data transfer by a hardware transmitter capable of dumping data directly to slave ICs

(a) Configuring master sends dump address to hardware master

(b) Hardware master dumps data to selected slave

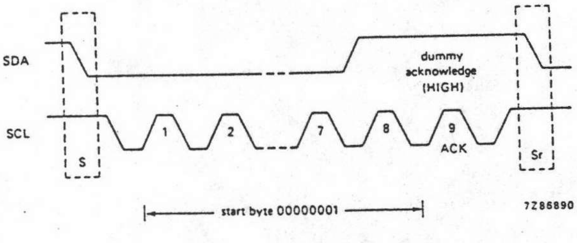


Fig.15 Start byte procedure

When B is a 'one'; the 2-byte sequence is a 'hardware general call'. This means that the sequence is transmitted by a hardware master IC, such as a keyboard scanner, which cannot be programmed to transmit a desired slave address. Since a hardware master doesn't know in advance to which IC the message has to be transferred, it can only generate this hardware general call and its own address - identifying itself to the system (Fig.13).

The seven bits remaining in the second byte contain the address of the hardware master. This address is recognised by an intelligent IC, such as a microcomputer, connected to the bus which will then direct the information from the hardware master. If the hardware master can also act as a slave, the slave address is identical to the master address.

In some systems, an alternative could be that the hardware master transmitter is set in the slave receiver mode after the system reset. In this way, a system configuring master can tell the hardware master transmitter (which is now in slave receiver mode) to which address data must be sent (Fig.14). After this programming procedure, the hardware master remains in the master transmitter mode.

8.1.2 start byte

Microcomputers can be connected to the I^{2}C-bus in two ways. A microcomputer with an on-chip hardware I^{2}C-bus interface can be programmed to be only interrupted by requests from the bus. When the IC doesn't have such an interface, it must constantly monitor the bus via software. Obviously, the more times the microcomputer monitors, or polls, the bus the less time it can spend carrying out its intended function. There is therefore a speed difference between fast hardware ICs and a relatively slow microcomputer which relies on software polling.

In this case, data transfer can be preceded by a start procedure which is much longer than normal (Fig.15). The start procedure consists of:

a) A START condition S

b) A start byte 00000001

c) An acknowledge clock pulse

d) A repeated START condition Sr

After the START condition S has been transmitted by a master which requires bus access, the start byte (00000001) is transmitted. Another microcomputer can therefore sample the SDA line at a low sampling rate until one of the seven zeros in the start byte is detected. After detection of this LOW level on the SDA line, the microcomputer can switch to a higher sampling rate to find the repeated START condition Sr which is then used for synchronization.

A hardware receiver will reset on receipt of the repeated START condition Sr and will therefore ignore the start byte.

An acknowledge-related clock pulse is generated after the start byte. This is present only to conform with the byte handling format used on the bus. No IC is allowed to acknowledge the start byte.

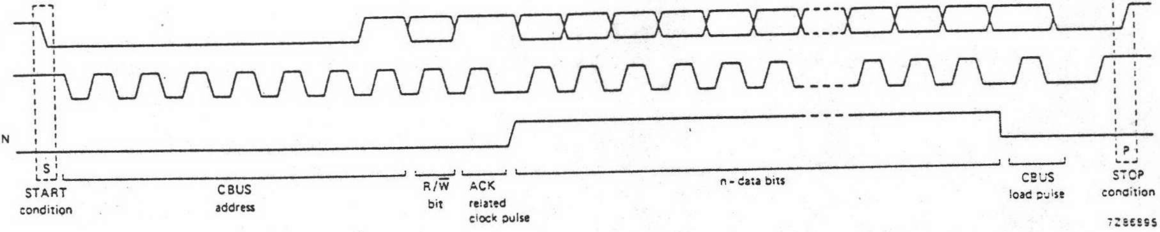


Fig.16 Data format of transmissions with CBUS receiver/transmitter

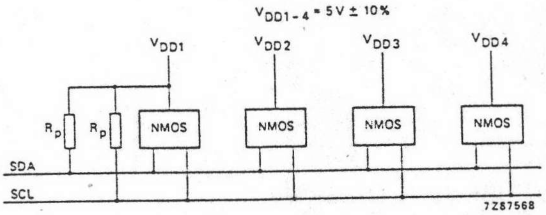


Fig.17 Fixed input level ICs connected to the I^2C-bus

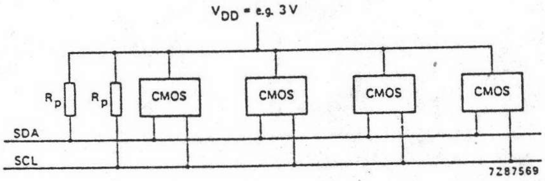


Fig.18 ICs with a wide range of supply voltages connected to the I^2C-bus

8.1.3 CBUS compatibility

Existing CBUS receivers can be connected to the I^2C-bus. However, in this case, a third line called DLEN has to be connected and the acknowledge bit omitted. Normally, I^2C transmissions are sequences of 8-bit bytes; CBUS compatible ICs have different formats however.

In a mixed bus structure, I^2C-bus compatible ICs are not allowed to respond to the CBUS message. For this reason, a special CBUS address (0000001X) to which no I^2C-bus compatible IC will respond, has been reserved. After transmission of the CBUS address, the DLEN line can be made active and transmission, according to the CBUS format, can be performed (Fig.16). After the STOP condition, all ICs are again ready to accept data.

Master transmitters are allowed to generate CBUS formats after having sent the CBUS address. Such a transmission is terminated by a STOP condition, recognised by all ICs. In the 'low speed' mode (see Section 11.0), full 8-bit bytes must always be transmitted and the timing of the DLEN signal adapted.

NOTE: If the CBUS configuration is known, and expansion with CBUS compatible ICs isn't foreseen, the designer is allowed to adapt the hold time to the specific requirements of IC(s) used.

9.0 Electrical specifications of inputs and outputs of I^2C interfaces

The I^2C-bus allows communication between ICs fabricated in different technologies which might also operate from different supply voltages. For interfaces with fixed input levels, operating on a supply voltage of 5 V ± 10%, the following levels have been defined:

$V_{IL\ max}$ = 1.5 V (maximum input LOW voltage)

$V_{IH\ min}$ = 3.0 V (minimum input HIGH voltage)

Interfaces in ICs operating from a fixed supply voltage other than 5 V (e.g. I^2L ICs), must also have these input levels of 1.5 V and 3.0 V for V_{IL} and V_{IH} respectively.

For ICs capable of operating from a wide range of supply voltages (e.g. CMOS ICs), the following levels have been defined:

$V_{IL\ max}$ = 0.3 V_{DD} (maximum input LOW voltage)

$V_{IH\ min}$ = 0.7 V_{DD} (minimum input HIGH voltage)

The maximum output LOW level for both groups is:

$V_{OL\ max}$ = 0.4 V at 3 mA sink current.

The maximum LOW level input current at $V_{OL\ max}$ of both the SDA and SCL pin of an I^2C-bus compatible IC is -10 μA, including the leakage current of a possible output stage.

The maximum HIGH level input current at 90% V_{DD} for both the SDA and SCL pin of an I^2C-bus compatible IC is 10 μA, including the leakage current of a possible output stage.

The maximum capacitance of both the SDA and SCL pin of an I^2C-bus compatible IC is 10 pF.

I^2C interfaces with fixed input levels can each have their own power supply of 5 V ± 10%. Pull-up resistors can be connected to any supply (Fig.17). However, I^2C

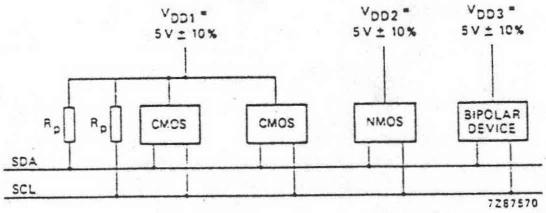


Fig.19 Interfaces with input levels related to V_{DD} mixed with fixed input level interfaces on the I^2C-bus

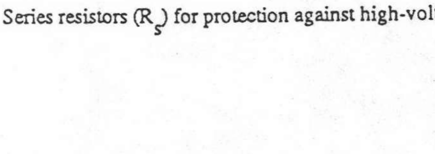


Fig.20 Series resistors (R_s) for protection against high-voltage spikes

interfaces with input levels related to V_{DD} must have one common supply line to which the pull-up resistor is also connected (Fig.18).

When ICs having interfaces with fixed input levels are mixed with ICs which have interfaces with input levels related to V_{DD}, the latter ICs must be connected to one common supply line of 5 V ± 10% and must have pull-up resistors connected to their SDA and SCL pins as shown in Fig.19.

Input levels are defined in such a way that:

1) The noise margin on the LOW level is 0.1 V_{DD}.

2) The noise margin on the HIGH level is 0.2 V_{DD}.

3) Series resistors (R_S) up to 300 Ω can be used for protection against high voltage spikes on the SDA and SCL line due to flash-over of a TV picture tube, for example (Fig.20).

The maximum bus capacitance per wire is 400 pF. This includes the capacitance of the wire itself and the capacitance of the pins connected to it.

10.0 Timing

The clock on the I^2C-bus has a minimum LOW period of 4.7 μs and a minimum HIGH period of 4 μs. Masters in this mode can generate a bus clock with a frequency up to 100 kHz.

All ICs connected to the bus must be able to follow transfers with frequencies up to 100 kHz, either by being able to transmit or receive at that speed or by applying the clock synchronization procedure which will force the master into a wait state and stretch the LOW periods. Of course, in the latter case the frequency is reduced.

Figure 21 shows the timing requirements in detail, a description of the abbreviations used is shown in the following Table. All timing references are at $V_{IL\ max}$ and $V_{IH\ min}$.

parameter	symbol	min.	max.	units
SCL clock frequency	f_{SCL}	0	100	kHz
Time the bus must be free before a new transmission can start	t_{BUF}	4.7	-	µs
Hold time START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	-	µs
LOW period of the clock	t_{LOW}	4.7	-	µs
HIGH period of the clock	t_{HIGH}	4.0	-	µs
Set-up time for START condition (Only relevant for a repeated START condition)	$t_{SU;STA}$	4.7	-	µs
Hold time DATA	$t_{HD;DAT}$			
for CBUS compatible masters (see NOTE, Section 8.1.3)		5	-	µs
for I^{2}C ICs		0*	-	µs
Set-up time DATA	$t_{SU;DAT}$	250	-	ns
Rise time of both SDA and SCL lines	t_R	-	1	µs
Fall time of both SDA and SCL lines	t_F	-	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.7	-	µs

All values referred to V_{IH} and V_{IL} levels (see section 9.0).

* Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max. 300 ns) of the falling edge of SCL.

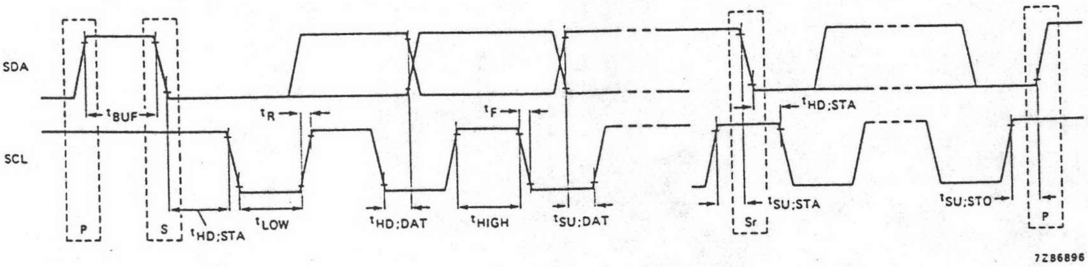


Fig.21 Timing requirements for the I^{2}C-bus

11.0 'Low speed' mode

As explained in section 8.1.2, there is a difference in speed on the I^2C-bus between fast hardware interfaces and a relatively slow microcomputer which relies on software polling. For this reason a 'low speed' mode is available on the I^2C-bus to allow these microcomputers to poll the bus less often.

11.1 START and STOP conditions

In the 'low speed' mode, data transfer is preceded by the start procedure of section 8.1.2.

11.2 Data format and timing

The bus clock in this mode has a LOW period of 130 µs ± 25 µs and a HIGH period of 390 µs ± 25 µs, resulting in a clock frequency of about 2 kHz. This clock duty cycle allows for more efficient use of microcomputers without an on-chip hardware I^2C-bus interface. Also in this mode, data transfer with acknowledge is obligatory. the maximum number of bytes transferred is unlimited (Fig.22).

In this mode, a transfer cannot be terminated during the transmission of a byte.

Clock:	t_{LOW} = 130µs ± 25µs t_{HIGH} = 390 µs ± 25µs
Duty cycle:	1:3 LOW to HIGH (Duty cycle of clock generator)
Start byte:	0000 0001
Max. number of bytes:	unrestricted
premature termination: of transfer:	not allowed
acknowledge clock bit:	always provided
acknowledgement of slaves:	obligatory

The bus is considered to be busy after the first START condition. It is considered to be free again one minimum clock LOW period (105 µs) after detection of the STOP condition. Figure 23 shows the timing requirements in detail and the following Table explains the abbreviations.

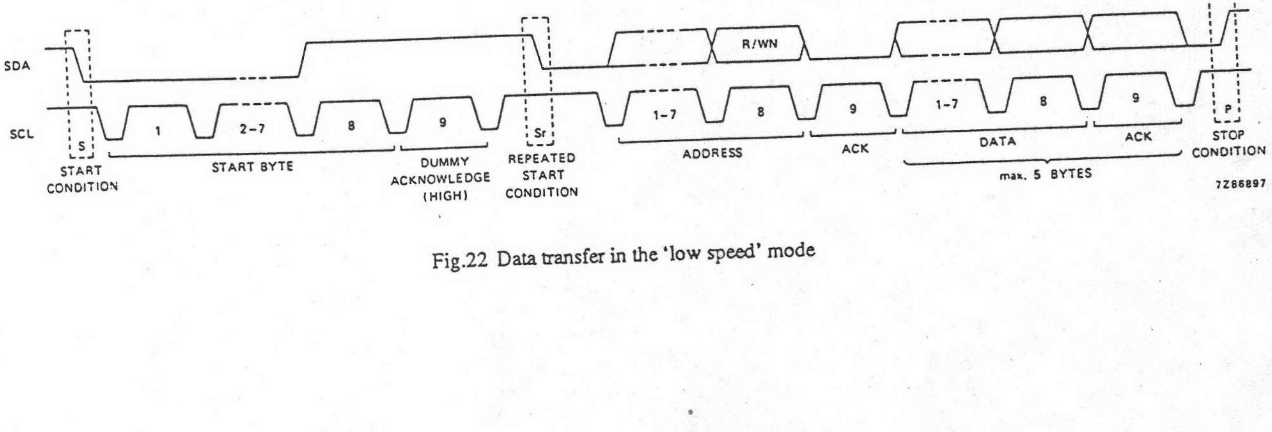


Fig.22 Data transfer in the 'low speed' mode

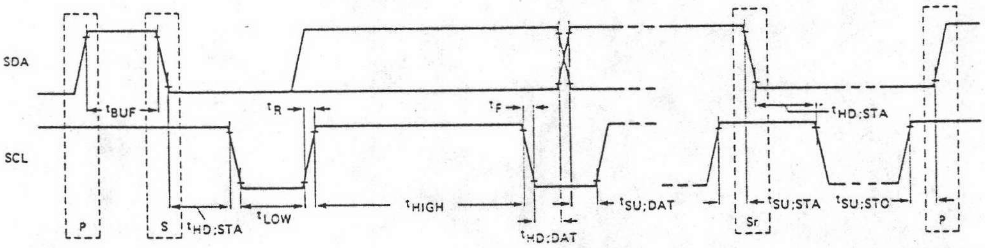


Fig.23 Timing in the 'low speed' mode

parameter	symbol	min.	max.	units
Time the bus must be free before a new transmission can start	t_{BUF}	105	-	µs
Hold time START condition. After this period the first clock pulse is generated	$t_{HD;STA}$	365	-	µs
Hold time (repeated START condition only)	$t_{HD;STA}$	210	-	µs
LOW period of the clock	t_{LOW}	105	155	µs
HIGH period of the clock	t_{HIGH}	365	415	µs
Set up time for START condition (Only relevant for a repeated START condition)	$t_{SU;STA}$	105	155	µs
Hold time DATA	$t_{HD;DAT}$			
for CBUS compatible masters (see also NOTE, Section 8.1.3)		5	-	µs
for I^2C ICs		0*	-	µs
Set-up time DATA	$t_{SU;DAT}$	250	-	ns
Rise time of both SDA and SCL lines	t_R	-	1	µs
Fall time of both SDA and SCL lines	t_F	-	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	105	155	µs

All values referred to V_{IH} and V_{IL} levels (see section 9.0).

* Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max. 300 ns) of the falling edge of SCL.

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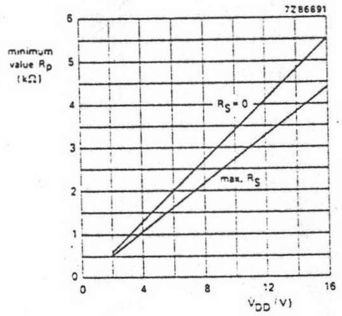
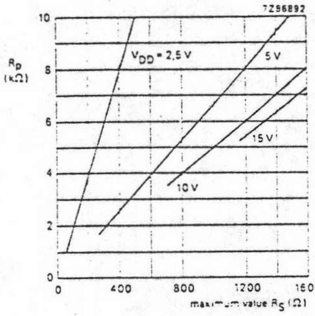
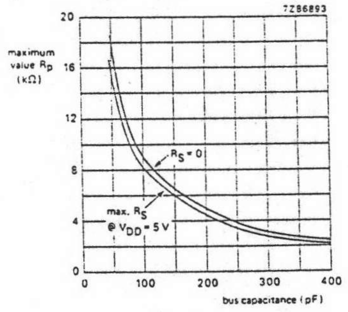


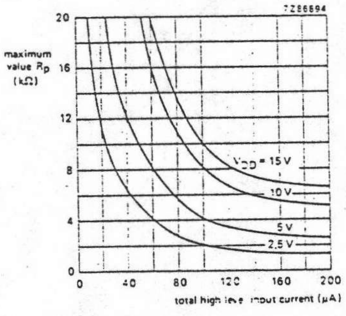
7Z86691
minimum value R_p (kΩ)
0
1
2
3
4
5
6
$R_S = 0$
max. R_S
0
4
8
12
16
V_{DD} (V)



7Z96892
R_p (kΩ)
0
2
4
6
8
10
V_{DD} = 2,5 V
5 V
15 V
10 V
0
400
800
1200
1600
maximum value R_S (Ω)



7Z86893
maximum value R_p (kΩ)
0
4
8
12
16
20
$R_S = 0$
max. R_S @ V_{DD} = 5 V
0
100
200
300
400
bus capacitance (pF)



7Z86894
maximum value R_p (kΩ)
0
4
8
12
16
20
V_{DD} = 15 V
10 V
5 V
2,5 V
0
40
80
120
160
200
total high level input current (μA)

Appendix A - Values of resistors R_p and R_s in Fig.20

In an I^{2}C-bus system these values depend on the following parameters:

1) Supply voltage

2) Bus capacitance

3) Number of connected ICs (input current + leakage current)

1) The supply voltage limits the minimum value of resistor R_p due to the specified minimum sink current of 3 mA at V_{OLmax} = 0.4 V for the output stages. V_{DD} as a function of $R_{p\ min}$ is shown in a graph on the facing page. The desired noise margin of 10% 0f V_{DD} for the LOW level limits the maximum value of R_s. $R_{S\ max}$ as a function of R_p is shown in another graph on the facing page.

2) The bus capacitance is the total capacitance of wire, connections and pins. This capacitance limits the maximum value of R_p due to the specified rise time of 1 µsec. A graph on the facing page shows $R_{p\ max}$ as a function of bus capacitance.

3) The maximum HIGH level input current of each input/output connection has a specified maximum value of 10 µA. Due to the desired noise margin of 20% of V_{DD} for the HIGH level, this input current limits the maximum value of R_p. This limit depends on V_{DD}. The total HIGH level input current is shown as a function of R_p max in a graph on the facing page.

Appendix B - Note to section 6.2

Special attention must be paid if, during a serial transfer, the arbitration procedure is still in progress at the moment when a repeated START condition or a STOP condition is transmitted to the I^{2}C-bus. If it's possible for such a situation to occur, the masters involved must send this repeated START condition or STOP condition at the same position in the format frame. In other words, arbitration isn't allowed between:

- a repeated START condition and a data bit,
- a STOP condition and a data bit,
- a repeated START condition and a STOP condition.

ภาคผนวก ข.

Data Sheet

TELETEXT VIDEO PROCESSOR

GENERAL DESCRIPTION

The SAA5231 is a bipolar integrated circuit intended as a successor to the SAA5030. It extracts Teletext Data from the video signal, regenerates Teletext Clock and synchronizes the text display to the television syncs. The integrated circuit is intended to work in conjunction with CCT (Computer Controlled Teletext), EUROM or other compatible devices.

Features

- Adaptive data slicer
- Data clock regenerator
- Adaptive sync separator, horizontal phase detector and 6 MHz VCO forming display phase locked loop (PLL)

QUICK REFERENCE DATA

Supply voltage (pin 16)	V_{CC}	typ.	12	V
Supply current (pin 16)	I_{CC}	typ.	70	mA
Video input amplitude (pin 27) (peak-to-peak value)				
pin 2 LOW	$V_{27\text{-}13(p\text{-}p)}$	typ.	1	V
pin 2 HIGH	$V_{27\text{-}13(p\text{-}p)}$	typ.	2,5	V
Storage temperature range	T_{stg}		−20 to + 125	°C
Operating ambient temperature range	T_{amb}		0 to + 70	°C

PACKAGE OUTLINE

28-lead dual in-line; plastic (SOT117).

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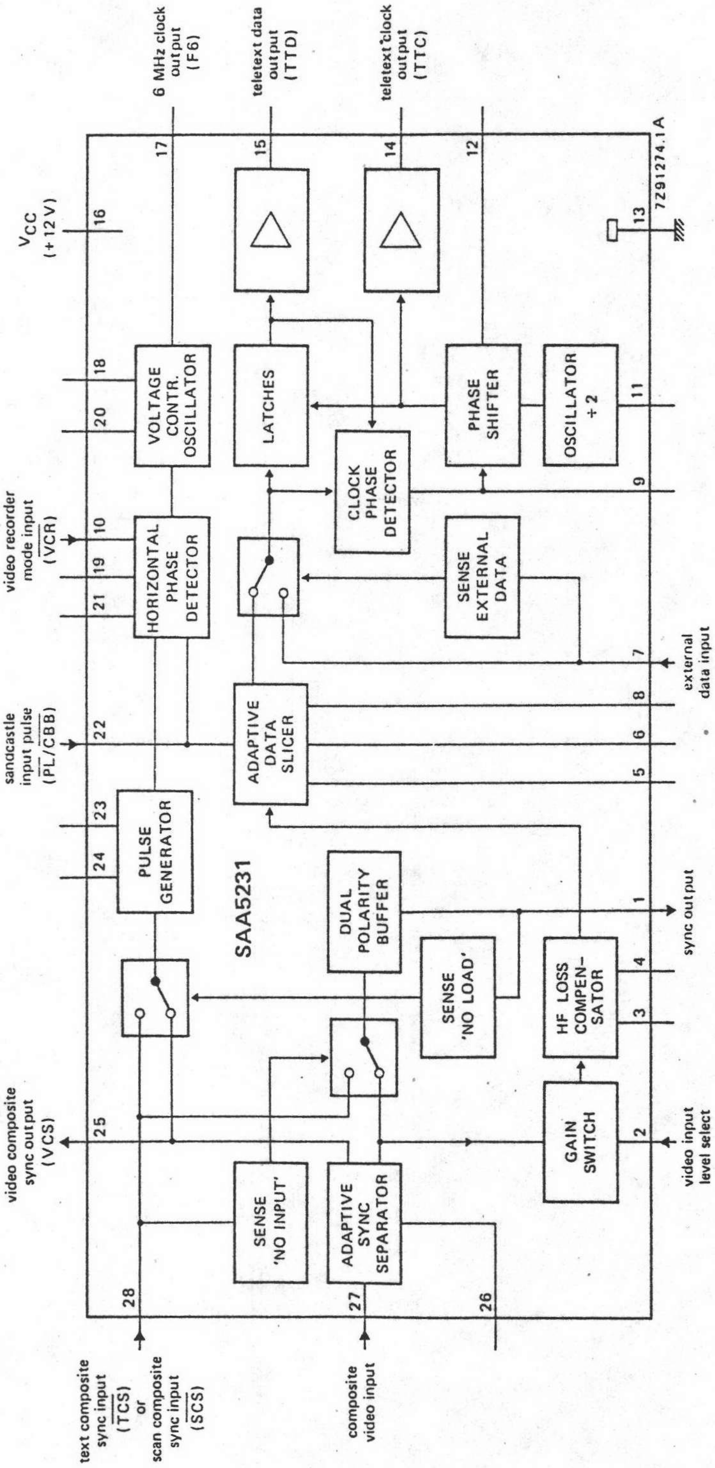

Fig. 1 Block diagram.

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PINNING

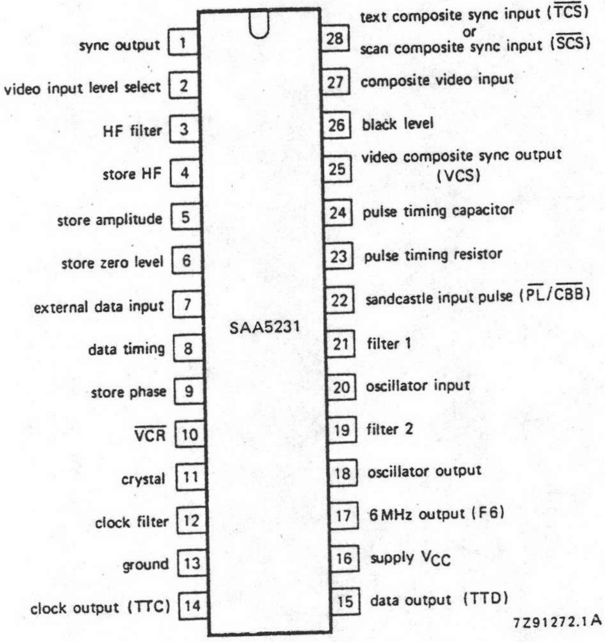

Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 16)	V_{CC}	max.	13,2 V
Storage temperature range	T_{stg}		−20 to + 125 °C
Operating ambient temperature	T_{amb}		0 to + 70 °C

CHARACTERISTICS

V_{CC} = 12 V; T_{amb} = 25 °C with external components as shown in application circuits unless otherwise stated.

parameter	symbol	min.	typ.	max.	unit
Supply (pin 16)					
Supply voltage	V_{CC}	10,8	12,0	13,2	V
Supply current	I_{CC}	50	70	105	mA
Video input and sync separator					
Video input amplitude (sync to white) (peak-to-peak value)					
video input select level LOW (pin 2)	$V_{27\text{-}13(p\text{-}p)}$	0,7	1	1,4	V
video input select level HIGH (pin 2)	$V_{27\text{-}13(p\text{-}p)}$	1,75	2,5	3,5	V
Source impedance	$\|Z_s\|$	–	–	250	Ω
Sync amplitude (peak-to-peak value)	$V_{27\text{-}13(p\text{-}p)}$	0,1	–	1	V
Video input level select					
Input voltage LOW	$V_{2\text{-}13}$	0	–	0,8	V
Input voltage HIGH	$V_{2\text{-}13}$	2,0	–	5,5	V
Input current LOW	I_2	0	–	−150	μA
Input current HIGH	I_2	0	–	1	mA
Text composite sync input ($\overline{TCS}$)					
Input voltage LOW	$V_{28\text{-}13}$	0	–	0,8	V
Input voltage HIGH	$V_{28\text{-}13}$	2,0	–	7,0	V
Scan composite sync input ($\overline{SCS}$)					
Input voltage LOW	$V_{28\text{-}13}$	0	–	1,5	V
Input voltage HIGH	$V_{28\text{-}13}$	3,5	–	7,0	V
Select video sync from pin 1					
Input current (pin 28)					
at V_{28} = 0 to 7 V	I_{28}	−40	−70	−100	μA
at V_{28} = 10 V to V_{CC}	I_{28}	−5	–	+ 5	μA
Video composite sync output (VCS)					
Output voltage LOW	$V_{25\text{-}13}$	0	–	0,4	V
Output voltage HIGH	$V_{25\text{-}13}$	2,4	–	5,5	V
D.C. output current LOW	I_{25}	–	–	0,5	mA
D.C. output current HIGH	I_{25}	–	–	−1,5	mA
Sync separator delay time	t_d	0,25	0,35	0,40	μs

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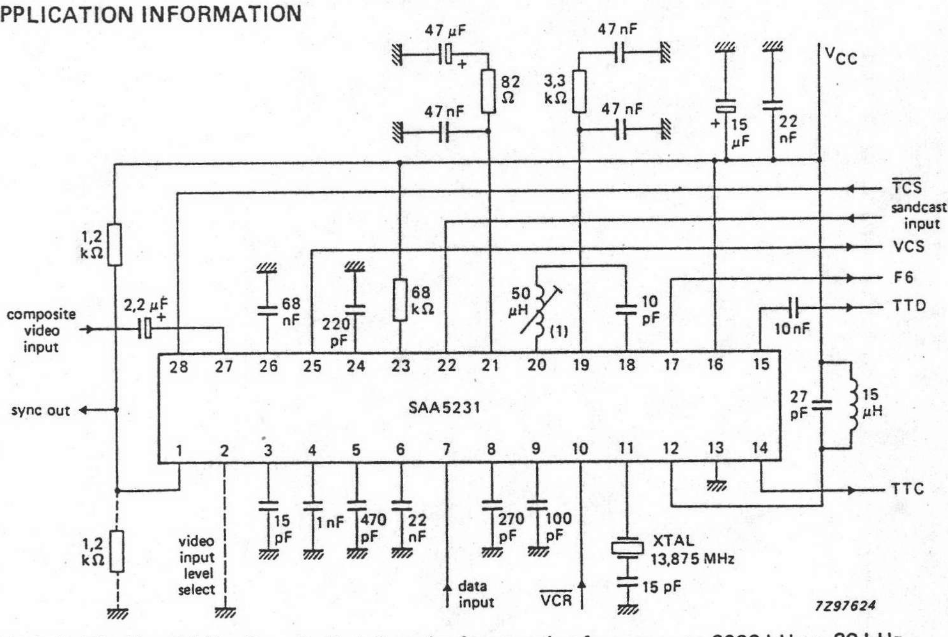
parameter	symbol	min.	typ.	max.	unit
Dual polarity buffer output					
$\overline{TCS}$ amplitude (peak-to-peak value)	$V_{1\text{-}13(p\text{-}p)}$	0,20	0,45	0,65	V
Video sync amplitude (peak-to-peak value)	$V_{1\text{-}13(p\text{-}p)}$	–	–	1	V
Output current	I_1	–3	–	+ 3	mA
D.C. output voltage					
R_L to ground (0 V)	$V_{1\text{-}13}$	1,0	1,4	2,0	V
R_L to V_{CC} (12 V)	$V_{1\text{-}13}$	9,0	10,1	11,0	V
Sandcastle input pulse ($\overline{PL}/\overline{CBB}$)					
Phase lock pulse (PL)					
PL on (LOW)	$V_{22\text{-}13}$	0	–	3	V
PL off (HIGH)	$V_{22\text{-}13}$	3,9	–	5,5	V
Blanking pulse (CBB)					
CBB on (LOW)	$V_{22\text{-}13}$	0	–	0,5	V
CBB off (HIGH)	$V_{22\text{-}13}$	1,0	–	5,5	V
Input current	I_{22}	–10	–	+ 10	μA
Phase locked loop (PLL)					
Phase detector timing					
Pulse duration using composite video	t_p	2,0	2,4	2,8	μs
using scan composite sync	t_p	3,0	3,5	4,0	μs
time PL must be LOW to make VCO run-free	t_L	100	–	–	μs
6 MHz clock output (F6)					
A.C. output voltage (peak-to-peak value)	$V_{17\text{-}13(p\text{-}p)}$	1	2	3	V
A.C. and d.c. output voltage range	$V_{17\text{-}13(max)}$	4	–	8,5	V
Rise and fall time	$t_r; t_f$	20	–	40	ns
Load capacitance	$C_{17\text{-}13}$	–	–	40	pF
Video recorder mode input ($\overline{VCR}$)					
VCR-mode on (LOW)	$V_{10\text{-}13}$	0	–	0,8	V
VCR-mode off (HIGH)	$V_{10\text{-}13}$	2,0	–	V_{CC}	V
Input current	I_{10}	–10	–	+ 10	μA

parameter	symbol	min.	typ.	max.	unit
Data slicer					
Data amplitude of video input (pin 27)					
video input level select LOW (pin 2)	V_{27-13}	0,30	0,46	0,70	V
video input level select HIGH (pin 2)	V_{27-13}	0,75	1,15	1,75	V
Teletext clock output					
A.C. output voltage (peak-to-peak value)	$V_{14-13(p-p)}$	2,5	3,5	4,5	V
D.C. output voltage (centre)	V_{14-13}	3,0	4,0	5,0	V
Load capacitance	C_L	–	–	40	pF
Rise and fall times	t_r; t_f	20	30	45	ns
Delay of falling edge relative to other edges of TTD	t_d	–20	0	+ 20	ns
Teletext data output					
A.C. output voltage (peak-to-peak value)	$V_{15-13(p-p)}$	2,5	3,5	4,5	V
D.C. output voltage (centre)	V_{15-13}	3,0	4,0	5,0	V
Load capacitance	C_L	–	–	40	pF
Rise and fall times	t_r; t_f	20	30	45	ns

APPLICATION INFORMATION



(1) Coil: 50 µH at 1 kHz, C_o = 4 pF. Adjust the free-running frequency to 6000 kHz ± 30 kHz.

Fig. 3a Application circuit using L/C circuit in PLL.

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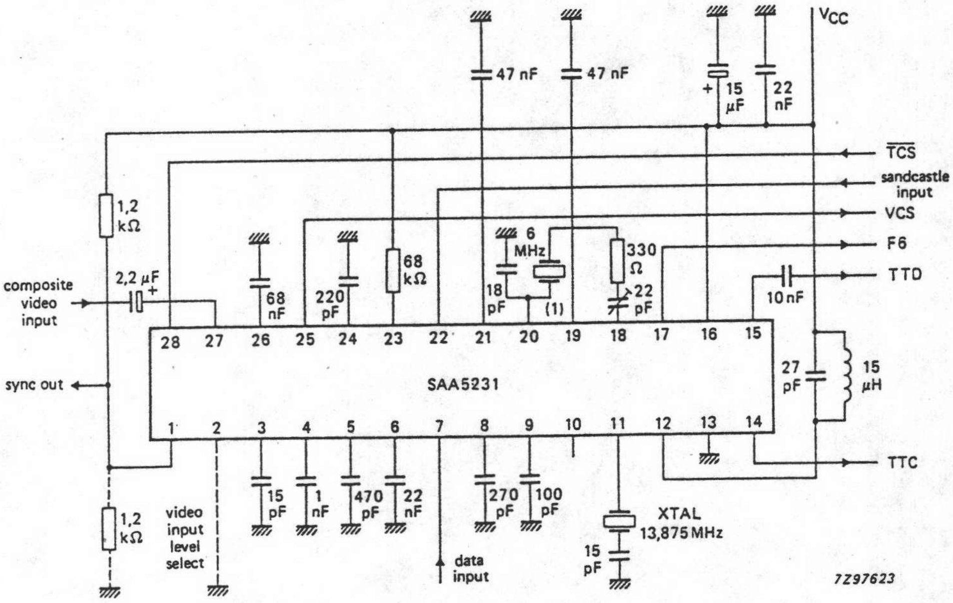
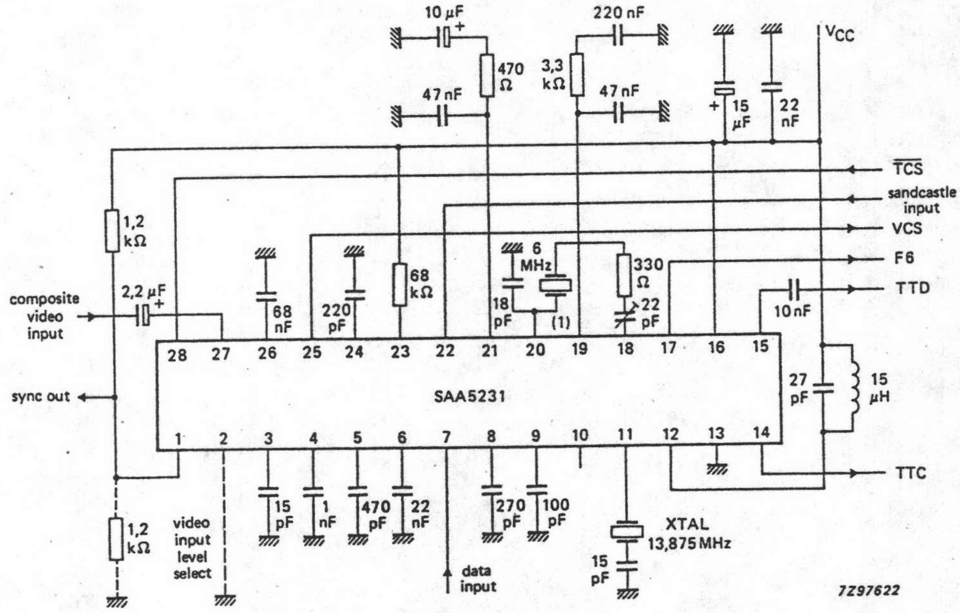


(1) Quartz crystal e.g. catalogue number 4322 143 04101. Adjust the free-running frequency to 6000,2 kHz ± 0,2 kHz.

Fig. 3b Application circuit using quartz crystal in PLL.



(1) Ceramic resonator e.g. Kyocera KBR 6,0 M. Adjust the free-running frequency to 6010 kHz ± 5 kHz.

Fig. 3c Application circuit using ceramic resonator in PLL.

Component specifications

Specifications of some external components in Figs 3a, 3b and 3c.

Quartz crystal 13,875 MHz; Figs 3a, 3b and 3c

Load resonance frequency (f) 13,875 MHz; adjustment tolerance ± $40 \cdot 10^{-6}$

Load capacitance (C_L) 20 pF

Temperature range (T) −20 to +70 °C; frequency tolerance maximum ± $30 \cdot 10^{-6}$

Resonance resistance (R_r) typical 10 Ω maximum 60 Ω

Motional capacitance (C_1) typical 19 fF

Static parallel capacitance (C_o) typical 5 pF

Fixed inductance Figs 3a, 3b and 3c

Inductance (L) 15 μH ± 20%

Quality factor (Q) minimum 20

Variable inductance Fig. 3a

Inductance (L) 50 μH at 1 kHz

Static parallel capacitance (C_o) typical 4 pF

Quartz crystal Fig. 3b

Preferred type 4322 143 04101

Load resonance frequency (f) 6 MHz; adjustment tolerance ± $40 \cdot 10^{-6}$

Load capacitance (C_L) 20 pF

Temperature range (T) −20 to +70 °C; frequency tolerance ± $30 \cdot 10^{-6}$

Resonance resistance (R_r) 60 Ω

Motional capacitance (C_1) typical 28 fF

Static parallel capacitance (C_o) typical 7 pF

Ceramic resonator; Fig. 3c

Preferred type KBR 6,0 M, Kyocera

Load resonance frequency (f) 6 MHz; adjustment tolerance ± 0,5%

Load capacitance (C_L) 20 pF

Temperature range (T) −20 to +70 °C; frequency tolerance maximum ± 0,3%

Resonance resistance (R_r) typical 6 Ω

Motional capacitance (C_1) typical 9 pF

Static parallel capacitance (C_o) typical 60 pF

Ageing (10 years) f maximum ± 0,3%

The function is quoted against the corresponding pin number.

1. **Synch output to TV**

   Output with dual polarity buffer, a load resistor to 0 V or + 12 V selects positive-going or negative-going syncs.

2. **Video input level select**

   When this pin is LOW a 1 V video input level is selected. When the pin is not connected it floats HIGH selecting a 2,5 V video input level.

3. **HF filter**

   The video signal for the h.f.-loss compensator is filtered by a 15 pF capacitor connected to this pin.

4. **Store h.f.**

   The h.f. amplitude is stored by a 1 nF capacitor connected to this pin.

5. **Store amplitude**

   The amplitude for the adaptive data slicer is stored by a 470 pF capacitor connected to this pin.

6. **Store zero level**

   The zero level for the adaptive data slicer is stored by a 22 nF capacitor connected to this pin.

7. **External data input**

   Current input for sliced teletext data from external device.
   Active HIGH level (current), low impedance input.

8. **Data timing**

   A 270 pF capacitor is connected to this pin for timing of the adaptive data slicer.

9. **Store phase**

   The output signal from the clock phase detector is stored by a 100 pF capacitor connected to this pin.

10. **Video tape recorder mode ($\overline{\text{VCR}}$)**

    Signal input to command PLL into short time constant mode. Not used in application circuit Fig. 3b or Fig. 3c.

11. **Crystal**

    A 13,875 MHz crystal, 2 x data rate, connected in series with a 15 pF capacitor is applied via this pin to the oscillator and divide-by-two to provide the 6,9375 MHz clock signal.

12. **Clock filter**

    A filter for the 6,9375 MHz clock signal is connected to this pin.

13. **Ground (0 V)**

14. **Teletext clock output (TTC)**

    Clock output for CCT (Computer Controlled Teletext).

APPLICATION INFORMATION (continued)

15. **Teletext data output (TTD)**

    Data output for CCT.

16. **Supply voltage V_{CC} (+ 12 V typ.)**

17. **Clock output (F6)**

    6 MHz clock output for timing and sandcastle generation in CCT.

18. **Oscillator output (6 MHz)**

    A series resonant circuit is connected between this pin and pin 20 to control the nominal frequency of the VCO.

19. **Filter 2**

    A filter with a short time constant is connected to this pin for the horizontal phase detector. It is used in the video recorder mode and while the loop is locking up.

20. **Oscillator input (6 MHz)**

    See pin 18.

21. **Filter 1**

    A filter with a long time constant is connected to this pin for the horizontal phase detector.

22. **Sandcastle input pulse ($\overline{PL}/\overline{CBB}$)**

    This input accepts a sandcastle waveform, which is formed from PL and CBB from the CCT. Signal timing is shown in Fig. 4.

23. **Pulse timing resistor**

    The current for the pulse generator is defined by a 68 kΩ resistor connected to this pin.

24. **Pulse timing capacitor**

    The timing of the pulse generator is determined by a 220 pF capacitor connected to this pin.

25. **Video composite sync output (VCS)**

    This output signal is for CCT.

26. **Black level**

    The black level for the adaptive sync separator is stored by a 68 nF capacitor connected to this pin.

27. **Composite video input (CVS)**

    The composite video signal is input via a 2,2 μF clamping capacitor to the adaptive sync separator.

28. **Text composite sync input ($\overline{\text{TCS}}$)/Scan composite sync input ($\overline{\text{SCS}}$)**

    $\overline{\text{TCS}}$ is input from CCT or $\overline{\text{SCS}}$ from external sync circuit. $\overline{\text{SCS}}$ is expected when there is no load resistor at pin 1. If pin 28 is not connected the sync output on pin 1 will be the composite video input at pin 27, internally buffered.

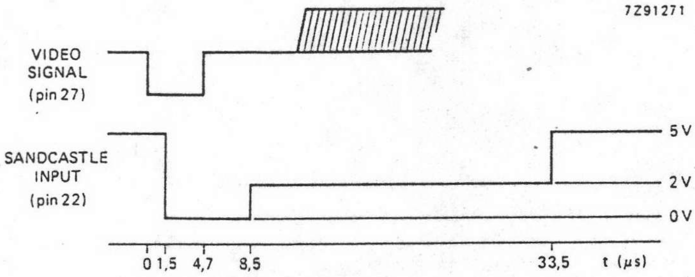


Fig. 4 Sandcastle waveform and timing.

ENHANCED COMPUTER CONTROLLED TELETEXT CIRCUITS
(ECCT)

GENERAL DESCRIPTION

The SAA5243 series are MOS N-channel integrated circuits which perform all the digital logic functions of a 625-line World System Teletext decoder. The SAA5243 series operate in conjunction with the teletext video processor SAA5231, standard static RAMs and are controlled via the 2-wire I^{2}C-bus. The devices can be used to provide videotex display conforming to a serial character attribute protocol.

Features

- Microcomputer controlled for flexibility
- High quality flicker-free display using a 12 x 10 character matrix
- Field flyback (lines 2 to 22), or full channel (all lines) data acquisition
- Up to four simultaneous page requests enabling acquisition during one magazine cycle
- Direct interface up to 8 K bytes static RAM
- Automatic language section of up to seven different languages
- 25th display row for software generated status messages
- Cursor control for videotex/telesoftware
- 7-bits parity or 8-bit data acquisition
- Extension packet reception option
- Standard I^{2}C-bus slave transceiver (slave address 0010001)
- Single 5 volt power supply
- Mask programmable character sets
- Slave sync mode operation
- $\overline{\text{Odd}}$/even field output for de-interlaced displays

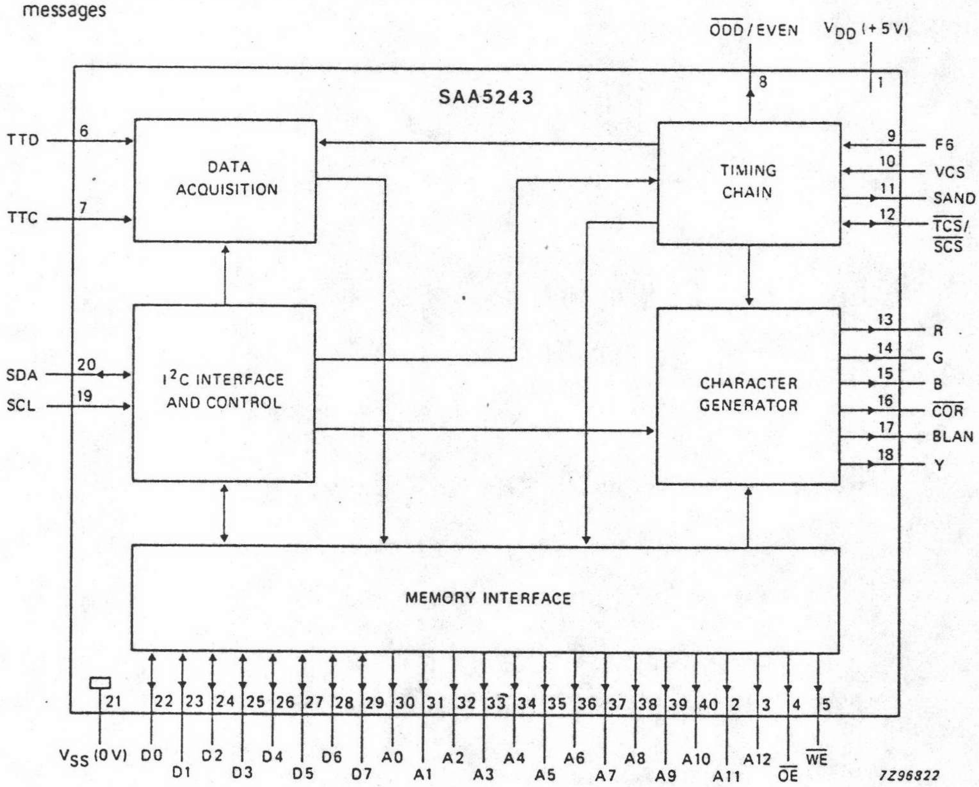


Fig.1 Block diagram.

PACKAGE OUTLINE 40-lead DIL; plastic (SOT129).

ORDERING INFORMATION

type number	version
SAA5243P/E/M2	West European languages
SAA5243P/H	East European languages
SAA5243P/K	Arabic and English languages
SAA5243P/L	Arabic and Hebrew languages

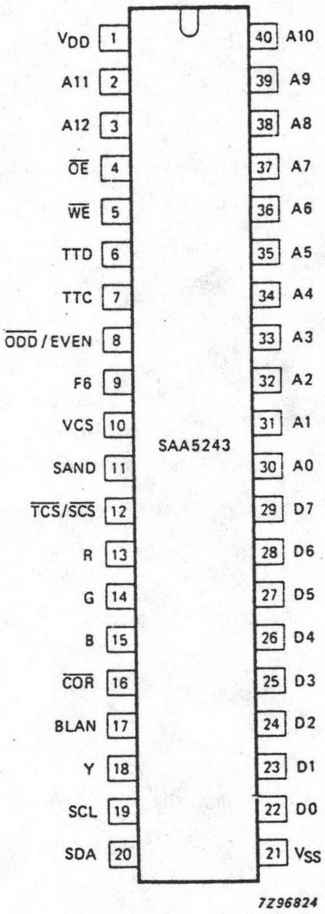


Fig.2 Pinning diagram.

PINNING

1 V_{DD} **Power supply:** + 5 V power supply pin.

2, 3, 40 A11, A12, A10 **Chapter Address:** three outputs that select which 1 K byte chapter of external RAM is being accessed for any read or write cycle.

4 $\overline{OE}$ **Output Enable:** active low output signal used to control the reading of the external RAM. It occurs continuously at a 1 MHz rate.

5	$\overline{\text{WE}}$	**Write Enable:** active low output signal used to control the writing of data to the external RAM. It occurs for a valid write cycle only and is interleaved with the read cycles.
6	TTD	**Teletext Data:** input from the SAA5231 Video Input Processor (VIP2). It is clamped to V_{SS} for 4 to 8 μs of each television line to maintain the correct DC level following the external AC coupling.
7	TTC	**Teletext Clock:** 6.9375 MHz clock input from the SAA5231. It is internally AC coupled to an active clamp input buffer.
8	$\overline{\text{ODD}}$/EVEN	**$\overline{\text{Odd}}$/Even:** for interlaced mode, the output changes once per field at 2 μs before the end of line 311 (624). The output is high for even fields and low for odd fields.
9	F6	**Character display clock:** 6 MHz clock input from the SAA5231. It is internally AC coupled to an active clamp input buffer.
10	VCS	**Video Composite Sync:** input from the SAA5231 derived from the incoming video signal. Sync pulses are active high.
11	SAND	**Sandcastle:** 3-level sandcastle output to the SAA5231 containing the phase locking and colour burst blanking information.
12	$\overline{\text{TCS}}$/$\overline{\text{SCS}}$	**Text Composite Sync/Scan Composite Sync:** as an output an active low composite sync waveform (TCS) with interlaced or non-interlaced format (see Fig.6) which is fed to the SAA5231 to drive the display timebases. Alternatively this pin can act as an input for an active low composite sync waveform (SCS) to 'slave' the display timing circuits.
13, 14, 15	R, G, B	**Red, Green, Blue:** these 3 open drain outputs are the character video signals to the television display circuits. They are active high and contain character and background information.
16	$\overline{\text{COR}}$	**Contrast Reduction:** open drain, active low output which allows selective contrast reduction of the television picture to enhance a mixed mode display.
17	BLAN	**Blanking:** open drain, active high output which controls the blanking of the television picture for a normal text display and for a mixed display.
18	Y	**Character foreground:** open drain, active high video output signal containing all the foreground information displayed on the television screen (e.g. for driving a display printer).
19	SCL	**Serial Clock:** input signal which is the I^2C-bus clock from the microcontroller.
20	SDA	**Serial Data:** is the I^2C-bus data line. It is an input/output function with an open drain output.
21	V_{SS}	**Ground:** 0 volts.
22-29	DO-D7	**8 RAM data lines:** 3-state input/output pins which carry the data bytes to and from the external RAM.
30-39	A0-A9	**RAM address:** 10 output signals that determine which byte location within a 1 K byte chapter of external RAM is accessed for any read or write cycle.

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ข.15

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range	pin 1	V_{DD}	–0.3	7.5	V
Input voltage range					
VCS, SDA, SCL, D0-D7		V_I	–0.3	7.5	V
TTC, TTD, F6, $\overline{TCS}$/$\overline{SCS}$		V_I	–0.3	10.0	V
Output voltage range SAND, A0-A12, $\overline{OE}$, $\overline{WE}$, D0-D7, SDA, $\overline{ODD}$/EVEN, R, G, B, BLAN, $\overline{COR}$, Y		V_O	–0.3	7.5	V
$\overline{TCS}$/$\overline{SCS}$		V_O	–0.3	10.0	V
Storage temperature range		T_{stg}	–20	+ 125	°C
Operating ambient temperature range		T_{amb}	–20	+ 70	°C

CHARACTERISTICS

V_{DD} = 5 V ± 10%; V_{SS} = 0 V; T_{amb} = −20 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
SUPPLY					
Supply voltage (pin 1)	V_{DD}	4.5	5.0	5.5	V
Supply current (pin 1)	I_{DD}	–	160	270	mA
INPUTS (note 1)					
TTD (note 2)					
External coupling capacitor	C_{ext}	–	–	50	nF
Input voltage (peak-to-peak value)	$V_{I(p-p)}$	2.0	–	7.0	V
Input data rise and fall times (note 3)	t_r, t_f	10	–	80	ns
Input data set-up time (note 4)	t_{DS}	40	–	–	ns
Input data hold time (note 4)	t_{DH}	40	–	–	ns
Input leakage current at V_I = 0 to 10 V	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	7	pF
TTC; F6 (note 5)					
DC input voltage range	V_I	−0.3	–	+ 10.0	V
AC input voltage (peak-to-peak value) F6	$V_{I(p-p)}$	1.0	–	7.0	V
AC input voltage (peak-to-peak value) TTC	$V_{I(p-p)}$	1.5	–	7.0	V
Input peaks relative to 50% duty cycle	± V_P	0.2	–	3.5	V
TTC clock frequency	f_{TTC}	–	6.9375	–	MHz
F6 clock frequency	f_{F6}	–	6.0	–	MHz
Clock rise and fall times (note 3)	t_r, t_f	10	–	80	ns
Input leakage current at V_I = 0 to 10 V	I_{LI}	–	–	20	μA
Input capacitance	C_I	–	–	7	pF
VCS					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	V_{DD}	V
Input rise and fall times (note 3)	t_r, t_f	–	–	500	ns
Input leakage current at V_I = 5.5 V	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
SCL					
Input voltage LOW	V_{IL}	0	–	1.5	V
Input voltage HIGH	V_{IH}	3.0	–	V_{DD}	V
SCL clock frequency	f_{SCL}	0	–	100	kHz
Input rise and fall times (note 3)	t_r, t_f	–	–	2	μs
Input leakage current at $V_I = 5.5$ V	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
INPUT/OUTPUTS (note 6)					
$\overline{TCS}$ (output)/$\overline{SCS}$ (input)					
Input voltage LOW	V_{IL}	0	–	1.5	V
Input voltage HIGH	V_{IH}	3.5	–	10.0	V
Input rise and fall times (note 3)	t_r, t_f	–	–	500	ns
Input leakage current at $V_I = 0$ to 10 V and output in high impedance state	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at $I_{OL} = 0.4$ mA	V_{OL}	0	–	0.4	V
Output voltage HIGH					
at $-I_{OH} = 0.2$ mA	V_{OH}	2.4	–	V_{DD}	V
at $I_{OH} = 0.1$ mA	V_{OH}	2.4	–	6.0	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	100	ns
Load capacitance	C_L	–	–	50	pF
SDA (note 7)					
Input voltage LOW	V_{IL}	0	–	1.5	V
Input voltage HIGH	V_{IH}	3.0	–	V_{DD}	V
Input rise and fall times (note 3)	t_r, t_f	–	–	2	μs
Input leakage current at $V_I = 5.5$ V with output off	I_{LI}	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at $I_{OL} = 3$ mA	V_{OL}	0	–	0.5	V
Output fall time between 3.0 V and 1.0 V levels	t_f	–	–	200	ns
Load capacitance	C_L	–	–	400	pF

parameter	symbol	min.	typ.	max.	unit
INPUT/OUTPUTS (continued)					
D0-D7 (note 8)					
Input voltage LOW	V_{IL}	0	–	0.8	V
Input voltage HIGH	V_{IH}	2.0	–	V_{DD}	V
Input leakage current at V_I = 0 V to 5.5 V and output in high impedance state	$\pm I_{LI}$	–	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output voltage LOW at I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	50	ns
Load capacitance	C_L	–	–	120	pF
OUTPUTS (note 6)					
A0-A12; $\overline{OE}$; $\overline{WE}$ (note 8)					
Output voltage LOW at I_{OL} = 1.6 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	50	ns
Load capacitance	C_L	–	–	120	pF
$\overline{ODD}$/EVEN					
Output voltage LOW at I_{OL} = 0.4 mA	V_{OL}	0	–	0.4	V
Output voltage HIGH at $-I_{OH}$ = 0.2 mA	V_{OH}	2.4	–	V_{DD}	V
Output rise and fall times between 0.6 V and 2.2 V levels	t_r, t_f	–	–	100	ns
Load capacitance	C_L	–	–	50	pF
SAND (note 9)					
Output voltage LOW at I_{OL} = 0.2 mA	V_{OL}	0	–	0.25	V
Output voltage INTERMEDIATE at I_{OL} = ± 10 μA	V_{OI}	1.1	–	3.1	V

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
SAND (continued)					
Output voltage HIGH at I_{OH} = 0 to −10 μA	V_{OH}	4.0	–	V_{DD}	V
Output rise time V_{OL} to V_{OI} between 0.4 V and 0.9 V levels	t_{r1}	–	–	400	ns
Output rise time V_{OI} to V_{OH} between 3.3 V and 3.8 V levels	t_{r2}	–	–	200	ns
Output fall time V_{OH} to V_{OL} between 3.8 V and 0.4 V levels	t_f	–	–	50	ns
Load capacitance	C_L	–	–	30	pF
R; G; B; $\overline{COR}$; BLAN; Y (note 10)					
Output voltage LOW at I_{OL} = 2 mA	V_{OL}	0	–	0.4	V
Output voltage LOW at I_{OL} = 5 mA	V_{OL}	0	–	1.0	V
Pull-up voltage as seen at pin	V_{PU}	–	–	6.0	V
Output fall time with a load resistor of 1.2 kΩ to 6 V and measured between 5.5 V and 1.5 V	t_f	–	–	20	ns
Skew delay between outputs with a load resistor of 1.2 kΩ to 6 V and measured on the falling edges at 3.5 V	t_{SK}	–	–	20	ns
Load capacitance	C_L	–	–	25	pF
Output leakage current at V_{PU} = 0 to 6 V with output off	I_{LO}	–	–	10	μA
TIMING					
I^2C-bus (note 11)					
Clock low period	t_{LOW}	4	–	–	μs
Clock high period	t_{HIGH}	4	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	170	–	–	ns
Stop set-up time from clock high	$t_{SU;STO}$	4	–	–	μs
Start set-up time following a stop	t_{BUF}	4	–	–	μs
Start hold time	$t_{HD;STA}$	4	–	–	μs
Start set-up time following clock low-to-high transition	$t_{SU;STA}$	4	–	–	μs

parameter	symbol	min.	typ.	max.	unit
TIMING (continued)					
Memory interface (note 12)					
Cycle time	t_{CY}	–	500	–	ns
Address change to $\overline{OE}$ LOW	t_{OE}	60	–	–	ns
Address active time	t_{ADDR}	450	500	–	ns
$\overline{OE}$ pulse duration	t_{OEW}	320	–	–	ns
Access time from $\overline{OE}$ to data valid	t_{ACC}	–	–	200	ns
Data hold time from $\overline{OE}$ HIGH or address change	t_{DH}	0	–	–	ns
Address change to $\overline{WE}$ LOW	t_{WE}	40	–	–	ns
$\overline{WE}$ pulse duration	t_{WEW}	200	–	–	ns
Data set-up time to $\overline{WE}$ HIGH	t_{DS}	100	–	–	ns
Data hold time from $\overline{WE}$ HIGH	t_{DHWE}	20	–	–	ns
Write recovery time	t_{WR}	25	–	–	ns

Notes to the characteristics

1. All inputs are protected against static charge under normal handling.
2. The TTD input incorporates an internal clamping diode in addition to the active clamping transistor (see Fig.3).
3. Rise and fall times between 10% and 90% levels.
4. Teletext input data set-up and hold times are with respect to a 50% duty cycle level of the rising edge of the teletext clock input (TTC). Data stable 1 $\geqslant$ 2.0 V; data stable 0 $\leqslant$ 0.8 V (see Fig.4).
5. The TTC and F6 inputs have internal clamping diodes and are AC coupled (see Fig.3).
6. All outputs and input/outputs are protected against static charge under normal handling and connection to V_{DD} and V_{SS}.
7. For details of I^{2}C-bus timing see Fig.8.
8. For details of RAM timing see Fig.9.
9. For details of synchronization timing see Fig.5.
10. For details of display output timing see Fig.7.
11. The I^{2}C-bus timings are referred to V_{IH} = 3 V and V_{IL} = 1.5 V. For waveforms see Fig.8.
12. The memory interface timings are referred to V_{IL} = 1.5 V. For waveforms see Fig.9.

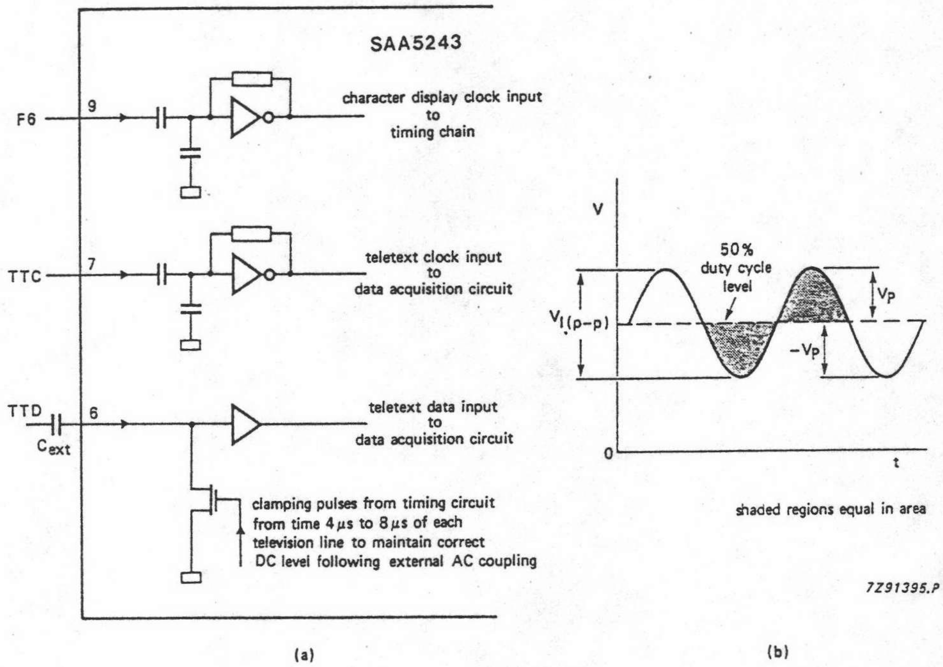
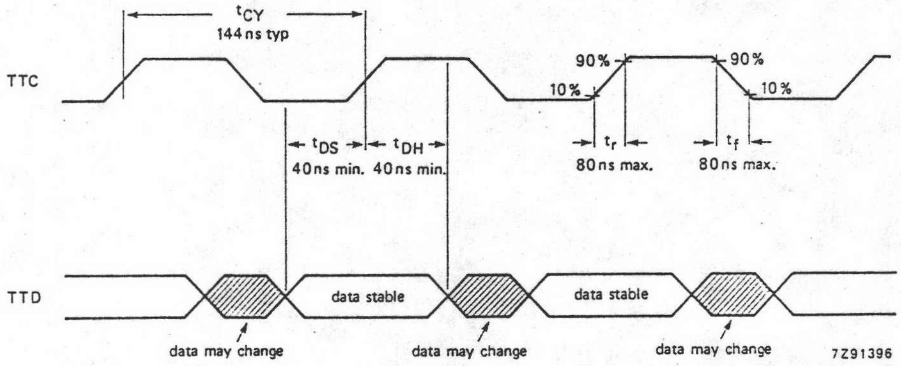

SAA5243
F6
9
character display clock input
to
timing chain
TTC
7
teletext clock input
to
data acquisition circuit
TTD
6
C_{ext}
teletext data input
to
data acquisition circuit
clamping pulses from timing circuit
from time 4 μs to 8 μs of each
television line to maintain correct
DC level following external AC coupling
V
50%
duty cycle
level
$V_{I(p-p)}$
V_P
$-V_P$
0
t
shaded regions equal in area
7Z91395.P
(a)
(b)

Fig.3 (a) F6, TTC and TTD input circuitry (b) input waveform parameters.



Data stable: 1 is ⩾ 2.0 V; 0 is ⩽ 0.8 V.

Fig.4 Teletext data input timing.

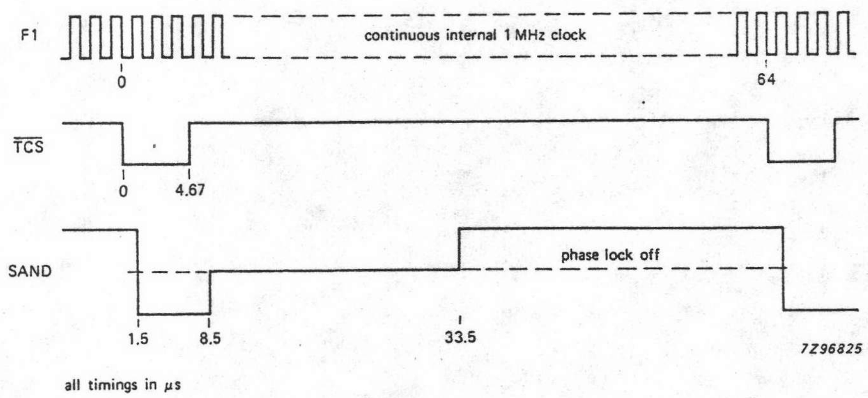
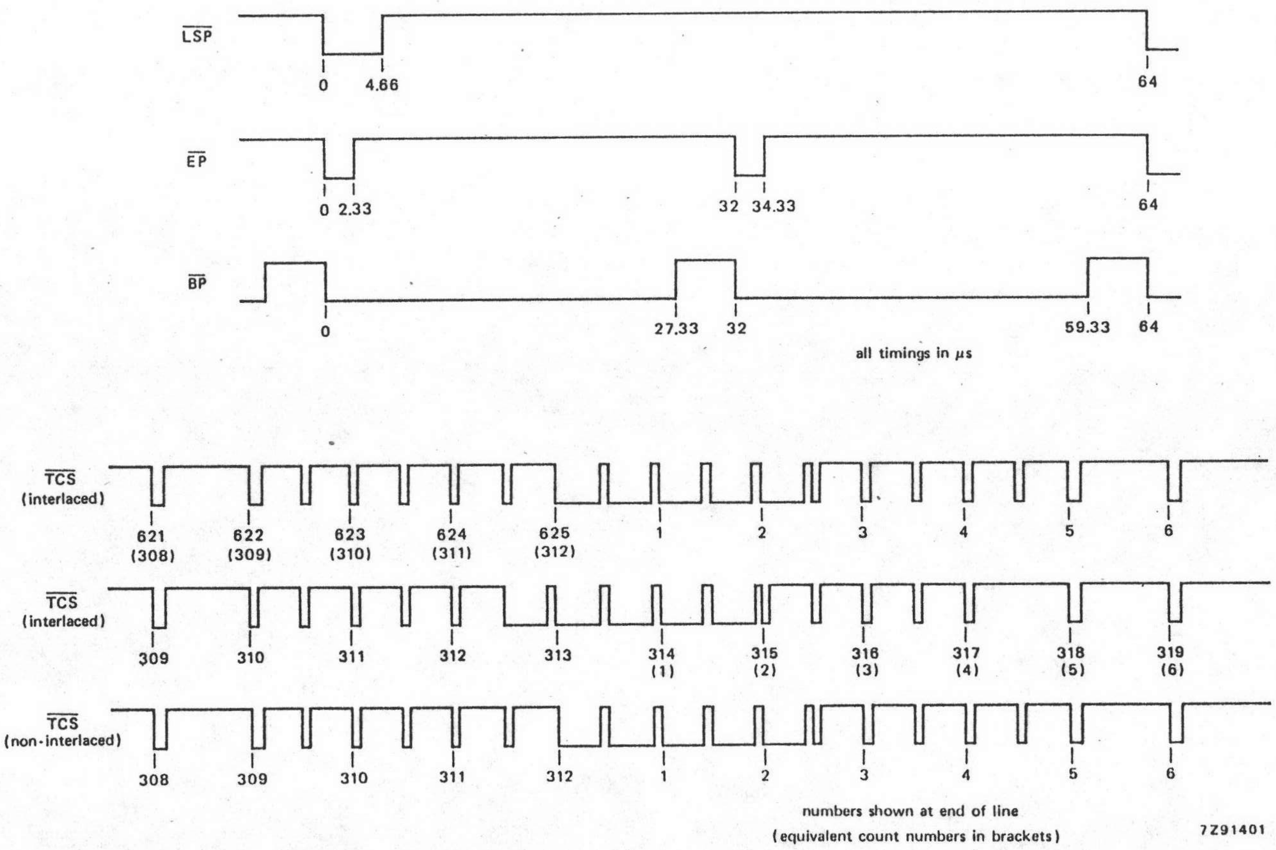


Fig.5 Synchronization timing.



Line sync pulses ($\overline{LSP}$), equalizing pulses ($\overline{EP}$) and broad pulses ($\overline{BP}$) are combined to provide the text composite sync waveform ($\overline{TCS}$) as shown. All timings measured from falling edge of $\overline{LSP}$ with a tolerance of ± 100 ns.

Fig.6 Composite sync waveforms.

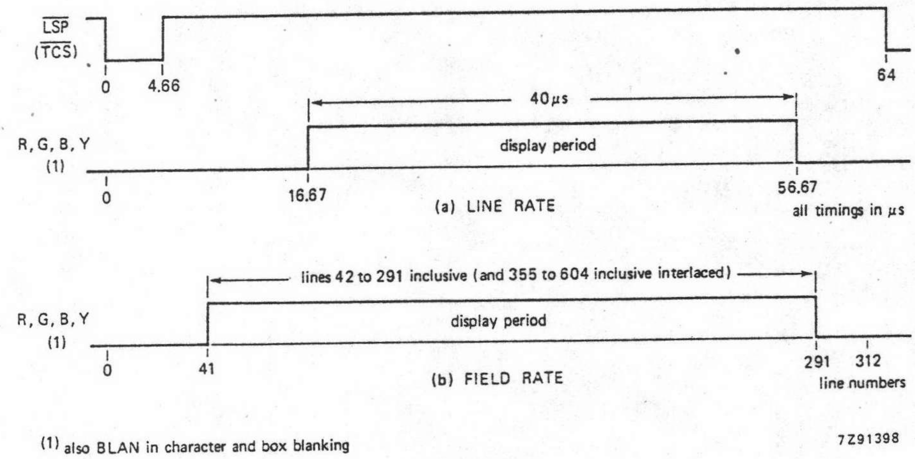


Fig.7 Display output timing (a) line rate (b) field rate.

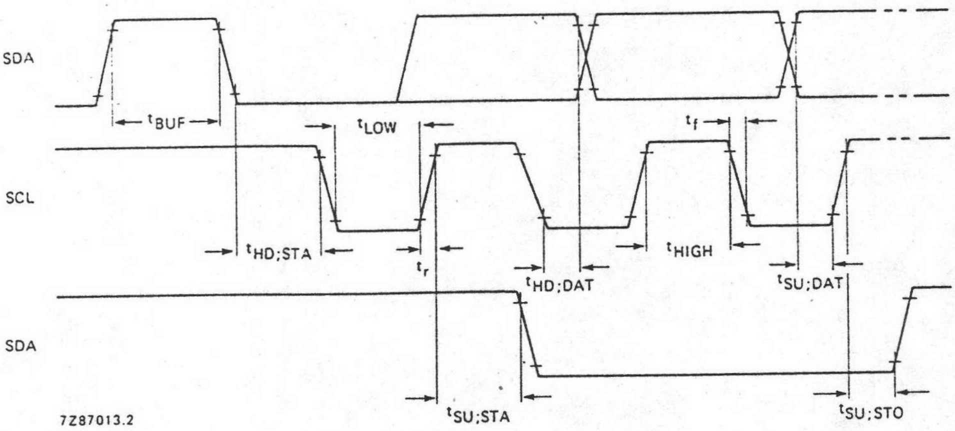


Fig.8 I^{2}C-bus timing.

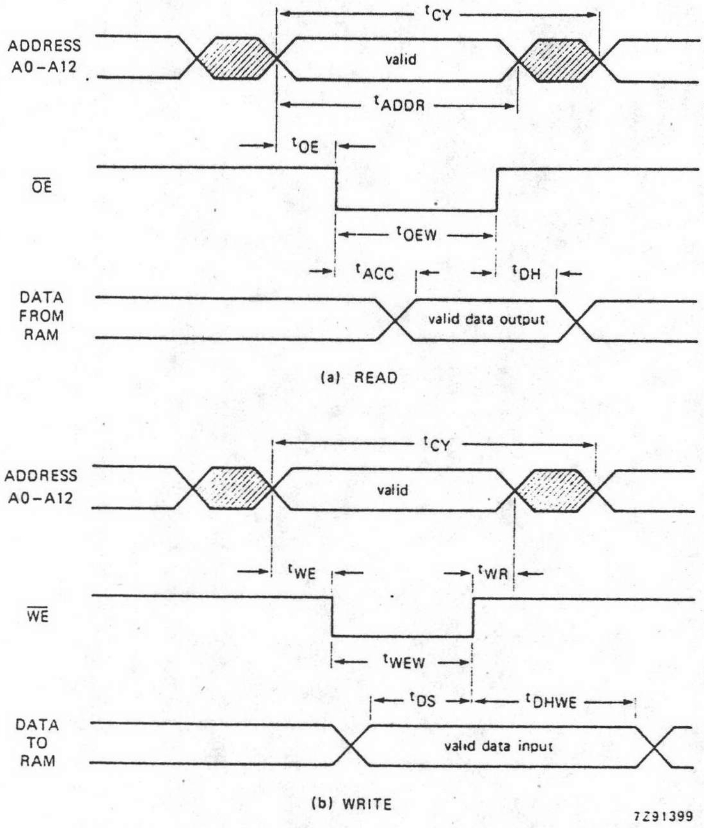


Fig.9 Memory interface timing (a) read (b) write.

125
v.26

APPLICATION INFORMATION

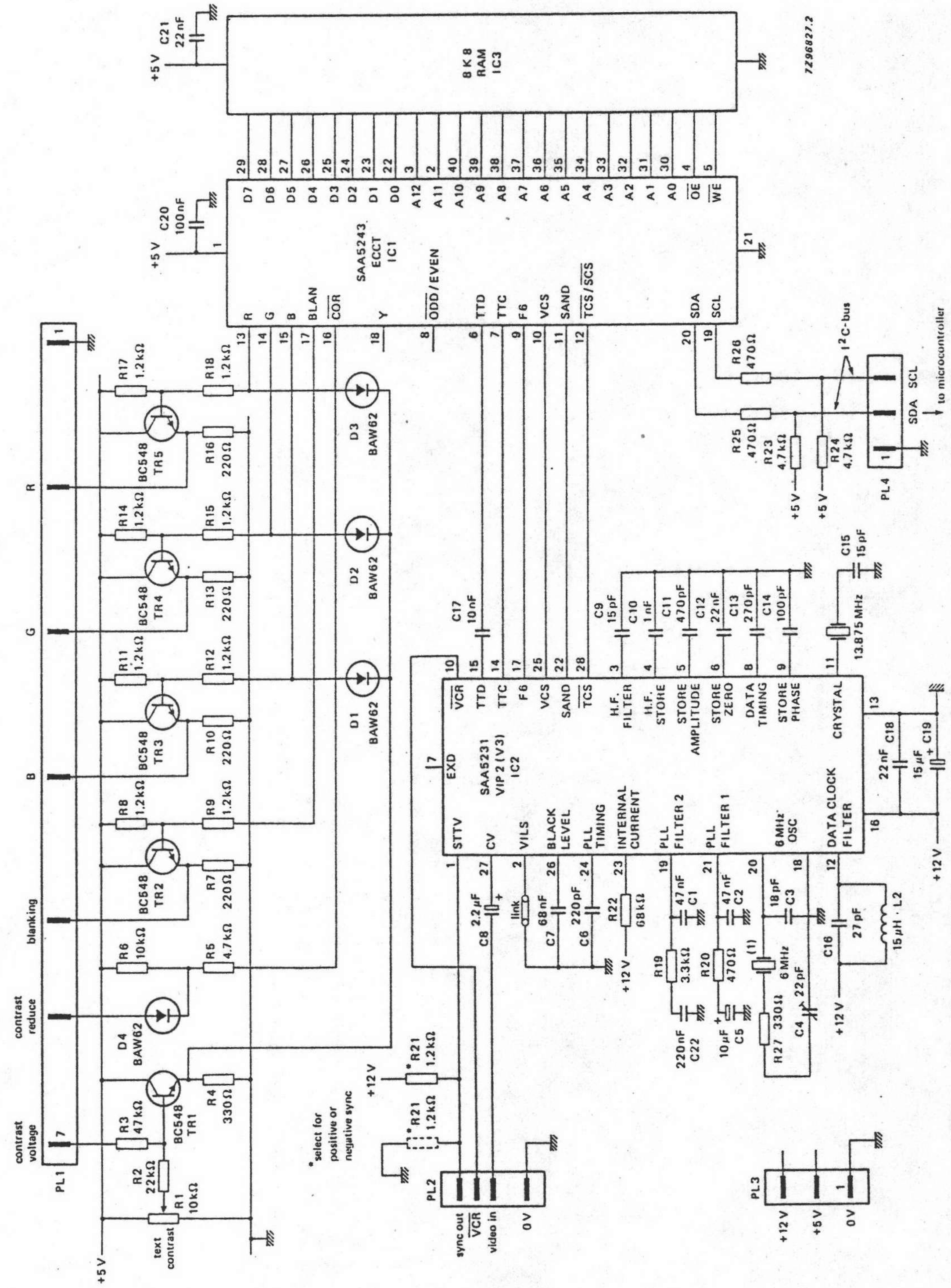


Fig. 10 ECCT based multi-page decoder circuit diagram.

(1) Ceramic resonator e.g. Kyocera KBR 6.0 M.

APPLICATION INFORMATION (continued)

ECCT page memory organization

The organization of a page memory is shown in Fig.11. The ECCT provides an additional row compared with first generation decoders bringing the display format up to 40 characters by 25 rows. Rows 0 to 23 form the teletext page as broadcast and row 24 is the extra row available for user-generated status messages.

A MORE DETAILED DESCRIPTION OF ECCT OPERATION AND APPLICATION IS AVAILABLE ON REQUEST.

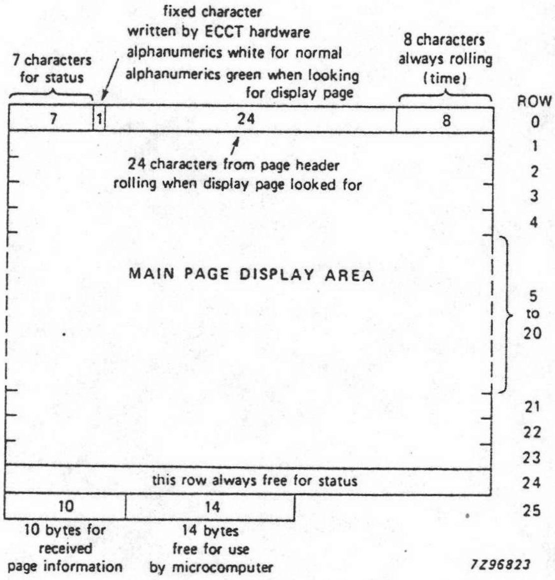


Fig.11 Page memory organization.

Table 1 Row 25 received control data format

D0	PU0	PT0	MU0	MT0	HU0	HT0	C7	C11	MAG0	0
D1	PU1	PT1	MU1	MT1	HU1	HT1	C8	C12	MAG1	0
D2	PU2	PT2	MU2	MT2	HU2	C5	C9	C13	MAG2	0
D3	PU3	PT3	MU3	C4	HU3	C6	C10	C14	0	0
D4	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	HAM.ER	$\overline{\text{FOUND}}$	0
D5	0	0	0	0	0	0	0	0	0	PBLF
D6	0	0	0	0	0	0	0	0	0	0
D7	0	0	0.	0	0	0	0	0	0	0
Column	0	1	2	3	4	5	6	7	8	9

Where:

MAG	magazine	page number	MU	minutes units	page sub-code
PU	page units		MT	minutes tens	
PT	page tens		HU	hours units	
$\overline{\text{PBLF}}$	page being looked for		HT	hours tens	
$\overline{\text{FOUND}}$	LOW for page has been found		C4-C14	transmitted control bits	
HAM.ER	Hamming error in corresponding byte				

Row 0

Row 0 is for the page header. The first seven columns (0 to 6) are free for status messages. The eighth is an alphanumeric white or green control character, written automatically by ECCT to give a green rolling header when a page is being looked for. The last eight characters are for rolling time.

Row 25

The first 10 bytes of row 25 contain control data relating to the received page. Seven digits are used to identify a page as shown in Table 1. The remaining 14 bytes are free for use by the microcomputer.

Register maps

ECCT mode registers R1 to R11 are shown in Table 2. R1 to R10 are WRITE only; R11 is READ/WRITE.
Register map (R3), for page requests, is shown in detail in Table 3.

Table 2 ECCT register map

D7	D6	D5	D4	D3	D2	D1	D0		
TA	$\overline{\text{7+P}}$/ 8 BIT	ACQ. $\overline{\text{ON}}$/OFF	EXTENSION PACKET ENABLE	$\overline{\text{DEW}}$/ FULL FIELD	TCS ON	T1	T0	R1	Mode
—	BANK SELECT A2	ACQ. CCT A1	ACQ. CCT A0	TB	START COLUMN SC2	START COLUMN SC1	START COLUMN SC0	R2	Page request address
—	—	—	PRD4	PRD3	PRD2	PRD1	PRD0	R3	Page request data
—	—	—	—	—	A2	A1	A0	R4	Display chapter
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R5	Display control (normal)
BKGND OUT	BKGND IN	COR OUT	COR IN	TEXT OUT	TEXT IN	PON OUT	PON IN	R6	Display control (newsflash/subtitle)
STATUS ROW $\overline{\text{BTM}}$/TOP	CURSOR ON	$\overline{\text{CONCEAL}}$/ REVEAL	$\overline{\text{TOP}}$/ BOTTOM	$\overline{\text{SINGLE}}$/ DOUBLE HEIGHT	BOX ON 24	BOX ON 1-23	BOX ON 0	R7	Display mode
—	—	—	—	CLEAR MEM.	A2	A1	A0	R8	Active chapter
—	—	—	R4	R3	R2	R1	R0	R9	Active row
—	—	C5	C4	C3	C2	C1	C0	R10	Active column
D7 (R/W)	D6 (R/W)	D5 (R/W)	D4 (R/W)	D3 (R/W)	D2 (R/W)	D1 (R/W)	D0 (R/W)	R11	Active data

— bit does not exist

Notes to Table 2

The arrows shown on the right of the register map indicate that the register auto-increments to the next one on the following I^{2}C transmission byte. TA and TB must be logic 0 for normal operation.
All bits in registers R1 to R10 are cleared to logic 0 on power-up except bits D0 and D1 of registers R5 and R6 which are set to logic 1.
All memory is cleared to 'space' (00100000) on power-up, except row 0 column 7 chapter 0, which is 'alpha white' (00000111) as the acquisition circuit is enabled but all pages are on hold.

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APPLICATION INFORMATION (continued)

CHARACTER SETS

Several versions of the ECCT are available, offering a variety of character sets. The full character sets are shown in Tables 4a to 4d.

The world system teletext specification allows the selection of national character sets via the page header transmission bits, C12 to C14. These bits are automatically decoded by the ECCT, the resulting character sets are shown in Tables 6a to 6d. For certain languages, control software processing of the extension packet data may be required for optimum useage of the range of available characters. See Fig. 12 for alphanumeric and graphic options.

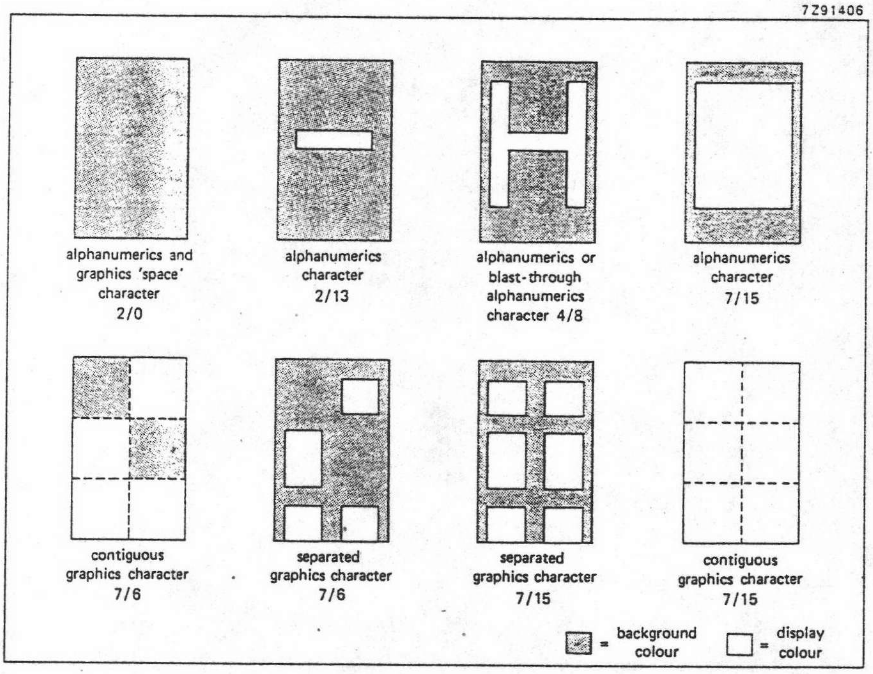
7Z91406
alphanumerics and graphics 'space' character 2/0
alphanumerics character 2/13
alphanumerics or blast-through alphanumerics character 4/8
alphanumerics character 7/15
contiguous graphics character 7/6
separated graphics character 7/6
separated graphics character 7/15
contiguous graphics character 7/15
▨ = background colour
□ = display colour

Fig.12 Alphanumeric and graphic options.

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v.30

Table 4a Character data input decoding, West European languages (SAA5243P/E/M2)

BITS																			
b8 →		0	0	0 or 1	0	0 or 1	0	0	0	0		0		1	1	1	1	1	1
b7 →		0	0	0	0	0	0	1	1	1		1		0	0	1	1	1	1
b6 →		0	0	1	1	1	1	0	0	1		1		0	0	0	0	1	1
b5 →		0	1	0	0	1	1	0	1	0		1		0	1	0	1	0	1
b4 b3 b2 b1	row \ column	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	0	alpha-numerics black	graphics black			0	🬏	§	P	°	🬞	p	🬭	@	É	é	à	i	Á
0 0 0 1	1	alpha-numerics red	graphics red	!	🬀	1	🬐	A	Q	a	🬟	q	🬮	―	é	ù	è	¿	À
0 0 1 0	2	alpha-numerics green	graphics green	"	🬁	2	🬑	B	R	b	🬠	r	🬯	¼	ä	à	â	ü	È
0 0 1 1	3	alpha-numerics yellow	graphics yellow	#	🬂	3	🬒	C	S	c	🬡	s	🬰	£	#	£	é	ç	Î
0 1 0 0	4	alpha-numerics blue	graphics blue	$	🬃	4	🬓	D	T	d	🬢	t	🬱	$	¤	$	ï	$	Ï
0 1 0 1	5	alpha-numerics magenta	graphics magenta	%	🬄	5	▌	E	U	e	🬣	u	🬲	[illegible]	[illegible]	ã	Ã	ª	Ó
0 1 1 0	6	alpha-numerics cyan	graphics cyan	&	🬅	6	🬔	F	V	f	🬤	v	🬳	[illegible]	[illegible]	õ	Õ	º	Ò
0 1 1 1	7	alpha-** numerics white	graphics white	'	🬆	7	🬕	G	W	g	🬥	w	🬴	(?)	(÷)	·	Ç	Ñ	Ú
1 0 0 0	8	flash	conceal display	(	🬇	8	🬖	H	X	h	🬦	x	🬵	‖	ö	ò	ô	ñ	æ
1 0 0 1	9	steady **	contiguous graphics **	)	🬈	9	🬗	I	Y	i	🬧	y	🬶	¾	å	è	û	è	Æ
1 0 1 0	10	end box **	separated graphics	*	🬉	:	🬘	J	Z	j	▐	z	🬷	÷	ü	ì	ç	à	ð
1 0 1 1	11	start box	ESC *	+	🬊	;	🬙	K	Ä	k	🬨	ä	🬸	←	Ä	°	ë	á	Đ
1 1 0 0	12	normal ** height	black ** back-ground	,	🬋	<	🬚	L	Ö	l	🬩	ö	🬹	½	Ö	ç	ê	é	ø
1 1 0 1	13	double height	new back-ground	-	🬌	=	🬛	M	Ü	m	🬪	ü	🬺	→	Å	→	ù	í	Ø
1 1 1 0	14	SO *	hold graphics	.	🬍	>	🬜	N	^	n	🬫	ß	🬻	↑	Ü	↑	î	ó	þ
1 1 1 1	15	SI *	release ** graphics	/	🬎	?	🬝	O	_	o	🬬	■	█	#	_	#	#	ú	Þ

7Z96828.4

* These control characters are reserved for compatibility with other data codes

** These control characters are presumed before each row begins

APPLICATION INFORMATION (continued)

Table 4d Character data input decoding, Arabic and Hebrew languages (SAA5243P/L)

B I T S b8 →		0	0	0 or 1	0	0 or 1	0	0	0	0	0 or 1	0	0 or 1	1	1	1	1	1	1
b7 →		0	0	0	0	0	0	1	1	1	1	1	1	0	0	1	1	1	1
b6 →		0	0	1	1	1	1	0	0	1	1	1	1	0	0	0	0	1	1
b5 →		0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	1	0	1
b4 b3 b2 b1 ↓ ↓ ↓ ↓	row \ column	0	1	2	2a	3	3a	4	5	6	6a	7	7a	8	9	12	13	14	15
0 0 0 0	0	alpha-numerics black	graphics black			0	🬏	@	P	א	🬞	נ	🬭	ﺔ	٠	ة	ﺬ	ـ	ﻰ
0 0 0 1	1	alpha-numerics red	graphics red	!	🬀	1	🬐	A	Q	ב	🬟	ס	🬮	ء	١	ﺄ	ر	ﻓ	ﻌ
0 0 1 0	2	alpha-numerics green	graphics green	"	🬁	2	🬑	B	R	ג	🬠	ע	🬯	آ	٢	ﺒ	ز	ﻗ	ﻐ
0 0 1 1	3	alpha-numerics yellow	graphics yellow	£	🬂	3	🬒	C	S	ד	🬡	ף	🬰	أ	٣	ب	س	ﻛ	ﻔ
0 1 0 0	4	alpha-numerics blue	graphics blue	$	🬃	4	🬓	D	T	ה	🬢	פ	🬱	ؤ	٤	ﺜ	ش	ﻟ	ﻒ
0 1 0 1	5	alpha-numerics magenta	graphics magenta	%	🬄	5	▌	E	U	ו	🬣	ץ	🬲	إ	٥	ت	ص	ﻣ	ﻘ
0 1 1 0	6	alpha-numerics cyan	graphics cyan	&	🬅	6	🬔	F	V	ז	🬤	צ	🬳	ﺊ	٦	ﺎ	ض	ﻧ	ق
0 1 1 1	7	alpha-numerics white **	graphics white	'	🬆	7	🬕	G	W	ח	🬥	ק	🬴	ئ	٧	ا	ط	ﻫ	ك
1 0 0 0	8	flash	conceal display	(	🬇	8	🬖	H	X	ט	🬦	ר	🬵	)	٨	ﺑ	ظ	و	ﻠ
1 0 0 1	9	steady **	contiguous graphics **	)	🬈	9	🬗	I	Y	י	🬧	ש	🬶	(	٩	ة	ع	ى	ل
1 0 1 0	10	end box **	separated graphics	*	🬉	:	🬘	J	Z	ך	▐	ת	🬷	،	ﻌ	ﺗ	ﻋ	ﻳ	ﻤ
1 0 1 1	11	start box	TWIST	+	🬊	;	🬙	K	←	כ	🬨	₪	🬸	؛	ﻊ	ﺛ	ﺸ	ﺚ	م
1 1 0 0	12	normal height **	black back-ground **	,	🬋	<	🬚	L	½	ל	🬩	‖	🬹	>	ﻐ	ﺟ	ﺠ	ج	ﻨ
1 1 0 1	13	double height	new back-ground	-	🬌	=	🬛	M	→	ם	🬪	¾	🬺	ﺋ	ﻬ	ﺣ	ﺤ	ح	ن
1 1 1 0	14	SO *	hold graphics	.	🬍	>	🬜	N	↑	מ	🬫	÷	🬻	<	ﻪ	ﺧ	ﺨ	خ	لا
1 1 1 1	15	SI *	release graphics **	/	🬎	?	🬝	O	#	ן	🬬	■	█	؟	ه	ﺪ	#	ﻴ	■

7Z22679.3

* These control characters are reserved for compatibility with other data codes

** These control characters are presumed before each row begins

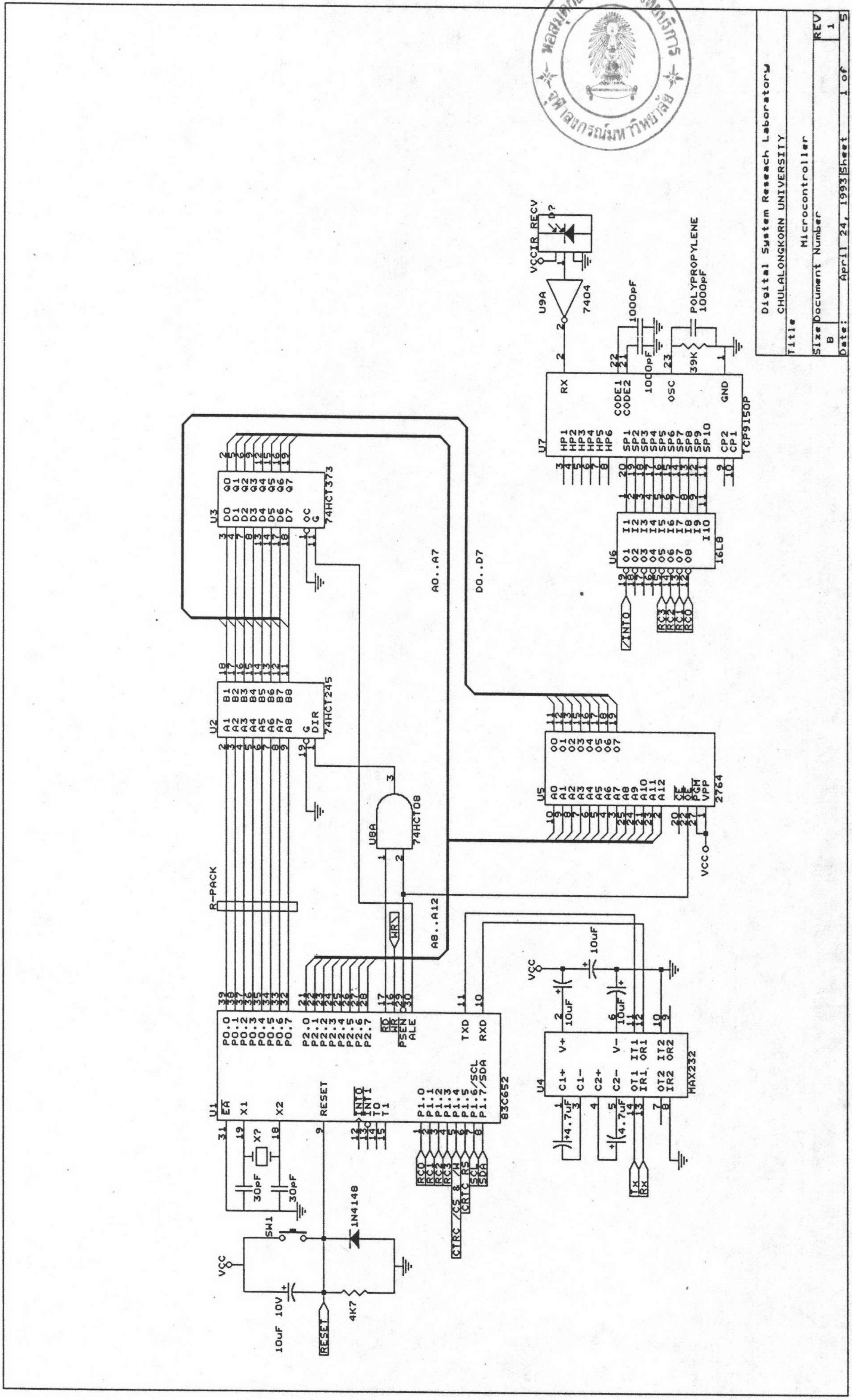
Notes to Table 4

1. Control characters shown in columns 0 and 1 are normally displayed as spaces.
2. Codes may be referred to by column and row. For example 2/5 refers to %.
3. Black represents displayed colour. White represents background.
4. Character rectangle shown as follows: □
5. National option characters are shown in Table 6.
6. Characters 8/6, 8/7, 9/5, 9/6 and 9/7 are special characters (for /E and /H character tables only) to combine with character 8/5.
7. With bit 8 = 0 national option character will be decoded according to the setting of control bits C12 to C14 (see Table 6).

Purchase of Philips' I^{2}C components conveys a license under the Philips' I^{2}C patent to use the components in the I^{2}C-system provided the system conforms to the I^{2}C specifications defined by Philips.

ภาคผนวก ค.
วงจรต้นแบบเครื่องถอดรหัสสัญญาณเทเลเท็กซต์

ค.1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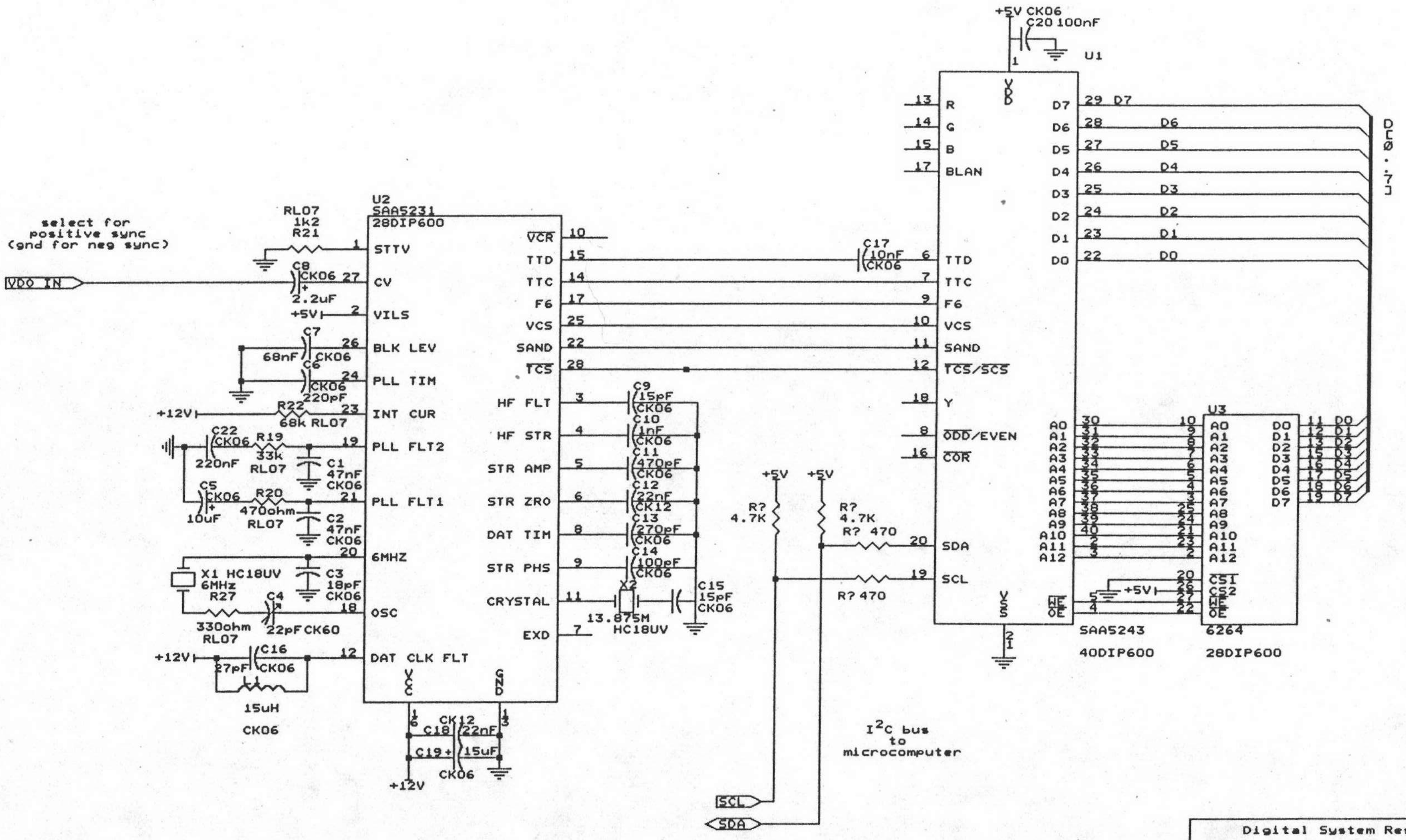
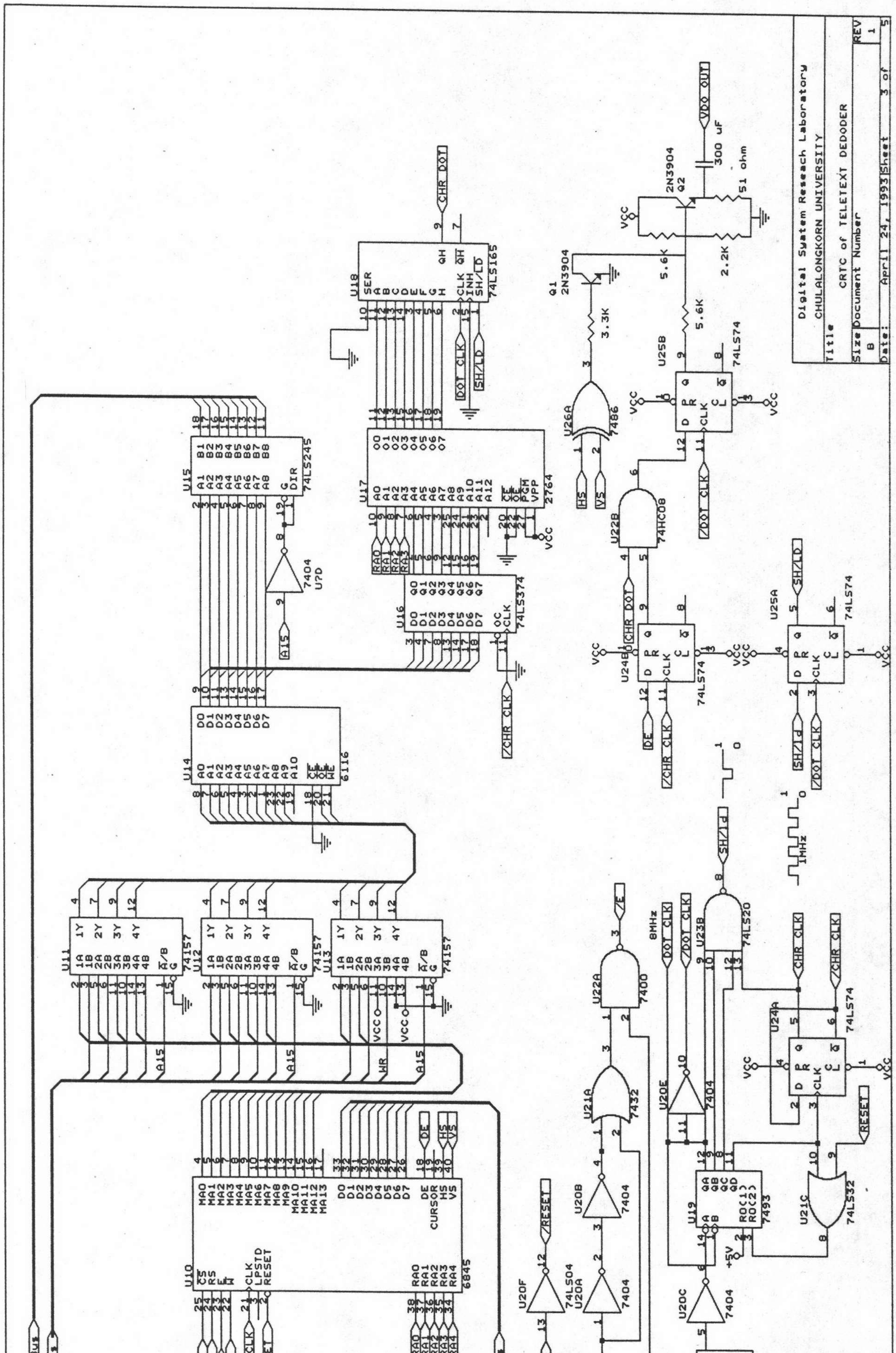
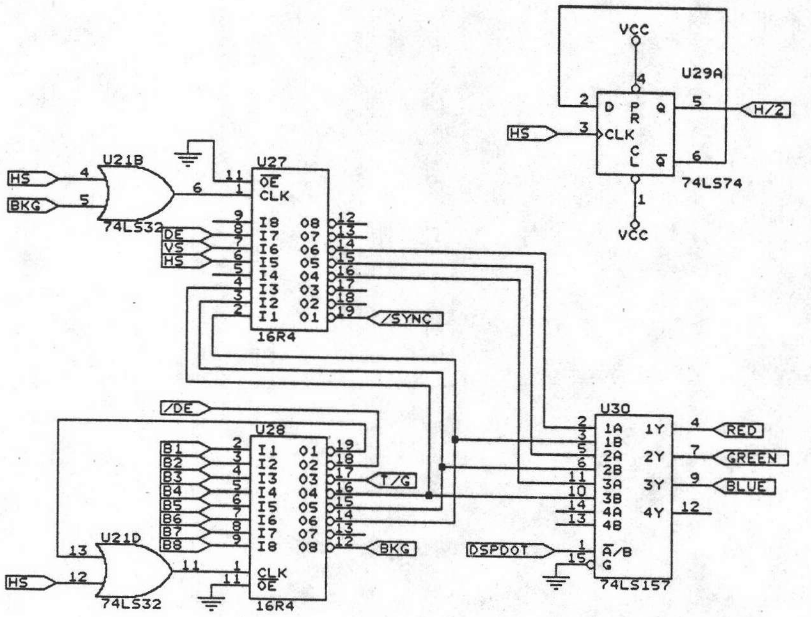
CHULALONGKORN UNIVERSITY
Title
Microcontroller
Size
B
Document Number
REV
1
Date: April 24, 1993
Sheet 1 of 5
U1
83C652
U2
74HCT245
U3
74HCT373
U4
MAX232
U5
2764
U6
16L8
U7
TCP9150P
U8A
74HCT08
U9A
7404
VCCIR RECV
D?
POLYPROPYLENE 1000pF
1000pF
39K
R-PACK
A0..A7
D0..D7
A8..A12
WR
VCC
SW1
1N4148
4K7
10uF 10V
RESET
X?
30pF
10uF
4.7uF
Tx
Rx
INT0
RC0
RC1
RC2
RC3
RC4
CTRC /CS & RS
SCL
SDA

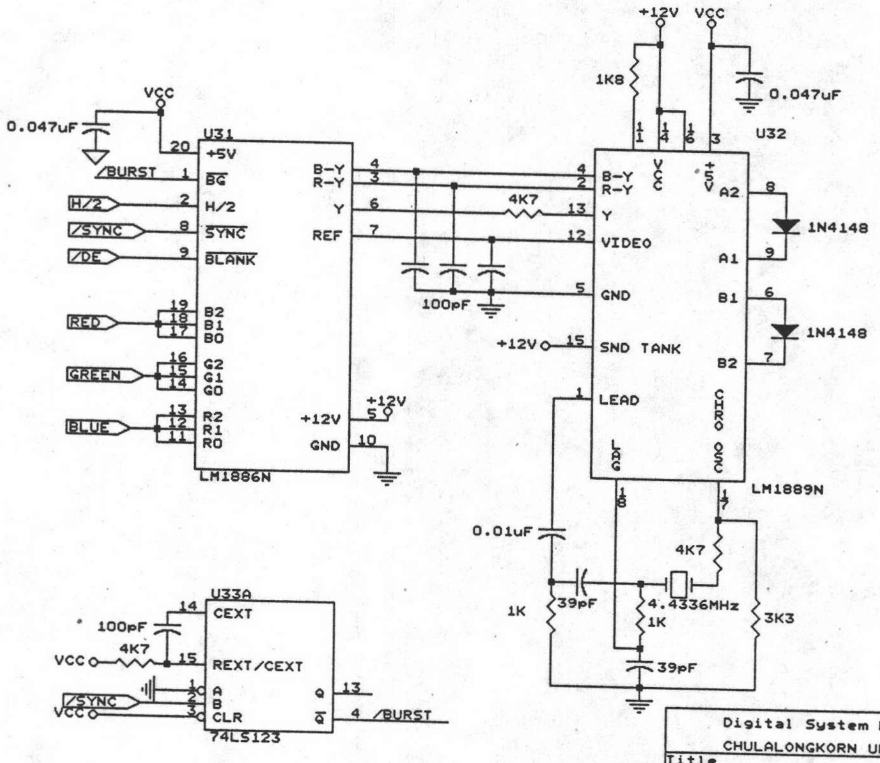


Digital System Reseach Laboratory		
CHULALONGKORN UNIVERSITY		
Title		
VIP & ECCT		
Size	Document Number	REV
B		1
Date: April 24, 1993	Sheet 2 of 5	


Digital System Reseach Laboratory
CHULALONGKORN UNIVERSITY
Title CRTC of TELETEXT DEDODER
Size B
Document Number
REV 1
Date: April 24, 1993
Sheet 3 of 5
U10 6845
CS RS E R/W CLK LPSTD RESET
MA0 MA1 MA2 MA3 MA4 MA5 MA6 MA7 MA8 MA9 MA10 MA11 MA12 MA13
D0 D1 D2 D3 D4 D5 D6 D7
DE CURSOR HS VS
RA0 RA1 RA2 RA3 RA4
P1.4 P1.5 /E P1.4
CHR CLK
/RESET
D Bus
A Bus
U11 74157
U12 74157
U13 74157
1A 1B 2A 2B 3A 3B 4A 4B A/B G 1Y 2Y 3Y 4Y
A15
WR
VCC
U14 6116
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 CE OE WE
U15 74LS245
B1 B2 B3 B4 B5 B6 B7 B8 G DIR
U7D 7404
U16 74LS374
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 OC CLK
/CHR CLK
U17 2764
O0 O1 O2 O3 O4 O5 O6 O7 A11 A12 PGM VPP
U18 74LS165
SER A B C D E F G H CLK INH SH/LD QH
CHR DOT
DOT CLK
SH/LD
Q1 2N3904
Q2 2N3904
3.3K
5.6K
5.6K
2.2K
51 ohm
300 uF
VDO OUT
U26A 7486
HS VS
U25B 74LS74
U22B 74HC08
U24B 74LS74
U25A 74LS74
D PR CLK CL Q
DE
SH/ld
/DOT CLK
1MHz
8MHz
U22A 7400
/E
U21A 7432
U20B 7404
U20A 7404
U20F 74LS04
RESET
/RESET
/RD
/WR
U23B 74LS20
U24A 74LS74
U20E 7404
U19 7493
A B RO(1) RO(2) QA QB QC QD
U21C 74LS32
U20C 7404
+5V
16 MHz OSC



Digital System Reseach Laboratory
CHULALONGKORN UNIVERSITY
Title
Color Decoder
Size A
Document Number
REV 1
Date: April 24, 1993 Sheet 4 of 5



Digital System Reseach Laboratory
CHULALONGKORN UNIVERSITY
Title
COLOR MATRIX DAC
Size A
Document Number
REV 1
Date: April 24, 1993 Sheet 5 of 5

ภาคผนวก ง.

โปรแกรมควบคุม

```
$PW 120

$TL

;%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

;%  SIO1 EQUATE LIST                                %

;%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

;************************************************************

; LOCATION OF THE SIO1 SPECIAL FUNCTION REGISTERS.

;************************************************************

        DEFSEG S1SFR,START=0DBH,CLASS=IDATA,ABSOLUTE

        SEG    S1SFR

        S1CON   EQU 0D8H

        S1STA   EQU 0D9H

        S1DAT   EQU 0DAH

        S1ADR   EQU 0DBH

        UP1A    EQU 04000H

        UP1B    EQU 04001H

        UP1C    EQU 04002H

        UP1CON  EQU 04003H

;************************************************************

; BIT LOCATION

;************************************************************

        SEG BIT

        STA     EQU 0DDH        ;STA BIT IN S1CON

        STO     EQU 0DCH        ;STO BIT IN S1CON

        SI    EQU 0DBH        ;SERIAL 1 INT.

        SIO1HP  EQU 0BDH        ;IPO,SIO1 PRIORITY BIT

;************************************************************

; LOCATION IN DATA RAM

;************************************************************
```

```
SEG DATA

MTD      EQU 030H          ;MST/TRX/DATA base address

MRD      EQU 05AH          ;MST/REC/DATA base address

THA      EQU 048H          ;THAI CODE

THAPAGE EQU 049H           ;THAI PAGE SIGNATURE

HADD     EQU 050H          ;HIGH address byte for STATE 0

                           ;till STATE 25

SLA      EQU 051H          ;Contains SLA+R/W to be transmitted.

NOTMST  EQU 052H           ;number of byte to transmit

                           ;or receive as MST

BACKUP  EQU 053H           ;Backup from NUMBYTMST

                           ;to restore NUMBYTMST in case

                            ;of arbitration Lost.

PAG_MAG EQU 054H           ;PAGE SELECT MAGAZINE  ADDRESS

PAG_TEN EQU 055H            ;PAGE SELECT PAGE TEN  ADDRESS

PAG_UNI EQU 056H            ;PAGE SELECT PAGE UNIT ADDRESS

WRT_MAG EQU 057H             ;USER WRITE MAG

WRT_TEN EQU 058H             ;USER WRITE TEN

WRT_UNI EQU 059H              ;USER WRITE UNIT

GCODE   EQU 05BH              ;GRAPHIC CODE SIGN

;************************************************************

; IMMEDIATE DATA TO WRITE INTO REGISTER S1CON (high speed)

;************************************************************

ENS1_NOTSTA_STO_NOTSI_AA_CRO        EQU 0D5h       ;GEN STOP(CR0=100Khz)

ENS1_STA_NOTSTO_NOTSI_AA_CRO        EQU 0E5h        ;Releases BUS and

                                                    ;set STA

ENS1_NOTSTA_NOTSTO_NOTSI_AA_CRO      EQU 0C5h      ;Releas BUS AND ACK

ENS1_NOTSTA_NOTSTO_NOTSI_NOTAA_CRO  EQU 0C1h ;Releas BUS AND

                                                   ;not ACK
```

```
;**********************************************************
; GENERAL IMMEDIATE DATA
;**********************************************************
          OWNSLA  EQU 031H        ;Own SLA+General Call
                                  ;must be written into S1ADR
          ENSIO1  EQU 0A0H        ;EA+ES1, enable SIO1 interrupt
                                  ;must be written into IENO
          PAG1    EQU 001H        ;Sele PAG1 as HADD
          SLAW    EQU 022H        ;SLA+W to be transmitted
          SLAR    EQU 023H        ;SLA+R to be transmitted
          SELRB2  EQU 010H        ;Select Register Blank 2
          SELRB3  EQU 018H        ;Select Register Blank 3

;==================================
; MACRO DEF SECTION
;==================================
PAG_REQ         %MACRO PH,PT,PU
                MOV R1,#MTD           ;SET POINTER TO MTD
                MOV @R1,#02H          ;ECCT SUB ADD OF R2
                INC R1
                MOV @R1,#10H          ;SET PAGE REQ ADD REG
                INC R1            ;AUTO INC TO R3
                MOV A,PH
                ADD A,#18H
                MOV @R1,A            ;HOLD,MAG2,MAG1,MAG0
                INC R1            ;AUTO INC TO NEXT COL R3
                MOV A,PT
                ADD A,#30H
                MOV @R1,A            ;PAGE TEN
```

```
             INC R1              ;AUTO INC TO NEXT COL R3
             MOV A,PU
             ADD A,#30H
             MOV @R1,A            ;PAGE UNIT
             MOV NOTMST,#05H        ;Transmitt 5 byte
             MOV SLA,#SLAw         ;SLA+W Transmitt funct.
             SETB STA             ;SET STA IN S1CON
            %ENDM


READ_PAGE:   %MACRO
             %GENSYM READIIC,READMRD,CHKSPACE,CHARSHIFT,CHARSHOW
                    ,E_CODE,C_CODE,NEXT_ROW,G_CODE,SHARS
             MOV R2,#01H          ;ROW COUNTER START AT ROW 1
             MOV DPTR,#8038H        ;VDO RAM ADDRESS
             MOV THA,#00H
             MOV THAPAGE,#00H        ;SET TO ENGLISH PAGE


READIIC:     MOV R1,#MTD
             MOV @R1,#08H          ;SUB ADD ECCT R8
             INC R1
             MOV @R1,#01H          ;SELECT ACT PAGE
             INC R1
             MOV A,R2
             MOV @R1,A            ;ACT ROW
             INC R1
             MOV @R1,#00H          ;ACT COL
             MOV NOTMST,#04H        ;Transmitt 4 byte
             MOV SLA,#SLAW          ;SLA+W Transmitt funct.
             SETB STA             ;SET STA IN S1CON
```

```
                CALL DELAY
                SETB STO
                MOV NOTMST,#28H       ;Transmitt 8 byte
                MOV SLA,#SLAR         ;SLA+R Recive funct.
                SETB STA          ;SET STA IN S1CON
                CALL DELAY
                SETB STO
;========================================
                MOV R1,#MRD
READMRD:        MOV A,@R1             ;SEND DATA TO PC SCREEN
                CJNE R2,#01H,CHKSPACE   ;ROW 1 ?
                CJNE R1,#MRD,CHKSPACE   ;AND COL1 ?
                CJNE A,#0AH,CHKSPACE    ;AND #0AH <IF YES THAI_PAGE>
                MOV THA,#83H          ;SO THAT CHARECTER SHIFT AND
                MOV THAPAGE,#0FFH      ;SWITCH TO THAI PAGE
CHKSPACE:       CJNE A,#20H,C_CODE     ;SPACE NO CHANGE
                SJMP CHARSHOW
C_CODE:         ANL  A,#0E0H          ;CHK CONTROL CODE
                JNZ  CHARSHIFT        ;NOT 0 = DISP CODE,0 = CONTROL CODE
E_CODE:         MOV  A,@R1
                CJNE A,#1BH,G_CODE     ;ENGLISH CODE IN PAGE OF THAI
                XRL THA,#83H
                SJMP CHARSHOW
G_CODE:         ANL  A,#18H
                CJNE A,#10H,CHARS   ;10 = GRAP COLOR 18=OTHER GRAP CTRL
                MOV A,THAPAGE
                CJNE A,#0FFH,CHARS
                XRL THA,#83H
CHARS:          MOV A,@R1
```

```
              SJMP CHARSHOW
CHARSHIFT:    MOV A,@R1
              ADD A,THA
CHARSHOW:     MOVX @DPTR,A
              CALL DELAY
              INC DPTR
              INC R1
              CJNE R1,#82H,READMRD
              INC R2
              MOV A,THAPAGE
              CJNE A,#0FFH,NEXT_ROW     ;'FF' IS THAI PAGE
              MOV  THA,#83H
              MOV  GCODE,#00H          ;RESET G_CODE SIGN
NEXT_ROW:     CJNE R2,#19H,READIIC
              %ENDM

READ_ROW0:    %MACRO
              MOV R1,#MTD
              MOV @R1,#08H           ;SUB ADD ECCT R8
              INC R1
              MOV @R1,#01H           ;SELECT ACT PAGE
              INC R1
              MOV @R1,#00H           ;ACT ROW 0
              INC R1
              MOV @R1,#04H           ;ACT COL
              MOV NOTMST,#04H          ;Transmitt 4 byte
              MOV SLA,#SLAW            ;SLA+W Transmitt funct.
              SETB STA              ;SET STA IN S1CON
              CALL DELAY
```

```
            SETB STO
            MOV NOTMST,#25H         ;Transmitt 37 byte
            MOV SLA,#SLAR           ;SLA+R Recive funct.
            SETB STA               ;SET STA IN S1CON
            CALL DELAY
            SETB STO
;========================================
            MOV  DPTR,#8010H
            MOV  A,#01H
            MOVX @DPTR,A
            INC  DPTR
            MOV  A,WRT_MAG
            MOVX @DPTR,A
            INC DPTR
            MOV  A,WRT_TEN
            MOVX @DPTR,A
            INC DPTR
            MOV  A,WRT_UNI
            MOVX @DPTR,A
            INC  DPTR
            MOV DPTR,#8014H         ;VDO RAM ADDRESS
            MOV R1,#MRD
ROW0MRD:    MOV A,@R1               ;GET DATA FROM MASTER RCV SPACE
            MOVX @DPTR,A
            CALL DELAY
            INC DPTR
            INC R1
            CJNE R1,#7FH,ROW0MRD
           %ENDM
```

```
;*********************************************************
; INITIALIZATION ROUTINE
;*********************************************************
        DEFSEG  IIC,START=00H,ABSOLUTE,CLASS=CODE
        SEG     IIC

        ORG 0000H
        LJMP CPU_INIT           ;RESET

        ORG 0003H               ;INT0 INTERUPT VECTOR
        MOV A,P1
        ANL A,#0FH
        MOV R7,A
        INC  R5
        CALL USR_INF
        RETI

;*********************************************************
; CRTC REG PARAMETER
;*********************************************************
        ORG 160H
        DB  38H,28H,2EH
        DB  04H,1CH,06H
        DB  19H,1AH,02H
        DB  09H

        ;ORG  0023H             ;VECTOR OF UART
        ;LJMP UART
```

```
;***********************************************************
;                  MAIN PROGRAM
; T9.ASM                                17/10/35
; REMOTE CONTROL AVALIBLE
;     - WRITE REMOTE DATA IN
;     - PAGE SELECT FROM DATA OF REMOTE
;     - START WITH PAGE 100
;     - TITLE SCREEN
;***********************************************************


            ORG 0200H
CPU_INIT:   MOV S1ADR,#OWNSLA       ;Load own SLA +enable
                                ;general call recognition
            SETB P1.6           ;P1.6 HIGH level
            SETB P1.7           ;P1.7 HIGH level
            SETB P1.3
            MOV  HADD,#PAG1
            ORL  IE,#ENSIO1         ;Enable SIO1 interrupt
            SETB SIO1HP             ;SET SIO1 interrupt HIGH priority
                                ;CLR SIO1 interrupt LOW  priority
            SETB IE.1           ;Enable ET0 timer0 interrupt
            SETB IE.0           ;Enable EXT int0
            SETB IP.0           ;Ext int0 HIGH priority
            MOV S1CON,#ENS1_NOTSTA_NOTSTO_NOTSI_AA_CRO
                                ;Initialize SLV funct.
            ORL PCON,#00H           ;CLEAR SMOD =0,K=1,BUAD SET
            MOV SCON,#052H          ;SET SIO0 8 BIT UART
            MOV TMOD,#021H          ;SET TIMER1 8 BIT AUTO RELOAD
                                ;   TIMER0 16BIT TIMER
            MOV TL1,#0FdH          ;SET TIMER1 LOW BYTE

            MOV TH1,#0FdH           ;SET TIMER1 HIGH BYTE,2400 buad

                              ;[ 0E8H = 1200 bps ]

                              ;[ 0F4H = 2400 bps ]

                              ;[ 0FAH = 4800 bps ]

                              ;[ 0FDH = 9600 bps ]

            SETB TCON.6            ;TIMER1 RUN

            SETB TCON.4            ;TIMER0 RUN

            SETB TCON.0            ;Int0 falling Edge

            MOV  R5,#00H           ;INTIAL VALUE OF DIGIT COUNTER

            MOV  DPTR,#UP1CON         ;PORT A,B,C0-C3 OUTPUT

            MOV  A,#88H            ;PORT C4-C7     INPUT

            MOVX @DPTR,A

            MOV  GCODE,#00H          ;CLR GRAPHIC SIGN


;---------------------------------------------------------------

; ECCT INITIAL ROUTINE                          PAGE 200

;---------------------------------------------------------------

ECCT_INIT: MOV R1,#MTD               ;SET POINTER TO MTD

            MOV @R1,#01H             ;ECCT SUB ADD OF R1

            INC R1

            MOV @R1,#05H             ;ECCT MODE SETTING

            INC R1

            MOV @R1,#10H             ;SET PAGE REQ ADD REG

            INC R1                 ;AUTO INC TO R3

            MOV @R1,#1AH              ;HOLD,MAG2,MAG1,MAG0

            INC R1

            MOV @R1,#10H              ;PAGE TEN = 0

            INC R1
```

```
          MOV @R1,#10H        ;PAGE UNIT = 0
          MOV NOTMST,#06H       ;Transmitt 6 byte
          MOV SLA,#SLAW        ;SLA+W Transmitt funct.
          SETB STA           ;SET STA IN S1CON
          CALL DELAY
          SETB STO
          MOV R1,#MTD          ;SET POINTER TO MTD
          MOV @R1,#04H         ;ECCT SUB ADD OF R4
          INC R1
          MOV @R1,#01H         ;SET DISP CHAPTER
          INC R1             ;AUTO INC TO R5
          MOV @R1,#0CCH         ;SET DISP CTRL NORMAL
                       ;#03H      PICTURE
          INC R1             ;AUTO INC TO R6
          MOV @R1,#0CCH         ;SET DISP CTRL SUBTITLE
          INC R1             ;AUTO INC TO R7
          MOV @R1,#00H         ;SET DISP MODE
          MOV NOTMST,#04H       ;Transmitt 5 byte
          MOV SLA,#SLAw        ;SLA+W Transmitt funct.
          SETB STA           ;SET STA IN S1CON
          CALL DELAY


CRTC_INIT: MOV R2,#09H          ;SET R2=09H FOR COUNT DOWN
          MOV DPTR,#160H        ;DTPR POINT TO TABLE ADD 0160H
          MOV R0,#0FFH
REG_NO:    MOV A,R2            ;SET CRTC REG.NO
          CLR P1.4            ;CRTC CS=0,WR=0,CRTC WR=0 WRITE ENABLE
          CLR P1.5            ;CRTC RS=0 ADDRESS REG
```

```
        MOVX @R0,A           ;OUT DATA BUS
        MOVC A,@A+DPTR
        SETB P1.5          ;CRTC RS=1
        MOVX @R0,A           ;SET CRTC REG.
        SETB P1.4          ;WRITE CRTC DISABLE,CS=1
        DJNZ R2,REG_NO         ;DOWN TO R1

        MOV A,#00H           ;SET CRTC REG.NO 0
        CLR P1.4           ;CRTC CS=0,CRTC WR=0 WRITE ENABLE
        CLR P1.5           ;CRTC RS=0 ADDRESS REG
        MOVX @R0,A           ;OUT DATA BUS
        MOVC A,@A+DPTR
        SETB P1.5          ;CRTC RS=1
        MOVX @R0,A           ;SET CRTC REG.
        SETB P1.4          ;WRITE CRTC DISABLE,CS =1

        MOV  WRT_MAG,#”-”
        MOV  WRT_TEN,#”-”
        MOV  WRT_UNI,#”-”

        CALL CLR_SCR
        MOV DPTR,#8040H        ;VDO RAM ADDRESS
        MOV R1,#00H
TITLE:  MOV A,R1
        CALL C_TITLE
        MOVX @DPTR,A
        INC DPTR
        INC R1
        CJNE R1,#1AH,TITLE1
```

```
          MOV  DPTR,#81ACH

TITLE1:        CJNE R1,#2FH,TITLE2

          MOV  DPTR,#83C0H

TITLE2:        CJNE R1,#3BH,TITLE


;++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++

; MAIN PROGRAM

;++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++

MAIN:          READ_ROW0

          CALL ROW25

          CJNE R5,#03H,MAIN_END

          PAG_REQ PAG_MAG,PAG_TEN,PAG_UNI

          MOV  R5,#00H          ;RESET COUNTER TO ZERO

MAIN_END:      CALL DELAY

          LJMP MAIN

;++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++


;_____________________________________________________

; SIO0 BYTE SEND/RECIVE ROUTINE

;_____________________________________________________

UART:          PUSH PSW

          JB  TI,SBYTE

          JB  RI,RBYTE

          POP PSW

          RETI


 SBYTE:        JNB TI,$              ;WAIT FOR PREV DATA

                                  ;HAS BEEN TRANSMITTED.

          CLR TI
```

```
            MOV SBUF,A
            RET

RBYTE:      JNB RI,$              ;WAIT FOR PREV DATA
                                  ;HAS BEEN RECIVED.
            CLR RI
            MOV A,SBUF
            RET

;*************************************************************
;FOUND ROUTINE
;*************************************************************
DELAY:      MOV   R6,#0FFH          ;COUNT DOWN VALUE
LOOP:       DJNZ  R6,LOOP
            MOV   R6,#0FFH          ;COUNT DOWN VALUE
LOOP1:      DJNZ  R6,LOOP1
            MOV   R6,#0FFH          ;COUNT DOWN VALUE
            RET

ROW25:      MOV R1,#MTD
            MOV @R1,#08H            ;SUB ADD ECCT R8
             INC R1
            MOV @R1,#01H            ;SELECT ACT PAGE
             INC R1
             MOV @R1,#19H            ;ACT ROW 25
             INC R1
             MOV @R1,#08H            ;ACT COL AT 8
             MOV NOTMST,#04H            ;Transmitt 4 byte
             MOV SLA,#SLAW            ;SLA+W Transmitt funct.
            SETB STA              ;SET STA IN S1CON
            CALL DELAY
            SETB STO
            MOV NOTMST,#02H          ;Recieve 2 byte
            MOV SLA,#SLAR          ;SLA+R Recive funct.
            SETB STA              ;SET STA IN S1CON
            CALL DELAY
            SETB STO


            MOV R1,#MRD
            MOV A,@R1              ;SEND DATA TO PC SCREEN
            ANL A,#10H
            CJNE A,#10H,FOUND       ;CHK FOUND BIT
NOT_FOUND:LJMP RETURN
FOUND:      READ_PAGE
            CALL DELAY
            MOV R1,#MTD            ;SET POINTER TO MTD
            MOV @R1,#08H           ;ECCT SUB ADD OF R8
            INC R1
            MOV @R1,#01H           ;SET ACTV CHAPTER
            INC R1               ;AUTO INC TO R9
            MOV @R1,#19H           ;SET ACTV ROW
            INC R1               ;AUTO INC TO R10
            MOV @R1,#08H           ;SET ACTV COL
            INC R1               ;AUTO INC TO R11
            MOV @R1,#0FFH           ;SET DATA FOUND
            MOV NOTMST,#05H          ;Transmitt 5 Byte
            MOV SLA,#SLAw           ;SLA+W Transmitt funct.
            SETB STA              ;SET STA IN S1CON
            MOV  WRT_MAG,#”-”
            MOV  WRT_TEN,#”-”
            MOV  WRT_UNI,#”-”
RETURN:     RET

CLR_SCR:   MOV DPTR,#8010H          ;DTPR POINT TO VDO RAM
           MOV R4,#19H
           MOV A,#00H
SHOWR:     MOV R3,#028H
SHOWC:     MOVX @DPTR,A
            INC  DPTR
           DJNZ R3,SHOWC
           DJNZ R4,SHOWR
           RET

USR_INF:   MOV  A,R7
MAG_DIGIT:CJNE R5,#01H,TEN_DIGIT
            MOV  PAG_MAG,A
            ADD  A,#30H
            MOV  WRT_MAG,A
            MOV  WRT_TEN,#”-”
            MOV  WRT_UNI,#”-”
            AJMP RMOT_RTN
TEN_DIGIT:CJNE R5,#02H,UNI_DIGIT
            MOV PAG_TEN,A
             ADD  A,#30H
            MOV  WRT_TEN,A
             MOV  WRT_UNI,#”-”
            AJMP RMOT_RTN
```

```
UNI_DIGIT:CJNE R5,#03H,RMOT_RTN
            MOV PAG_UNI,A
            ADD  A,#30H
            MOV  WRT_UNI,A
RMOT_RTN:RET

C_TITLE:   INC  A
            MOVC A,@A+PC
            RET
          DB 1CH,02H,’T’,’E’,’L’,’E’,’T’,’E’,’X’,’T’,’ ‘
           DB ‘ ‘,’D’,’E’,’C’,’O’,’D’,’E’,’R’,’ ‘
            DB ‘ ‘,’ ‘,’V’,’1',’.’,’0'
           DB 1CH,04H,’D’,’ ‘,’S’,’ ‘,’R’,’ ‘,’L’,’ ‘,’ ‘,’ ‘
           DB ‘C’,’ ‘,’H’,’ ‘,’U’,’ ‘,’L’,’ ‘,’A’,’ ‘
           DB 1CH,05H,’B’,’Y’,’.’,’.’,’S’,’a’,’y’,’a’,’n’

             include “inti2c.asm”
             END.
```

ประวัติผู้เขียน

นายสายัณห์ ธีรปัญญาวัฒน์ เกิดวันที่ 6 มกราคม 2509 ณ.กรุงเทพมหานคร สำเร็จการศึกษา ปริญญาตรีวิศวกรรมศาสตร์ สาขาวิศวกรรมไฟฟ้า จากมหาวิทยาลัยขอนแก่น ในปีการศึกษา 2529 และเข้าศึกษาต่อในหลักสูตรวิศวกรรมศาสตรมหาบัณฑิต ที่จุฬาลงกรณ์มหาวิทยาลัย เมื่อ พ.ศ.2533 ปัจจุบันเป็นพนักงานรัฐวิสาหกิจ สังกัดองค์การโทรศัพท์แห่งประเทศไทย