รายการอ้างอิง

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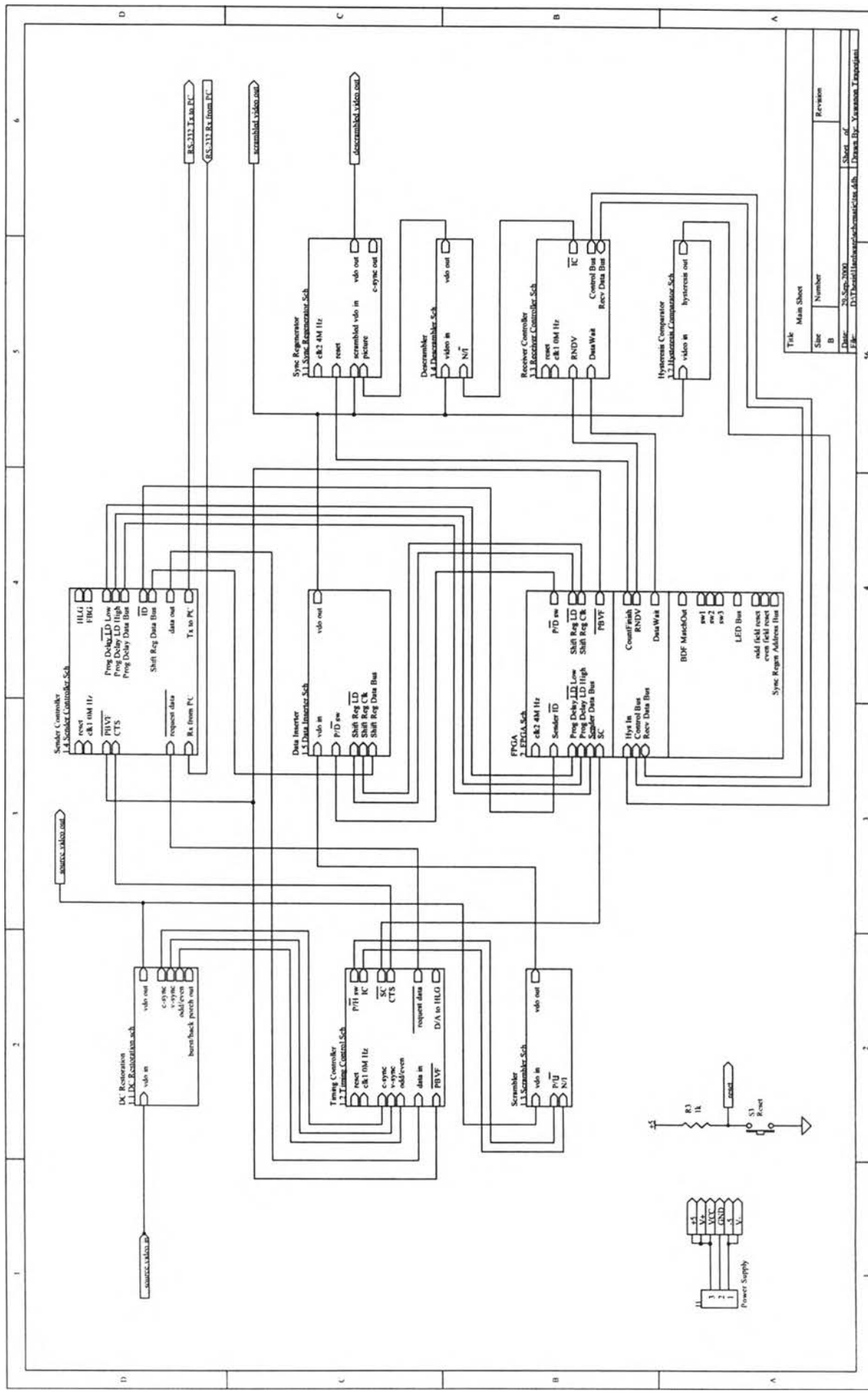
ภาคผนวก ก
แผนภาพวงจรต้นแบบเครื่องสแครมเบิลและดีสแครมเบิล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Main Sheet
Size
B
Number
Revision
Date:
29-Sep-2000
Sheet of
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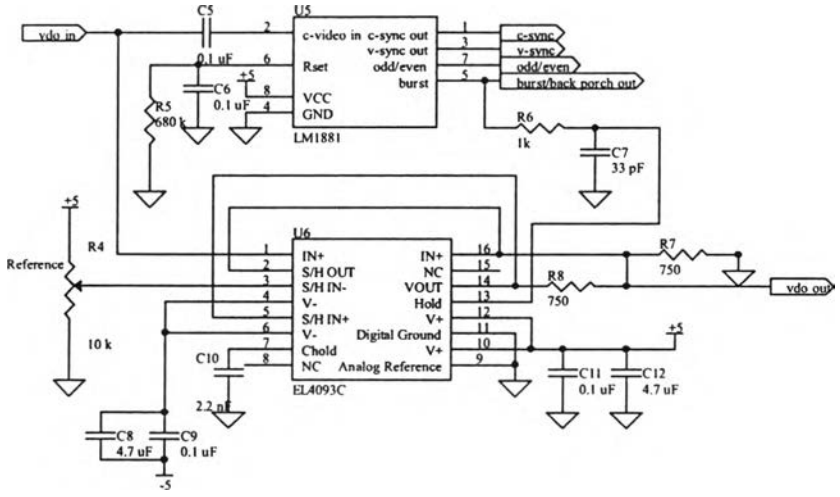
Drawn By:
Yuvarajan Trapojini
RS-232 Tx to PC
RS-232 Rx from PC
scrambled video out
descrambled video out
Sync Regenerator
1.1 Sync Regenerator.Sch
clk2 4M Hz
reset
scrambled vdo in
picture
vdo out
c-sync out
Descrambler
1.4 Descrambler.Sch
video in
N/I
vdo out
Receiver Controller
1.3 Receiver Controller.Sch
reset
clk1 6M Hz
RNDV
DataWait
I2C
Control Bus
Recv Data Bus
Hysteresis Comparator
1.2 Hysteresis Comparator.Sch
video in
hysteresis out
Sender Controller
1.4 Sender Controller.Sch
reset
clk1 6M Hz
P/H/V
CTS
request data
Rx from PC
HLG
PBG
Prog Delay LD Low
Prog Delay LD High
Prog Delay Data Bus
ID
Shift Reg Data Bus
data out
Tx to PC
Data Inserter
1.5 Data Inserter.Sch
vdo in
P/D sw
Shift Reg LD
Shift Reg Clk
Shift Reg Data Bus
vdo out
FPGA
1.7 FPGA.Sch
clk2 4M Hz
Sender ID
P/D sw
Prog Delay LD Low
Prog Delay LD High
Sender Data Bus
SC
Shift Reg LD
Shift Reg Clk
P/H/V
Hys In
Control Bus
Recv Data Bus
CountFinish
RNDV
DataWait
BDF MatchOut
sw1
sw2
sw3
LED Bus
odd field reset
even field reset
Sync Regen Address Bus
source video out
DC Restoration
1.1 DC Restoration.sch
vdo in
vdo out
c-sync
v-sync
odd/even
burst back porch out
Timing Controller
1.7 Timing Control.Sch
reset
clk1 6M Hz
I2C
c-sync
v-sync
odd/even
data in
P/H/V
P/H sw
SC
CTS
request data
D/A to HLG
Scrambler
1.6 Scrambler.Sch
vdo in
P/D sw
N/I
vdo out
source video in
+5
R3
1k
reset
S1
Reset
Power Supply
+5
Vo
Vcc
GND
-5
Vo
J1
3
2
1



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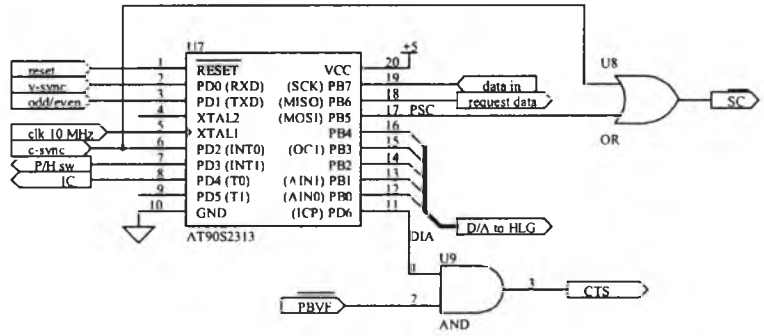

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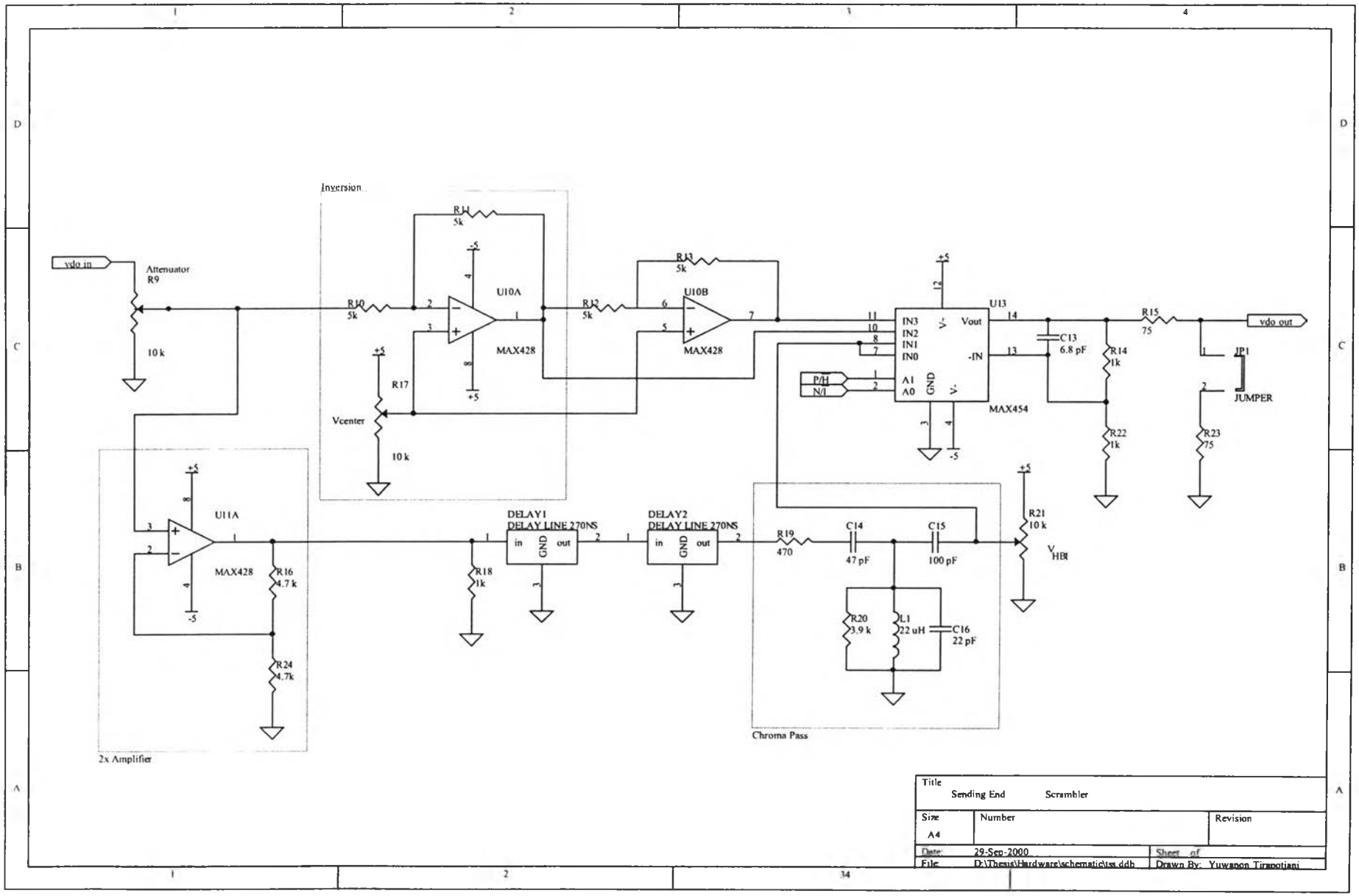
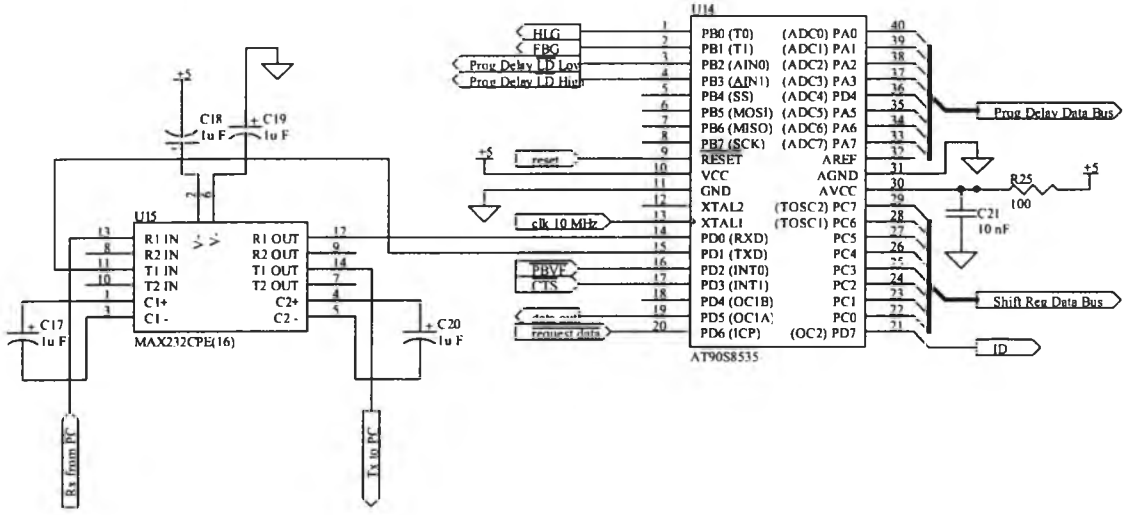
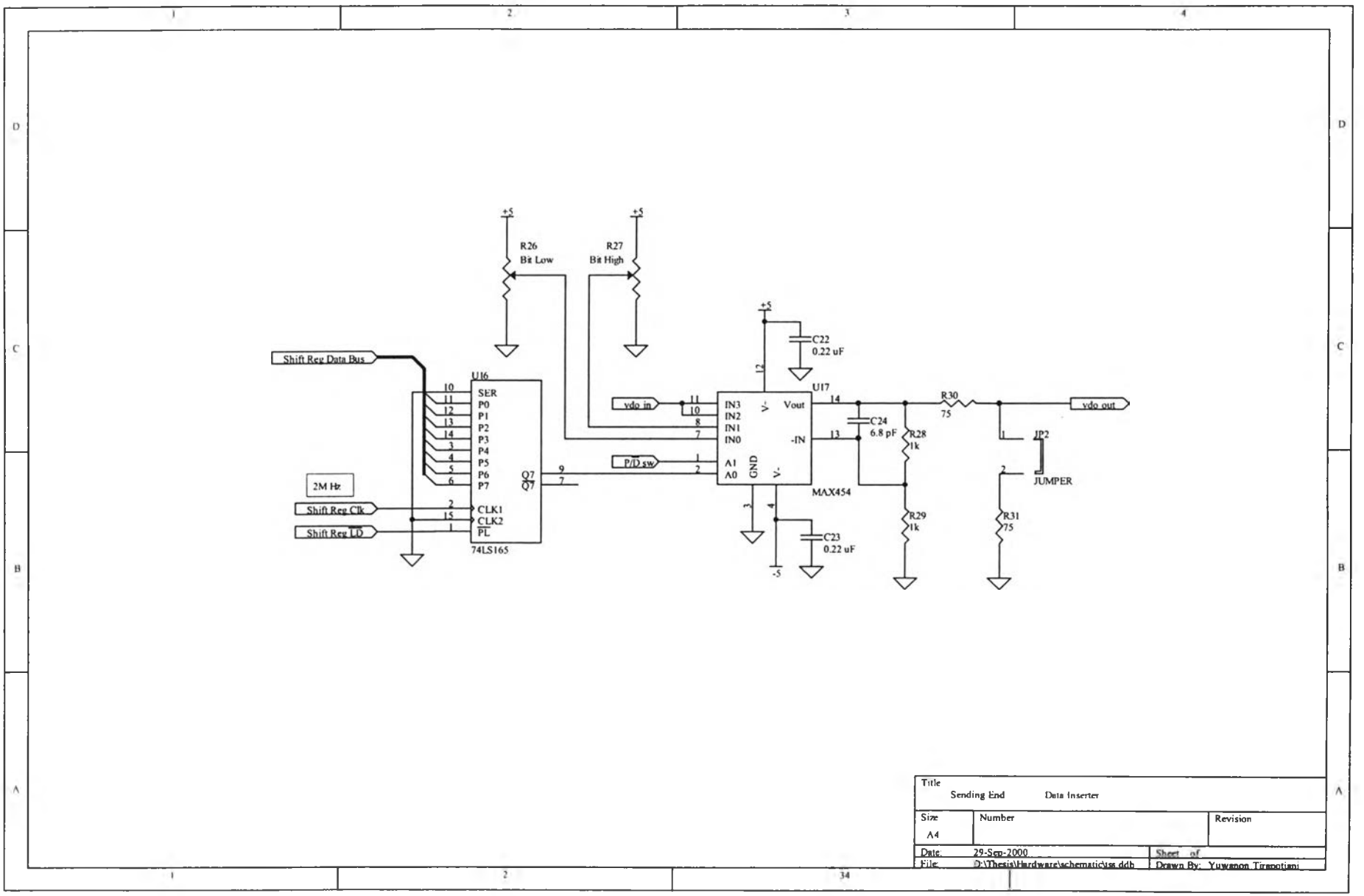
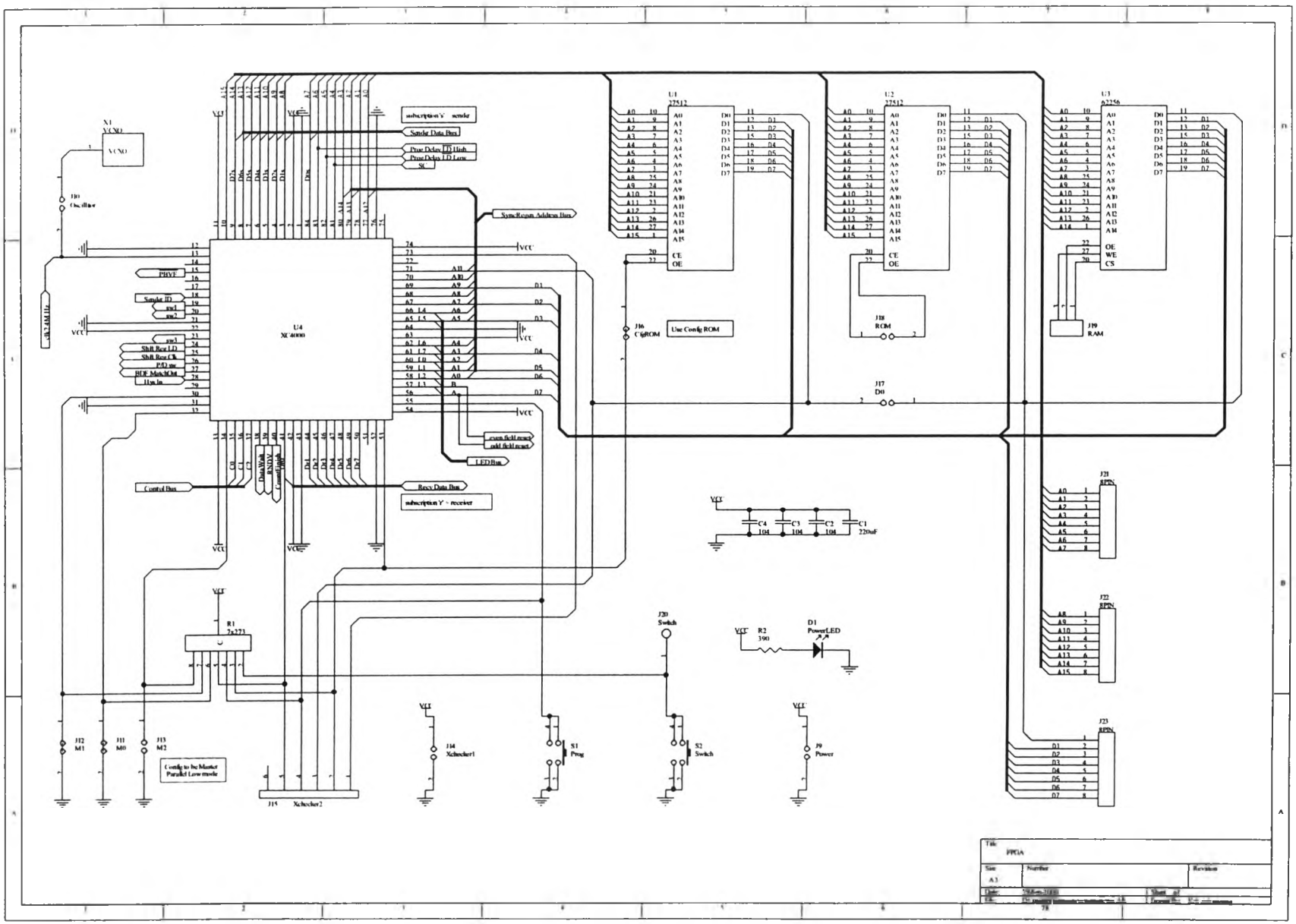
Size: A4	Number:	Revision:
Date: 29-Sep-2000		Sheet of
File: D:\Thesis\Hardware\schematic\tss.ddb		Drawn By: Yuwanon Tirapotiani


Inversion
vdo in
Attenuator
R9
10 k
R11
5k
U10A
MAX428
R10
5k
R12
5k
R13
5k
U10B
MAX428
R17
Vcenter
10 k
+5
-5
U13
MAX454
IN3
IN2
IN1
IN0
Vout
-IN
P/H
N/I
A1
A0
GND
V-
C13
6.8 pF
R14
1k
R22
1k
R15
75
R23
75
JP1
JUMPER
vdo out
U11A
MAX428
R16
4.7 k
R24
4.7k
2x Amplifier
DELAY1
DELAY LINE 270NS
DELAY2
DELAY LINE 270NS
in
GND
out
R18
1k
R19
470
C14
47 pF
C15
100 pF
R21
10 k
V_HBI
R20
3.9 k
L1
22 uH
C16
22 pF
Chroma Pass
Title
Sending End Scrambler
Size
A4
Number
Revision
Date: 29-Sep-2000
Sheet of
File: D:\Thesis\Hardware\schematic\ss.ddb
Drawn By: Yuwasan Tirapotjani



Title: Sending End Controller		
Size: A4	Number	Revision
Date: 29-Sep-2000	Sheet of	
File: D:\Thesis\Hardware\schematic\tss.ddb	Drawn By: Yuwanon Tiamsiriamai	


+5
R26
Bit Low
R27
Bit High
+5
+5
C22
0.22 uF
Shift Reg Data Bus
U16
SER
P0
P1
P2
P3
P4
P5
P6
P7
Q7
Q7
ydo in
IN3
IN2
IN1
IN0
V-
Vout
-IN
U17
R30
75
ydo out
C24
6.8 pF
R28
1k
JP2
JUMPER
P/D sw
A1
A0
GND
V-
2M Hz
Shift Reg Clk
Shift Reg LD
CLK1
CLK2
PL
74LS165
MAX454
R29
1k
R31
75
C23
0.22 uF
-5
Title
Sending End Data Inserter
Size
A4
Number
Revision
Date: 29-Sep-2000
Sheet of
File: D:\Thesis\Hardware\schematic\ss.ddb
Drawn By: Yuwanon Tirapotjani


X1
VCXO
VCXO
Y0
Oscillator
U4
XC4000
U1
27512
U2
27512
U3
62256
J16
Config ROM
Use Config ROM
J18
ROM
J19
RAM
J17
D0
PHYF
Sampler ID
sw1
sw2
sw3
Shift Reg LD
Shift Reg Clk
P/S sw
BDF MatchOut
Hsw In
Control Bus
Recv Data Bus
subscription 'Y' - receiver
subscription 'x' - sender
Sampler Data Bus
Prior Delay TD High
Prior Delay TD Low
SC
Sync/Resync Address Bus
even field reset
odd field reset
LED Bus
C4
104
C3
104
C2
104
C1
220uF
R1
7x273
R2
390
D1
PowerLED
J20
Switch
J12
M1
J11
M0
J13
M2
Config to be Master
Parallel Low mode
J14
Xchecker1
J15
Xchecker2
S1
Prog
S2
Switch
J9
Power
J21
RPIN
J22
RPIN
J23
RPIN
Title
FPGA
Size
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Number
Revision
Date:
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of
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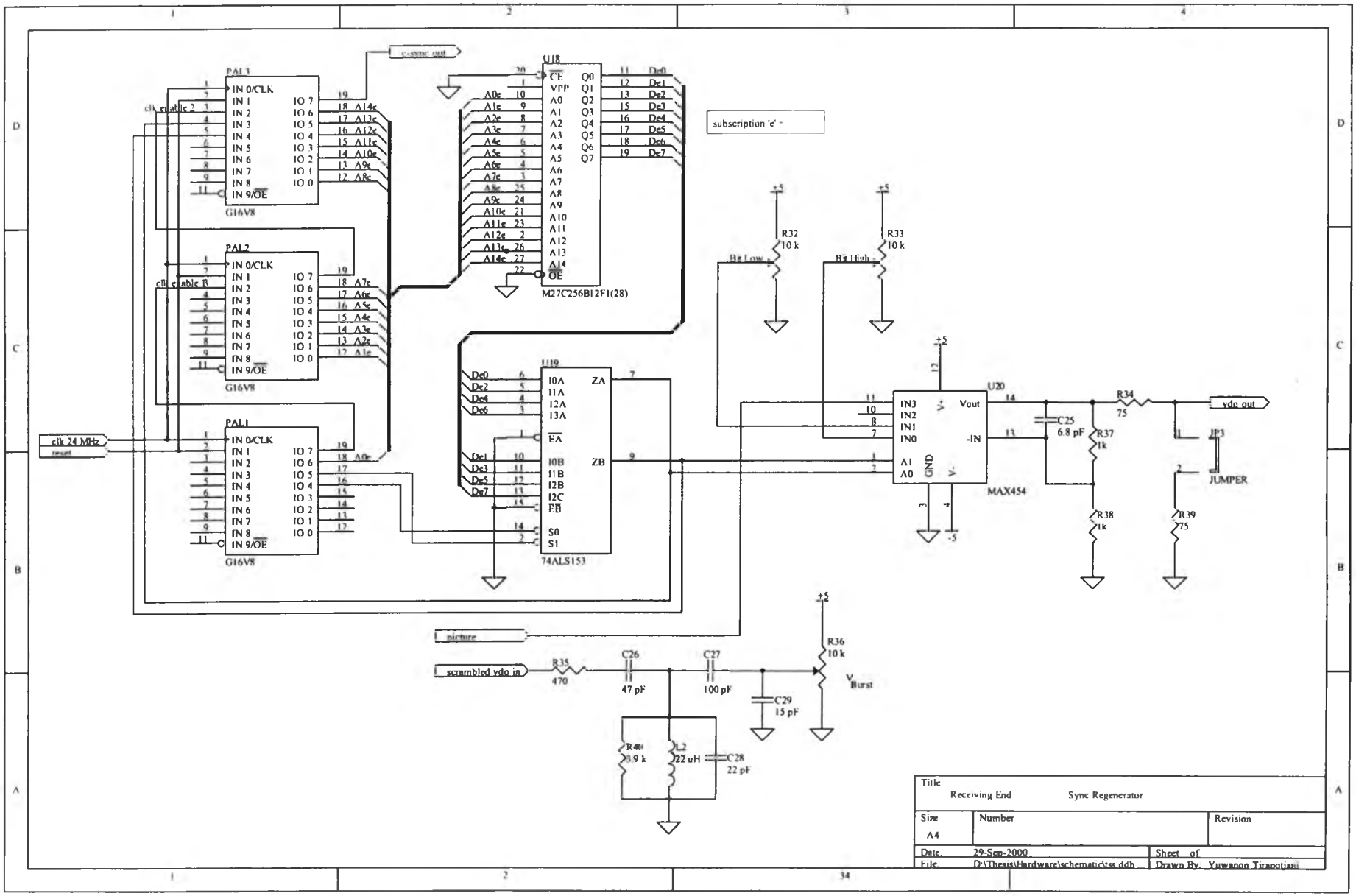
PAL3
PAL2
PAL1
G16V8
clk 24 MHz
reset
clk enable 2
clk enable 1
c-sync out
U18
M27C256B12F1(28)
subscription 'e' =
Bit Low
Bit High
R32
10 k
R33
10 k
U19
74ALS153
U20
MAX454
C25
6.8 pF
R34
75
R37
1k
R38
1k
R39
75
JP3
JUMPER
vdo out
picture
scrambled vdo in
R35
470
C26
47 pF
C27
100 pF
C29
15 pF
R36
10 k
R40
3.9 k
L2
22 uH
C28
22 pF
Title
Receiving End
Sync Regenerator
Size
A4
Number
Revision
Date:
29-Sep-2000
Sheet of
File:
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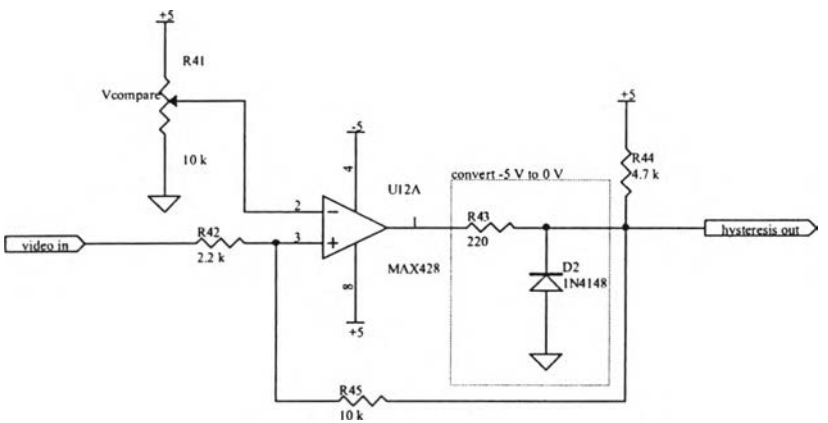
Drawn By:
Yuwanon Tirapotiani



Title: Receiving End Hysteresis Comparator		
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Date: 29-Sep-2000		Sheet of
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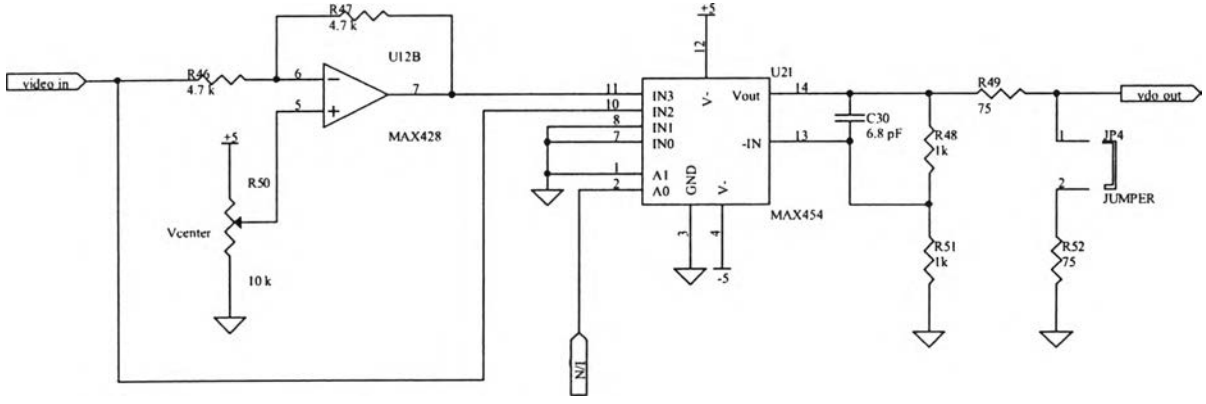

Title: Receiving End Descrambler		
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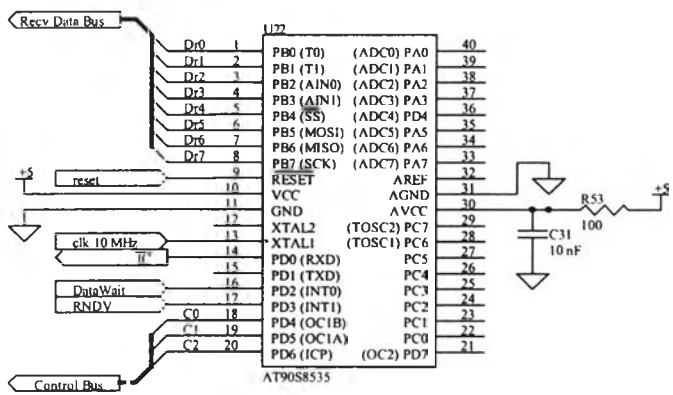
Date: 29-Sep-2000		Sheet of
File: D:\Thesis\Hardware\schematic\tss.ddb		Drawn By: Yuwanon Tirapotiani



Title: Receiving End Controller		
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ประวัติผู้เขียนวิทยานิพนธ์

นายยุวนนท์ ธีรพจนี เกิดวันที่ 9 กรกฎาคม พ.ศ. 2518 ที่จังหวัดกรุงเทพมหานคร สำเร็จการศึกษาชั้นมัธยมศึกษาตอนปลายจากโรงเรียนเตรียมอุดมศึกษา ในปีการศึกษา 2535 ระหว่างนี้ได้รับคัดเลือกให้เป็นตัวแทนประเทศไทยเข้าแข่งขันคอมพิวเตอร์โอลิมปิกระหว่างประเทศ ครั้งที่ 5 ณ ประเทศอาร์เจนตินา ได้รับรางวัลเหรียญเงิน

สำเร็จการศึกษาปริญญาตรีวิศวกรรมศาสตรบัณฑิต สาขาวิศวกรรมไฟฟ้า จากคณะวิศวกรรมศาสตร์ จุฬาลงกรณ์มหาวิทยาลัยในปีการศึกษา 2539 และเข้าศึกษาต่อในหลักสูตรวิศวกรรมศาสตรมหาบัณฑิตสาขาวิศวกรรมไฟฟ้า (แขนงวิชาระบบเชิงเลข) ที่คณะวิศวกรรมศาสตร์ จุฬาลงกรณ์มหาวิทยาลัย